PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT3749006

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ADVANCED MICRO DEVICES, INC.	02/12/2016

RECEIVING PARTY DATA

Name:	CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.
Street Address:	515 LEGGET DRIVE
Internal Address:	SUITE 704
City:	OTTAWA
State/Country:	ONTARIO
Postal Code:	K2K3G4

PROPERTY NUMBERS Total: 48

Property Type	Number
Patent Number:	6210999
Patent Number:	6057209
Patent Number:	6462416
Patent Number:	6518154
Patent Number:	6365450
Patent Number:	6380091
Patent Number:	6410967
Patent Number:	6518646
Patent Number:	6531347
Patent Number:	6611029
Patent Number:	6812119
Patent Number:	6861350
Patent Number:	6686248
Patent Number:	6724051
Patent Number:	7034361
Patent Number:	6821713
Patent Number:	7005358
Patent Number:	6524947
Patent Number:	6573172

Property Type	Number
Patent Number:	7473623
Patent Number:	7906424
Patent Number:	7754556
Patent Number:	8183605
Patent Number:	7696052
Patent Number:	8274120
Patent Number:	8318598
Patent Number:	5937302
Patent Number:	5989964
Patent Number:	5885879
Patent Number:	6372588
Patent Number:	5970347
Patent Number:	6399505
Patent Number:	6159814
Patent Number:	6069046
Patent Number:	6090712
Patent Number:	6265253
Patent Number:	6127259
Patent Number:	6358803
Patent Number:	7071101
Patent Number:	6635409
Patent Number:	6936480
Patent Number:	7141502
Patent Number:	7091097
Patent Number:	7504287
Patent Number:	7531403
Patent Number:	7986008
Patent Number:	7816199
Patent Number:	6500754

CORRESPONDENCE DATA

Fax Number: (613)591-8148

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 613-576-3000
Email: ipadmin@conversantip.com
Correspondent Name: RONAN O'BYRNE
Address Line 1: 515 LEGGET DRIVE, SUITE 704
Address Line 2: CONVERSANT IPM
Address Line 4: OTTAWA, ONTARIO K2K3G4

ATTORNEY DOCKET NUMBER:	AMD ASSIGNMENT SUBMISSION
NAME OF SUBMITTER:	RONAN O'BYRNE
SIGNATURE:	/Ronan O'Byrne/
DATE SIGNED:	02/22/2016

Total Attachments: 9
source=AMD_Assignment#page1.tif
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Exhibit C

ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, Advanced Micro Devices, Inc., a Delaware corporation, with a registered address at One AMD Place, Sunnyvale, CA 94088-3453 USA ("**Assignor**"), does hereby assign, transfer and convey unto Conversant Intellectual Property Management, Inc., a Canadian corporation, with an office at 515 Legget Drive, Suite 704, Ottawa, ON K2K3G4, Canada ("**Assignee**"), all of Assignor's entire right, title and interest in and to all patents and patent applications listed in the attached Exhibit 1 (collectively "**Patent Rights**"), subject to the terms and conditions of the Confidential Purchase and Sale Agreement (the "**Agreement**"). Assignor and Assignee acknowledge that some of the Patent Rights may be currently expired or abandoned.

In addition, Assignor agrees to and hereby does sell, assign, transfer and convey unto Assignee all rights (i) in and to causes of action and enforcement rights for the Patent Rights including all rights to pursue damages, injunctive relief and other remedies for past, present and future infringement of the Patent Rights, (ii) the right to apply (or continue prosecution) in any and all countries of the world for patents, design patents, utility models, certificates of invention or other governmental grants for the Patent Rights, including under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding, and (iii) the rights, if any, to revive prosecution of any abandoned Patent Rights.

Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents or certificates of invention or equivalent which may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment shall inure to the benefit of Assignee, its successor and other legal representatives, and shall be binding upon Assignor, its successor, assigns and other legal representatives.

IN WITNESS WHEREOF, this Assignment of Patent Rights is executed at Sunnyvale, CA on Feb 12, 2016 @2:17p.

ASSIGNOR

By: [signature]

Name: Kevin O'Neil

Title: VP, IP & Licensing

(Signature must be notarized)

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document.

State of California)
)
County of Santa Clara)

On February 12, 2016 before me, Rita S. Marquis, Notary Public personally appeared Kevin A. O'Neil, who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/~~are~~ subscribed to the within instrument and acknowledged to me that he/~~she~~/they executed the same in his/~~her~~/their authorized capacity(~~ies~~) and that by his/~~her~~/their signature(~~s~~) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[signature]
Notary Public

RITA S. MARQUIS
Commission # 2054591
Notary Public - California
Santa Clara County
My Comm. Expires Feb 5, 2018

[SEAL

IN TESTIMONY WHEREOF, in accepting said Assignment, I hereunto set my hand as of the date indicated below:

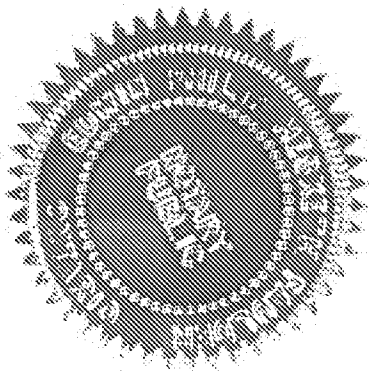
Conversant Intellectual Property Management, Inc.

16 Feb, 2016
Date

Signature

Name: Scott Burt
Title: SVP, Chief IP officer

(Signature must be notarized)



Before me, EDWIN PH FAULDER
Notary Public at ONTARIO, CANADA
Date: 16 FEB, 2016

Exhibit 1

Family	AMD Family	Title	Country	App No.	File Date	Patent No.	Issue Date
05900	TT2935	METHOD AND TEST STRUCTURE FOR LOW-TEMPERATURE INTEGRATION OF HIGH DIELECTRIC CONSTANT GATE DIELECTRICS INTO SELF-ALIGNED SEMICONDUCTOR DEVICES	US	09/285,047	12/4/1998	6,210,999	4/3/2001
05901	TT1824	A PROCESS OF MANUFACTURING A SEMICONDUCTOR DEVICE HAVING A NITROGEN BEARING ISOLATION REGION	US	08/891,278	7/10/1997	6,057,209	5/2/2000
05901	TT1824	SEMICONDUCTOR DEVICE HAVING A NITROGEN BEARING ISOLATION REGION AND PROCESS OF MANUFACTURE	WO	PCT/US1998/008113	3/27/1998	WO 1999/003149	1/21/1999
05902	F0345	GRADATED BARRIER LAYER IN INTEGRATED CIRCUIT INTERCONNECTS	US	09/905,469	7/13/2001	6,462,416	10/8/2002
05903	F0934	METHOD OF FORMING SEMICONDUCTOR DEVICES WITH DIFFERENTLY COMPOSED METAL-BASED GATE ELECTRODES	US	09/813,310	3/21/2001	6,518,154	2/11/2003
05904	G0027	FABRICATION OF P-CHANNEL FIELD EFFECT TRANSISTOR WITH MINIMIZED DEGRADATION OF METAL OXIDE GATE	US	09/809,706	3/15/2001	6,365,450	4/2/2002
05905	D429	DUAL DAMASCENE ARRANGEMENT FOR METAL INTERCONNECTION WITH OXIDE DIELECTRIC LAYER AND LOW K DIELECTRIC CONSTANT LAYER	US	09/238,050	1/27/1999	6,380,091	4/30/2002
05906	TT2680	TRANSISTOR HAVING ENHANCED METAL SILICIDE AND A SELF-ALIGNED GATE ELECTRODE	US	09/173,273	10/15/1998	6,410,967	6/25/2002
05907	F0391	SEMICONDUCTOR DEVICE WITH VARIABLE COMPOSITION LOW-K INTER-LAYER DIELECTRIC AND METHOD OF MAKING	US	09/819,615	3/29/2001	6,518,646	2/11/2003
05908	D621	RECESSED SOURCE/DRAIN FORMATION FOR FRINGING CAPACITANCE REDUCTION	US	60/181,086	2/8/2000		
05908	D621	RECESSED SOURCE DRAINS TO REDUCE FRINGING CAPACITANCE	US	09/776,713	2/6/2001	6,531,347	3/11/2003
05909	H1105	DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	US	10/290,158	11/8/2002	6,611,029	8/26/2003
05909	H1105	DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	TW	092130612	11/3/2003	311371	6/21/2009
05909	H1105	DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	US	10/602,061	6/24/2003		
05909	H1105	DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	WO	PCT/US2003/032662	10/14/2003	WO2004/044992	5/27/2004

Family	AMD Family	Title	Country	App No.	File Date	Patent No.	Issue Date
05909	H1105	DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	CN	200380102759.0	10/14/2003	100459166	2/4/2009
05909	H1105	DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	DE	10393687.4	10/14/2003	10393687	12/6/2012
05909	H1105	DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	GB	0504833.5	10/14/2003	2408849	6/28/2006
05909	H1105	DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	JP	2004551527	10/14/2003		
05909	H1105	DOUBLE GATE SEMICONDUCTOR DEVICE HAVING SEPARATE GATES	KR	10-2005-7008204	10/14/2003	1029383	4/15/2011
05910	H1477	NARROW FINS BY OXIDATION IN DOUBLE-GATE FINFET	US	10/614,052	7/8/2003	6,812,119	11/2/2004
05911	H1393	METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE COMPRISING SILICON-RICH TASIN METAL GATE ELECTRODE	US	10/464,508	6/19/2003	6,861,350	3/1/2005
05912	G0036	METHOD OF FABRICATING A SEMICONDUCTOR DEVICE HAVING A MOS TRANSISTOR WITH A HIGH DIELECTRIC CONSTANT MATERIAL	US	09/825,658	4/3/2001	6,686,248	2/3/2004
05913	F0238	NICKEL SILICIDE PROCESS USING NON-REACTIVE SPACER	US	09/679,877	10/5/2000	6,724,051	4/20/2004
05914	H1491	NARROW BODY RAISED SOURCE/DRAIN METAL GATE MOSFET	US	10/653,234	9/3/2003	7,034,361	4/25/2006
05915	G1277	METHOD FOR LATERAL TRIMMING OF SPACERS	US	10/085,242	2/27/2002	6,821,713	11/23/2004
05916	DE0339	TECHNIQUE FOR FORMING RECESSED SIDEWALL SPACERS FOR A POLYSILICON LINE	DE	10335100.0	7/31/2003	10335100.0	6/5/2008
05916	DE0339	TECHNIQUE FOR FORMING RECESSED SIDEWALL SPACERS FOR A POLYSILICON LINE	US	10/786,401	2/25/2004	7,005,358	2/28/2006
05917	F0389	SLOTTED TRENCH DUAL INLAID STRUCTURE AND METHOD OF FORMING THEREOF	US	09/774,800	2/1/2001	6,524,947	2/25/2003
05918	H0481	METHODS FOR IMPROVING CARRIER MOBILITY OF PMOS AND NMOS DEVICES	US	10/244,439	9/16/2002	6,573,132	6/3/2003
05919	TT5996	PROVIDING STRESS UNIFORMITY IN A SEMICONDUCTOR DEVICE	US	11/428,032	6/30/2006	7,473,623	1/6/2009
05919	TT5996	PROVIDING STRESS UNIFORMITY IN A SEMICONDUCTOR DEVICE	WO	PCT/US2007/007842	3/29/2007	WO2008/005083	1/10/2008
05919	TT5996	PROVIDING STRESS UNIFORMITY IN A SEMICONDUCTOR DEVICE	TW	20070122851	6/25/2007	404146	8/1/2013
05920	070098	CONDUCTOR BUMP METHOD AND APPARATUS	US	11/832,486	8/1/2007	7,906,424	3/15/2011
05920	070098	UNDER BUMP ROUTING LAYER METHOD AND APPARATUS	US	11/949,951	12/4/2007		
05920	070098	UNDER BUMP ROUTING LAYER METHOD AND APPARATUS	WO	PCT/IB2008/003343	12/4/2008	WO2009/071982	6/11/2009

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05920	070098	SEMICONDUCTOR DEVICE HAVING A BUMP ELECTRODE AND METHOD FOR ITS MANUFACTURE	WO	PCT/IB2008/002024	8/1/2008	WO2009/016495	2/5/2009
05920	070098	CONDUCTOR BUMP METHOD AND APPARATUS	US	13/027,076	2/14/2011	8,294,266	10/23/2012
05920	070098	UNDER BUMP ROUTING LAYER METHOD AND APPARATUS	CN	200880126089.9	12/4/2008	101952962	
05920	070098	UNDER BUMP ROUTING LAYER METHOD AND APPARATUS	EP	08855955.4	12/4/2008		
05920	070098	UNDER BUMP ROUTING LAYER METHOD AND APPARATUS	IN	4835/DELNP/2010	12/4/2008		
05920	070098	UNDER BUMP ROUTING LAYER METHOD AND APPARATUS	JP	2010536543	12/4/2008	5567489	
05920	070098	UNDER BUMP ROUTING LAYER METHOD AND APPARATUS	JP	2013030065	2/19/2013	5654067	
05920	070098	UNDER BUMP ROUTING LAYER METHOD AND APPARATUS	KR	10-2010-7014910	12/4/2008		
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	DE	102007030053.2	6/29/2007	102007030053.0	7/21/2011
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	US	12/027,583	2/7/2008	7,754,556	7/13/2010
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	TW	200801240048.0	6/27/2008	471044	2/1/2015
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	WO	PCT/US08/08150	6/30/2008	WO2009/005785	01.08.2009
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	US	12/791,290	6/1/2010	8,183,605	5/22/2012
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	CN	200880022751.6	6/30/2008	ZL200880022751.6	2/27/2013
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	EP	8794399.9	6/30/2008	2168152	1/18/2012
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	DE	8794399.9	6/30/2008	602008012726.5	1/18/2012
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	GB	8794399.9	6/30/2008	2168152	1/18/2012
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	IN	8532/DELNP/2009	6/30/2008		
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	JP	2010514849	6/30/2008	5244908	4/12/2013
05921	DE0939	REDUCING TRANSISTOR JUNCTION CAPACITANCE BY RECESSING DRAIN AND SOURCE REGIONS	EP	11192120.1	6/30/2008		

Family	AMD Family	Title	Country	App No.	File Date	Patent No.	Issue Date
05922	DE0691	TECHNIQUE FOR PROVIDING STRESS SOURCES IN TRANSISTORS IN CLOSE PROXIMITY TO A CHANNEL REGION BY RECESSING DRAIN AND SOURCE REGIONS	DE	102006015077.5	3/31/2006	102006015077.0	12/23/2010
05922	DE0691	TECHNIQUE FOR PROVIDING STRESS SOURCES IN TRANSISTORS IN CLOSE PROXIMITY TO A CHANNEL REGION BY RECESSING DRAIN AND SOURCE REGIONS	US	11/558,006	11/9/2006	7,696,052	4/13/2010
05922	DE0691	TECHNIQUE FOR PROVIDING STRESS SOURCES IN TRANSISTORS IN CLOSE PROXIMITY TO A CHANNEL REGION BY RECESSING DRAIN AND SOURCE REGIONS	TW	096109293	3/19/2007		
05922	DE0691	TECHNIQUE FOR PROVIDING STRESS SOURCES IN TRANSISTORS IN CLOSE PROXIMITY TO A CHANNEL REGION BY RECESSING DRAIN AND SOURCE REGIONS	WO	PCT/US07/04689	2/21/2007	WO2007-126495	11/8/2007
05922	DE0691	TECHNIQUE FOR PROVIDING STRESS SOURCES IN TRANSISTORS IN CLOSE PROXIMITY TO A CHANNEL REGION BY RECESSING DRAIN AND SOURCE REGIONS	US	12/710,744	2/23/2010	8,274,120	9/25/2012
05922	DE0691	TECHNIQUE FOR PROVIDING STRESS SOURCES IN TRANSISTORS IN CLOSE PROXIMITY TO A CHANNEL REGION BY RECESSING DRAIN AND SOURCE REGIONS	CN	200780011436.9	2/21/2007	101416287	7/21/2010
05922	DE0691	TECHNIQUE FOR PROVIDING STRESS SOURCES IN TRANSISTORS IN CLOSE PROXIMITY TO A CHANNEL REGION BY RECESSING DRAIN AND SOURCE REGIONS	GB	0817592.9	2/21/2007	2449824	2/22/2011
05922	DE0691	TECHNIQUE FOR PROVIDING STRESS SOURCES IN TRANSISTORS IN CLOSE PROXIMITY TO A CHANNEL REGION BY RECESSING DRAIN AND SOURCE REGIONS	JP	2009-502792	2/21/2007	5576655	7/11/2014
05922	DE0691	TECHNIQUE FOR PROVIDING STRESS SOURCES IN TRANSISTORS IN CLOSE PROXIMITY TO A CHANNEL REGION BY RECESSING DRAIN AND SOURCE REGIONS	KR	10-2008-7026877	2/21/2007	1430703	8/8/2014
05923	DE1113	CONTACTS AND VIAS OF A SEMICONDUCTOR DEVICE FORMED BY A HARD MASK AND DOUBLE EXPOSURE	DE	102008049727.4	9/30/2008		
05923	DE1113	CONTACTS AND VIAS OF A SEMICONDUCTOR DEVICE FORMED BY A HARD MASK AND DOUBLE EXPOSURE	US	12/537,321	8/7/2009	8,318,598	11/27/2012
05923	DE1113	CONTACTS AND VIAS OF A SEMICONDUCTOR DEVICE FORMED BY A HARD MASK AND DOUBLE EXPOSURE	WO	PCT/EP2009/00780	9/29/2009	2010037521	WO/2010/037521

Family	AMD Family	Title	Country	App No.	File Date	Patent No.	Issue Date
85923	DE1113	CONTACTS AND VIAS OF A SEMICONDUCTOR DEVICE FORMED BY A HARD MASK AND DOUBLE EXPOSURE	CN	200980141244.9	9/29/2009	102187453	6/25/2014
85923	DE1113	CONTACTS AND VIAS OF A SEMICONDUCTOR DEVICE FORMED BY A HARD MASK AND DOUBLE EXPOSURE	IN	2309/DELNP/2011	9/29/2009		
85923	DE1113	CONTACTS AND VIAS OF A SEMICONDUCTOR DEVICE FORMED BY A HARD MASK AND DOUBLE EXPOSURE	JP	2011528254	9/29/2009	5732395	4/17/2015
85923	DE1113	CONTACTS AND VIAS OF A SEMICONDUCTOR DEVICE FORMED BY A HARD MASK AND DOUBLE EXPOSURE	KR	10-2011-7010115	9/29/2009	1539415	7/20/2015
85924	TT1503	METHOD OF FORMING LIGHTLY DOPED DRAIN REGION AND HEAVILY DOPING A GATE USING A SINGLE IMPLANT STEP	US	08/781,002	1/8/1997	5,937,302	8/10/1999
85925	TT1506	POST-SPACER LDD IMPLANT FOR SHALLOW LDD TRANSISTOR	US	08/818,427	3/17/1997	5,989,964	11/23/1999
85926	TT1507	THIN POLYSILICON MASKING TECHNIQUE FOR IMPROVED LITHOGRAPHY CONTROL	US	08/822,941	3/21/1997	5,885,879	3/23/1999
85926	TT1507	THIN POLYSILICON MASKING TECHNIQUE FOR IMPROVED LITHOGRAPHY CONTROL	US	09/217,234	12/21/1998		
85927	TT1175	METHOD OF MAKING AN IGFET USING SOLID PHASE DIFFUSION TO DOPE THE GATE, SOURCE AND DRAIN	US	08/837,523	4/21/1997	6,372,588	4/16/2002
85928	TT1536	HIGH PERFORMANCE MOSFET TRANSISTOR FABRICATION TECHNIQUE	US	08/896,400	7/18/1997	5,970,347	10/19/1999
85929	C669497	METHOD AND SYSTEM FOR COPPER INTERCONNECT FORMATION	US	08/954,175	10/20/1997	6,399,505	6/4/2002
85930	TT2087	SPACER FORMATION BY POLY STACK DOPANT PROFILE DESIGN	US	08/968,444	11/12/1997	6,159,814	12/12/2000
85931	TT1961	TRANSISTOR FABRICATION EMPLOYING IMPLANTATION OF DOPANT INTO JUNCTIONS	US	08/979,282	11/26/1997	6,069,046	5/30/2000
85932	C432397	SHALLOW TRENCH ISOLATION FORMATION WITH NO POLISH STOP	US	08/992,489	12/18/1997	6,090,712	7/18/2000
85933	D655	ALUMINUM DISPOSABLE SPACER TO REDUCE MASK COUNT IN CMOS TRANSISTOR FORMATION	US	09/305,098	5/5/1999	6,265,253	7/24/2001
85934	D874	PHOSPHORIC ACID PROCESS FOR REMOVAL OF CONTACT BARC LAYER	US	09/372,443	8/11/1999	6,127,259	10/3/2000
85935	TT3477	METHOD OF FABRICATING A DEEP SOURCE/DRAIN	US	09/489,369	1/21/2000	6,358,803	3/19/2002
85936	D730	SACRIFICIAL TIN ARC LAYER FOR INCREASED PAD ETCH THROUGHPUT	US	09/208,325	12/9/1998	7,071,101	7/4/2006
85937	F0815	METHOD OF STRENGTHENING PHOTORESIST TO PREVENT PATTERN COLLAPSE	US	09/962,588	9/12/2001	6,635,409	10/21/2003

Family	AMD Family	Title	Country	App No.	File Date	Patent No.	Issue Date
05938	DE0190	METHOD OF CONTROLLING THE CHEMICAL MECHANICAL POLISHING OF STACKED LAYERS HAVING A SURFACE TOPOLOGY	DE	10234956.8	7/31/2002	10234956	1/4/2007
05938	DE0190	METHOD OF CONTROLLING THE CHEMICAL MECHANICAL POLISHING OF STACKED LAYERS HAVING A SURFACE TOPOLOGY	US	10/304,573	11/26/2002	6,936,480	8/30/2005
05939	H1213	SLURRY-LESS POLISHING FOR REMOVAL OF EXCESS INTERCONNECT MATERIAL DURING FABRICATION OF A SILICON INTEGRATED CIRCUIT	US	10/673,597	9/29/2003	7,141,502	11/28/2006
05940	G0340	END-OF-RANGE DEFECT MINIMIZATION IN SEMICONDUCTOR DEVICE	US	10/933,424	9/3/2004	7,091,097	8/15/2006
05941	NY0167	METHODS FOR FABRICATING AN INTEGRATED CIRCUIT	US	11/689,764	3/22/2007	7,504,287	3/17/2009
05942	H2289	SOI SEMICONDUCTOR COMPONENTS AND METHODS FOR THEIR FABRICATION	US	11/538,001	10/2/2006	7,531,403	5/12/2009
05942	H2289	SOI SEMICONDUCTOR COMPONENTS AND METHODS FOR THEIR FABRICATION	US	12/413,185	3/27/2009	7,986,008	7/26/2011
05943	DE0970	METHOD OF FORMING A SEMICONDUCTOR STRUCTURE COMPRISING AN IMPLANTATION OF IONS OF A NON-DOPING ELEMENT	DE	102007035838.7	7/31/2007	102007035838.0	8/29/2014
05943	DE0970	METHOD OF FORMING A SEMICONDUCTOR STRUCTURE COMPRISING AN IMPLANTATION OF IONS OF A NON-DOPING ELEMENT	US	12/037,533	2/26/2008	7,816,199	10/19/2010
05944	F0325	ANNEAL HILLOCK SUPPRESSION METHOD IN INTEGRATED CIRCUIT INTERCONNECTS	US	60/245,690	11/2/2000		
05944	F0325	ANNEAL HILLOCK SUPPRESSION METHOD IN INTEGRATED CIRCUIT INTERCONNECTS	US	09/999,661	10/31/2001	6,500,754	12/31/2002