PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3785554

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
TRIAD SEMICONDUCTOR, INC.	03/02/2016

RECEIVING PARTY DATA

Name:	SILICON VALLEY BANK
Street Address:	380 INTERLOCKEN CRESCENT, SUITE 600
City:	BROOMFIELD
State/Country:	COLORADO
Postal Code:	80021

PROPERTY NUMBERS Total: 14

Property Type	Number
Patent Number:	6580289
Patent Number:	6693454
Patent Number:	6873185
Patent Number:	7248071
Patent Number:	7334208
Patent Number:	7378874
Patent Number:	7538580
Patent Number:	7692309
Patent Number:	7930670
Patent Number:	7335966
Patent Number:	7449371
Patent Number:	7595229
Patent Number:	7626272
Patent Number:	7972907

CORRESPONDENCE DATA

Fax Number: (800)494-7512

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 202-370-4750
Email: ipteam@nationalcorp.com

Correspondent Name:	JOANNA MCCALL
Address Line 1:	1025 VERMONT AVE NW, SUITE 1130
Address Line 2:	NATIONAL CORPORATE RESEARCH, LTD
Address Line 4:	WASHINGTON, D.C. 20005

ATTORNEY DOCKET NUMBER:	F161894
NAME OF SUBMITTER:	JAMES WON
SIGNATURE:	/James Won/
DATE SIGNED:	03/16/2016

Total Attachments: 11
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AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Amended and Restated Intellectual Property Security Agreement (this "Agreement") is entered into as of March 2, 2016 by and between **SILICON VALLEY BANK**, a California corporation, with a loan production office located at 380 Interlocken Crescent, Suite 600, Broomfield, Colorado 80021 ("Bank") and **TRIAD SEMICONDUCTOR, INC.**, a Florida corporation, with its principal place of business located at 1760 Jonestown Road, Winston-Salem, North Carolina 27103 ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodations to Grantor (the "Loans") in the amounts and manner set forth in that certain Amended and Restated Loan and Security Agreement by and between Bank and Grantor dated as of March 2, 2016 (as the same has been and as may be further amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in its Copyrights, Trademarks, Patents, and Mask Works (as each term is described below) to secure the obligations of Grantor to Bank.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of Grantor's obligations to Bank, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

1. Grant of Security Interest. To secure Grantor's obligations to Bank, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "Intellectual Property Collateral"), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work of authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "Copyrights");

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the

same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto (collectively, the "Trademarks");

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "Mask Works");

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

2. Recordation. Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement upon request by Bank.

3. Loan Documents. This Agreement has been entered into pursuant to and in conjunction with the Loan Agreement, which is hereby incorporated by reference. The provisions of the Loan Agreement shall supersede and control over any conflicting or inconsistent provision herein. The rights and remedies of Bank with respect to the Intellectual Property Collateral are as provided by the Loan Agreement and related documents, and nothing in this Agreement shall be deemed to limit such rights and remedies.

4. Execution in Counterparts. This Agreement may be executed in counterparts (and by different parties hereto in different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a signature page to this Agreement by facsimile or in electronic (i.e., "pdf" or "tif" format) shall be effective as delivery of a manually executed counterpart of this Agreement.

5. Successors and Assigns. This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

6. Governing Law. This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby and thereby shall be governed by, and construed in accordance with, the laws of the United States and the Commonwealth of Massachusetts, without giving effect to any choice or conflict of law provision or rule (whether of the Commonwealth of Massachusetts or any other jurisdiction).

7. Amended and Restated Agreement. This Agreement amends and restates, and replaces, that certain Intellectual Property Security Agreement dated as of November 30, 2015, between Grantor and Bank, as amended.

[Signature page follows.]

QCK

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

TRIAD SEMICONDUCTOR, INC.

By: James C. Kemerling

Title: Vice President

BANK:

SILICON VALLEY BANK

By:_____

Title:_____

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

TRIAD SEMICONDUCTOR, INC.

By:_____

Title: Vice President

BANK:

SILICON VALLEY BANK

By: Zach Norris

Title: Vice President

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EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date
None		

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EXHIBIT B

Patents

Description	Registration/ Application Number	Registration/ Application Date
See Attachment		

9CK

Current Patent Inventory
Triad Semiconductor, Inc. (consolidated)

Patents:

U.S. Patent No. 6,580,289 issued June 17, 2003 for "Cell Architecture to Reduce Customization in a Semiconductor Device"

U.S. Patent No. 6,693,454 issued February 17, 2004 for "Distributed Ram in a Logic Array"

U.S. Patent No. 6,873,185 issued March 29, 2005 for "Logic Array Devices Having Complex Macro-Cell Architecture and Methods Facilitating Use of Same"

U.S. Patent No. 7,248,071 B2 issued July 24, 2007 for "Logic Array Devices Having Complex Macro-Cell Architecture and Methods Facilitating Use of Same"

U.S. Patent No. 7,334,208 B1 issued February 19, 2008 for "Customization of Structured ASIC Devices Using Pre-Process Extraction of Routing Information"

U.S. Patent No. 7,378,874 B2 issued May 27, 2008 for "Creating High-Drive Logic Devices from Standard Gates with Minimal Use of Custom Masks"

U.S. Patent No. 7,538,580 issued May 26, 2009 for "Logic Array Devices Having Complex Macro-Cell Architecture and Methods Facilitating Use of Same"

U.S. Patent No. 7,692,309 issued April 6, 2010 for "Configuring Structured ASIC Fabric Using Two Non-adjacent Via Layers"

U.S. Patent No. 7,930,670 issued April 19, 2011 for "Using Selectable In-line Inverters to Reduce the Number of Inverters in a Semiconductor Design"

U.S. Patent No. 7,335,966 B2 issued February 26, 2008 for "Configurable Integrated Circuit Capacitor Array Using Via Mask Layers"

U.S. Patent No. 7,449,371 B2 issued November 11, 2008 for "Via Configurable Architecture for Customization of Analog Circuitry in a Semiconductor Device"

U.S. Patent No. 7,595,229 B2 issued September 29, 2009 for "Configurable Integrated Circuit Capacitor Array Using Via Mask Layers"

U.S. Patent No. 7,626,272 B2 issued December 1, 2009 for "Via Configurable Architecture for Customization of Analog Circuitry in a Semiconductor Device"

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U.S. Patent No. 7,972,907 issued July 5, 2011 for "Via Configurable Architecture for Customization of Analog Circuitry in a Semiconductor Device"

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EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date
None		

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EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date
None		

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