

PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT3807642

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
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JEREMY LEE	03/30/2016
PRAMODCHANDRAN VARIYAM	03/23/2016
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Property Type	Number
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DATE SIGNED:	03/30/2016
Total Attachments: 4	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: ANORA LLC

§ Inventors: JAYASHREE SAXENA, ET AL.

§ Customer No. 96658

Filed: Herewith

§ Attorney Docket No.: 15AN702-NP

For: DETERMINING TEST CONDITIONS FOR AT-SPEED TRANSITION DELAY FAULT TESTS ON SEMICONDUCTOR DEVICES

PATENT ASSIGNMENT

I, the undersigned inventor, for good and valuable consideration, the receipt of which is hereby acknowledged, hereby:

1. Assign to Anora LLC, a Texas limited liability company (hereinafter "Assignee") the entire right, title and interest throughout the world, including the United States of America, its Territories, Possessions, and Puerto Rico, in and to the above-entitled invention and application for patent and all Letters Patents issuing thereon, and any non-provisional, continuation, continuation-in-part or division of the application and any reissue or extension of the Letters Patents.
2. Agree to execute any documents that legally may be required in connection with the filing, prosecution and maintenance of the application or any other patent applications anywhere in the world, including the United States for the invention, including additional documents that may be required to affirm the rights of Assignee in and to the invention, all without further consideration.
3. Authorize and request the Commissioner of Patents and Trademarks of the United States to issue any and all Letters Patent that may be granted upon any patent application or any additional, continuing or divisional applications thereof to the Assignee, its successors and assigns.

SIGNATURE PAGES TO FOLLOW

INVENTORS: SAXENA, ET AL.

TITLE: DETERMINING TEST CONDITIONS FOR AT-SPEED TRANSITION DELAY FAULT TESTS ON
SEMICONDUCTOR DEVICES

ATTORNEY DOCKET NO.: 15AN702-NP

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Jayashree Saxena

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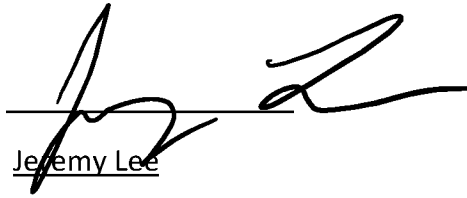
3/23/16

INVENTORS: SAXENA, ET AL.

TITLE: DETERMINING TEST CONDITIONS FOR AT-SPEED TRANSITION DELAY FAULT TESTS ON
SEMICONDUCTOR DEVICES

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INVENTORS: SAXENA, ET AL.

TITLE: DETERMINING TEST CONDITIONS FOR AT-SPEED TRANSITION DELAY FAULT TESTS ON
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