

## PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1  
 Stylesheet Version v1.2

EPAS ID: PAT3821574

|   |   |
|---|---|
| <b>SUBMISSION TYPE:</b>   | NEW ASSIGNMENT                          |
| <b>NATURE OF CONVEYANCE:</b>  | ASSIGNMENT                              |
| <b>CONVEYING PARTY DATA</b>   |   |
| <b>Name</b>   | <b>Execution Date</b>                   |
| KHEE YONG LIM   | 02/04/2016                              |
| JAE HAN CHA   | 02/04/2016                              |
| CHIA CHING YEO  | 02/04/2016                              |
| KIOK BOONE ELGIN QUEK   | 02/04/2016                              |
| <b>RECEIVING PARTY DATA</b>   |   |
| <b>Name:</b>  | GLOBALFOUNDRIES SINGAPORE PTE. LTD.     |
| <b>Street Address:</b>  | 60 WOODLANDS INDUSTRIAL PARK D STREET 2 |
| <b>City:</b>  | SINGAPORE                               |
| <b>State/Country:</b>   | SINGAPORE                               |
| <b>Postal Code:</b>   | 738406                                  |
| <b>PROPERTY NUMBERS Total: 1</b>  |   |
| <b>Property Type</b>  | <b>Number</b>                           |
| <b>Application Number:</b>  | 15093888                                |
| <b>CORRESPONDENCE DATA</b>  |   |
| <b>Fax Number:</b>  | (480)385-5061                           |
| <i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i> |   |
| <b>Phone:</b>   | 480-385-5060                            |
| <b>Email:</b>   | docketing@ifllaw.com                    |
| <b>Correspondent Name:</b>  | INGRASSIA FISHER & LORENZ, P.C. (GF)    |
| <b>Address Line 1:</b>  | 7010 E. COCHISE RD.                     |
| <b>Address Line 4:</b>  | SCOTTSDALE, ARIZONA 85253               |
| <b>ATTORNEY DOCKET NUMBER:</b>  | 126.0097 (HSG032)                       |
| <b>NAME OF SUBMITTER:</b>   | RYAN T. FORTIN                          |
| <b>SIGNATURE:</b>   | /Ryan T. Fortin/                        |
| <b>DATE SIGNED:</b>   | 04/08/2016                              |
| <b>Total Attachments: 4</b>   |   |
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| source=20160408_Assignment#page2.tif  |   |
| source=20160408_Assignment#page3.tif  |   |



**COMBINED DECLARATION and ASSIGNMENT (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)**

**Title of  
Invention**

**METHODS FOR FABRICATING INTEGRATED CIRCUITS WITH LOW, MEDIUM, AND/OR HIGH VOLTAGE TRANSISTORS ON AN EXTREMELY THIN SILICON-ON-INSULATOR SUBSTRATE**

**DECLARATION**

As the below named inventor, I hereby declare that:

This declaration  
is directed to:



The attached application, or



United States application or PCT international application number \_\_\_\_\_ filed on \_\_\_\_\_

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I have reviewed and understand the contents of the application and am aware of the duty to disclose to the US Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR § 1.56.

**ASSIGNMENT**

For good and valuable consideration, the receipt, sufficiency and adequacy of which are hereby acknowledged, I hereby sell, assign, transfer, to GLOBALFOUNDRIES Singapore Pte. Ltd. having a business address of 60 Woodlands Industrial Park D Street 2, Singapore 738406 its successors and assigns, absolutely and forever, my entire right, title and interest in and to the invention listed above, together with the Application, any and all Patents that may issue in the United States and/or any foreign countries, and any reissues, re-examinations, renewals, continuations, continuation-in-parts, divisionals or extensions thereof that may be issued or granted, and all right, title and interest to the inventions contained in said Patents and Applications, for the United States and all foreign countries, and all the rights and privileges relating thereto including but not limited to the priority rights arising from said Applications, the right to recover and take all such proceedings as may be necessary for the recovery of damages or otherwise in respect of past, present and future infringement, and the right to apply for, take and maintain patents on said inventions.

If any portion of this Combined Declaration or Assignment is held unenforceable, then remaining portions hereof shall nevertheless remain in full force and effect.

**LEGAL NAME OF INVENTOR**

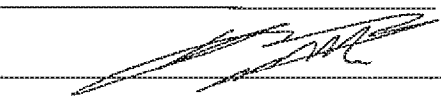
Inventor: Khee Yong Lim

Date: Feb, 4, 2016

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional form for each additional inventor.

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| <b>Title of<br/>Invention</b>  | <b>METHODS FOR FABRICATING INTEGRATED CIRCUITS WITH LOW,<br/>MEDIUM, AND/OR HIGH VOLTAGE TRANSISTORS ON AN<br/>EXTREMELY THIN SILICON-ON-INSULATOR SUBSTRATE</b>                    |
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| <b>LEGAL NAME OF INVENTOR</b>  |   |
| Inventor: Jae Han Cha  | Date: 4 <sup>th</sup> Feb. 2016   |
| Signature:    |   |
| Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional form for each additional inventor.  |   |

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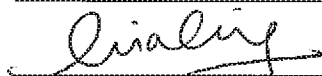
### LEGAL NAME OF INVENTOR

Inventor: Chia Ching Yeo

Date:

4/2/2016

Signature:



Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional form for each additional inventor.

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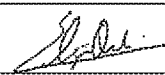
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**LEGAL NAME OF INVENTOR**

Inventor: Kiok Boone Elgin Quek

Date: Feb 4, 2016

Signature: 

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