

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3828276

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
OCZ STORAGE SOLUTIONS, INC.	03/30/2016
RECEIVING PARTY DATA	
Name:	TOSHIBA CORPORATION
Street Address:	1-1, SHIBAURA 1-CHOME
City:	MINATO-KU, TOKYO
State/Country:	JAPAN
Postal Code:	105-8001
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	14458614
CORRESPONDENCE DATA	
Fax Number:	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
Phone:	202-626-3600
Email:	toshibapatents@whitecase.com
Correspondent Name:	WHITE & CASE LLP
Address Line 1:	701 13TH STREET NW
Address Line 4:	WASHINGTON, D.C. 20005
ATTORNEY DOCKET NUMBER:	1283810-0105
NAME OF SUBMITTER:	DAVID M. TENNANT
SIGNATURE:	/David M. Tennant/
DATE SIGNED:	04/13/2016
Total Attachments: 11	
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PATENT ASSIGNMENT AGREEMENT

This Patent Assignment Agreement (the “Agreement”), dated as of March 30, 2016 (the “Effective Date”), is made by OCZ Storage Solutions, Inc., a California corporation, located at 6373 San Ignacio Avenue, San Jose, CA 95119 (“Assignor”), and Toshiba Corporation, a Japanese corporation, located at 1-1 Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan (“Purchaser”), the purchaser of certain assets of Assignor pursuant to an Asset Purchase Agreement between Assignor and Purchaser, dated March 25th, 2016 (the “Asset Purchase Agreement”), and assignee of certain assets of Assignor assigned pursuant to an FY2015A Technical Services Agreement, dated April 1, 2015 (the “FY15A TSA”) and an FY2015B Technical Services Agreement, dated October 1, 2015 (the “FY15B TSA”).

WHEREAS, Assignor is the sole owner of the patents and patent applications listed in Exhibit A attached to this Agreement;

WHEREAS, under the terms of the Asset Purchase Agreement, Assignor has agreed to sell, assign, transfer, and convey to Purchaser, among other assets, the patents and patent applications listed in Exhibit A that were filed prior to April 1, 2015;

WHEREAS, under the terms of the FY15A TSA, Assignor assigned, transferred, and conveyed to Purchaser, among other assets, the patents and patent applications listed in Exhibit A that were filed on or after April 1, 2015 but prior to October 1, 2015;

WHEREAS, under the terms of the FY15B TSA, Assignor assigned, transferred, and conveyed to Purchaser, among other assets, the patents and patent applications listed in Exhibit A that were filed on or after October 1, 2015;

WHEREAS, Purchaser desires to confirm its acquisition of all right, title, and interest in and to the patents and patent applications listed in Exhibit A, including the related rights described below; and

WHEREAS, Assignor will therefore deliver this Agreement and other intellectual property assignment agreements, for recording with the United States Patent and Trademark Office and corresponding entities or agencies in any applicable jurisdictions.

NOW THEREFORE, Assignor and Purchaser agree as follows:

1. Assignment. For good and valuable consideration, the receipt of which is hereby acknowledged, Assignor hereby does and agrees to (and to the extent applicable, confirms that it already has done the following) irrevocably sell, assign, transfer and convey to Purchaser and its successors and assigns, all right, title and interest that may exist today and in the future in and to any and all:

- (a) the patents and patent applications listed in Exhibit A attached to this Agreement;

- (b) patents and patent applications to which any of the patents or patent applications listed in Exhibit A directly or indirectly claim, or forms the basis for, priority anywhere in the world, including the right of priority;
 - (c) reissues, reexaminations, extensions, continuations, continuations-in-part, continuing prosecution applications and divisions of any of the items under (a) or (b) of Section 1 of this Agreement;
 - (d) foreign counterparts to any of the items under (a), (b) or (c) of Section 1 of this Agreement, including utility models, inventors' certificates, industrial design protection and any other form of governmental grants or issuances for the protection of inventions, designs or discoveries;
 - (e) inventions, invention disclosures, designs and discoveries claimed in the items under (a) through (d) of Section 1 of this Agreement;
 - (f) patents that issue from any of the items under (a) through (e) of Section 1 of this Agreement (collectively the items listed in (a) through (f), the "**Patents**");
 - (g) claims, causes of action and enforcement rights of any kind, whether currently pending, filed or otherwise, and whether known or unknown, under or arising from any of the items under (a) through (f) of Section 1 of this Agreement, including all rights to pursue and collect damages, costs, injunctive relief and other remedies for past, current, or future infringement of the Patents, and including rights afforded under 35 U.S.C. § 154(d);
 - (h) royalties, income and other payments due as of the Effective Date or thereafter under or arising from any of the items under (a) through (g) of Section 1 of this Agreement; and
 - (i) rights to apply for, file, register, maintain, extend and renew in any or all countries of the world patents, certificates of invention, utility models, industrial design protection, design patent protection and other governmental grants or issuances of any kind related to any of the items under (a) through (h) of Section 1 of this Agreement.
2. Further Actions. Assignor shall take such steps and actions, and provide such cooperation and assistance to Purchaser and its successors, assigns and legal representatives, including the execution and delivery of any affidavits, declarations, oaths, exhibits, assignments, powers of attorney, or other documents, as may be necessary to effect, evidence or perfect the assignment of the Patents contemplated hereby to Purchaser, or any assignee or successor.
3. Recordation. Assignor hereby authorizes and requests the Commissioner for Patents in the United States Patent and Trademark Office and the officials in any of the corresponding patent offices in the applicable jurisdictions to issue any and all patents, utility models or

other governmental grants or issuances pertaining to any of the items assigned hereunder in the name of Purchaser.

4. Terms of the Asset Purchase Agreement. The parties hereto acknowledge and agree that this Agreement is entered into in connection with the Asset Purchase Agreement, FY15A TSA, and FY15B TSA, to which reference is made for a further statement of the rights and obligations of Assignor and Purchaser with respect to the sale of the Patents.
5. Counterparts. This Agreement may be executed in counterparts, each of which shall be deemed an original, but all of which together shall be deemed to be one and the same agreement. A signed copy of this Agreement delivered by e-mail or other means of electronic transmission shall be deemed to have the same legal effect as delivery of an original signed copy of this Agreement.
6. Governing Law. This Agreement will be deemed to be made and in all respects will be interpreted, construed and governed by and in accordance with the laws of the United States and the State of California without regard to the conflicts of laws principles thereof.
7. Successors and Assigns. This Agreement will inure to the benefit of Purchaser and its successors, assigns and other legal representatives and is binding upon Assignor and its successors, assigns, heirs and legal representatives.

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IN WITNESS WHEREOF, the parties have duly executed this Agreement as of the Effective Date.

ASSIGNOR:

DATE: March 30, 2016

OCZ STORAGE SOLUTIONS, INC.

By: Ralph Schmitt
Printed/Typed Name

Title: CEO


Signature

PURCHASER:

DATE: March 29th, 2016

TOSHIBA CORPORATION

By: Tomoharu Watanabe
Printed/Typed Name

Title: Vice President, Memory Division

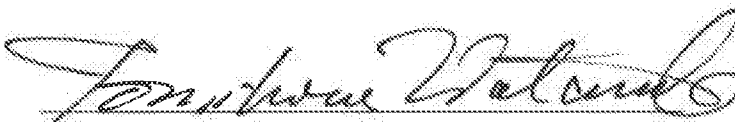

Signature

Exhibit A

Country	App No.	Title	Filing Date (US Format)
US	08/482,924	Method for correcting single bit hard errors	07/07/95
US	08/641,934	Solid state disk drive address generator with multiplier circuit	02/05/96
US	29/142,455	Computer	05/29/01
US	29/180,860	Computer	04/29/03
US	10/731,636	Exchange server method and system	12/08/03
US	10/711,653	Method and Apparatus for Increasing Computer Memory Performance	09/29/04
US	10/907,420	Method for Increasing Stability of System Memory through Enhanced Quality of Supply Power	03/31/05
US	11/138,768	Method of increasing DDR memory bandwidth in DDR SDRAM modules	05/25/05
TW	TW094117251A	Method of increasing DDR memory bandwidth in DDR SDRAM modules	05/26/05
US	11/162,029	Memory Module Having On-Package or On-Module Termination	08/25/05
US	11/164,835	On-Device Data Compression to Increase Speed of Flash Memory-Based Mass Storage Devices	12/07/05
US	11/621,396	Method and Apparatus for Improved Thermal Management of Computer Memory Modules	01/09/07
KR	10-2007-0139108	Flash Memory device and Flash memory programming method equalizing wear-level	12/27/07
KR	10-2007-0139106	Read Enable Signal Adjusting Flash Memory Device and Read Control Method of Flash Memory Device	12/27/07
US	12/127,133	Method and Apparatus for Cooling Computer Memory	05/27/08
US	12/179,715	Method for Optimizing Memory Modules for User-Specific Environments	07/25/08
KR	10-2008-0078484	Device and Method of Controlling a Flash Memory	08/11/08
US	12/207,507	Methods and Apparatus for Providing Error Correction to Unwritten Pages and for Identifying Unwritten Pages in Flash Memory	09/10/08
KR	10-2008-0112575	Controller for solid state disk of controlling access to memory bank	11/13/08

Country	App No.	Title	Filing Date (US Format)
KR	10-2008-0136866	Memory controller and method for memory management	12/30/08
KR	10-2009-0006854	Solid state disks controller of controlling simultaneously switching of pads	01/29/09
KR	10-2009-0009229	Memory device, device and method for memory management	02/05/09
KR	10-2009-0011138	Apparatus and method for programming of buffer cache in solid state disk system	02/11/09
KR	10-2009-0011781	Storage system using high speed storage device as cache	02/13/09
KR	10-2009-0023620	Apparatus and method for managing dram buffer	03/19/09
KR	10-2009-0023989	Solid state drive controller and method for operating of the solid state drive controller	03/20/09
KR	10-2009-0033479	Method managing cache/disk and controller of enabling the method	04/17/09
US	12/632,176	Memory Modules and Methods for Modifying Memory Subsystem Performance	12/07/09
KR	10-2009-0131512	Controller for detecting and correcting an error without buffer and method of enabling the controller	12/28/09
US	12/713,349	Modular Mass Storage System and Method Therefor	02/26/10
US	12/783,978	Mass Storage Device for a Computer System and Method Therefor	05/20/10
US	12/793,023	Method and Apparatus for Reducing Write Cycles in NAND-Based Flash Memory Devices	06/03/10
US	12/835,817	Method and Apparatus to Increasing File Copy Performance on Solid State Mass Storage Devices	07/14/10
US	12/859,339	Optical Memory Device and Method Therefor	08/19/10
US	12/859,595	Mass Storage Device and Method for Offline Background Scrubbing of Solid-State Memory Devices	08/19/10
US	12/862,176	NAND Flash-Based Storage Device With Built-In Test-Ahead for Failure Anticipation	08/24/10
US	12/886,771	High Performance Solid-State Drives and Methods Therefor	09/21/10

Country	App No.	Title	Filing Date (US Format)
US	12/900,596	Computer System and Processing Method of Utilizing Graphics Processing Unit with ECC and Non-ECC Memory Switching Capability	10/08/10
US	12/903,260	Modular Mass Storage Devices and Methods of Using	10/13/10
US	12/917,641	Mass Storage Device and Method of Accessing Memory Devices Thereof	11/02/10
US	12/943,192	Mass Storage Device with Solid-State Memory Components Capable of Increased Endurance	11/10/10
US	12/811,001	Flash Memory Device and Flash Memory Programming Method Equalizing Wear-Level	11/11/10
US	12/960,626	RAID Storage Systems Having Arrays of Solid-State Drives and Methods of Operation	12/06/10
KR	10-2010-0139231	Adaptive digital phy for high speed external memory interface	12/30/10
US	12/986,564	Solid State Mass Storage Device and Method for Failure Anticipation	01/07/11
US	13/027,597	Computer System with Backup Function and Method Therefor	02/15/11
US	13/088,450	Flash Memory Device and Method of Operation	04/18/11
US	13/103,270	NAND Flash Based Storage Device and Methods of Using	05/09/11
US	13/142,605	Memory Controller and Memory Management Method	06/29/11
US	13/177,839	Memory System and method for generating and transferring parity information	07/07/11
US	13/181,589	Non-volatile storage devices, methods of addressing and control logic therefor	07/13/11
US	13/128,981	Controller for Solid State Disk which controls access to Memory Bank	07/26/11
US	13/146,427	Controller for Solid State Disk, which controls Simultaneous Switching of Pads	07/27/11
US	13/147,403	Memory Device, Memory Management Device, and Memory Management Method	08/02/11
US	13/148,115	Programming Method and Device for a Buffer Cache in a Solid-State Disk System	08/05/11
US	13/205,300	PCIe Bus Extension System, Method and Interfaces Therefor	08/08/11

Country	App No.	Title	Filing Date (US Format)
US	13/211,760	Mass Storage System and Method Using Hard Disk and Solid-State Media	08/17/11
US	13/058,314	Device and Method of Controlling a Flash Memory	02/09/11
US	13/257,458	SSD Controller, and Method for Operating an SSD Controller	09/19/11
US	13/251,491	Non-Volatile Memory-Based Mass Storage Device and Methods for Writing Data Thereto	10/03/11
US	13/264,275	Cache and Disk Management Method, and a Controller Using the Method	10/13/11
US	13/280,597	Page-Buffer Management of Non-Volatile Memory-Based Mass Storage Devices	10/25/11
US	13/311,723	Mass Storage Systems and Methods Using Solid-State Storage Media	12/06/11
US	13/337,482	Methods, Storage Devices, and Systems for Promoting the Endurance of Non-Volatile Solid-State Memory Components	12/27/11
US	13/339,413	Mounting Structure and Method for Dissipating Heat from a Computer Expansion Card	12/29/11
US	13/405,350	System And Method For Increasing DDR Memory Bandwidth In DDR SDRAM Modules	02/26/12
US	13/558,830	Non-Volatile Solid State Memory-Based Mass Storage Device and Methods Thereof	07/26/12
US	13/584,867	Methods and Apparatus for Providing Acceleration of Virtual Machines in Virtual Environments	08/14/12
US	13/586,979	Mass Storage Device for a Computer System and Method Therefor	08/16/12
US	13/669,727	Integrated Storage/Processing Devices, Systems and Methods for Performing Big Data Analytics	11/06/12
US	13/678,192	NAND Flash Based Storage Device and Methods of Using	11/15/12
US	13/758,346	Apparatus, Methods and Architecture to Increase Write Performance and Endurance of Non-Volatile Solid State Memory Components	02/04/13
US	13/775,916	Graphene Based Memory Devices and Methods Therefor	02/25/13
US	61/771,432	System and Method For The efficient Polling of a Status	03/01/13

Country	App No.	Title	Filing Date (US Format)
US	61/771,440	System and Method For Limiting Inrush Current in Solid State Devices	03/14/13
US	13/866,098	Modular Mass Storage System and Method Therefor	04/19/13
EU	EP20050760508	Method of increasing DDR memory bandwidth in DDR SDRAM modules	05/01/13
US	13/901,827	Solid State Mass Storage Device and Method for Failure Anticipation	05/24/13
US	61/861,590	System and Method for Interfacing Between Storage Device and Host	08/02/13
US	13/978,276	Storage for Adaptively Determining a Processing Technique With Respect to a Host Request Based on Partition Data and Operating Method for the Storage Device	11/07/13
US	14/079,192	Cache Device for Hard Disk Drives and Methods of Operation	11/13/13
US	14/175,553	Methods for Writing Data to Non-volatile memory based mass storage devices	02/07/14
US	14/175,627	Method Of Connecting a PCIe Bus Extension System	02/07/14
US	14/195,375	System and Method for the Efficient Polling of a Status	03/03/14
US	14/195,494	System and Method for Limiting Inrush Current in Solid State Devices	03/03/14
US	14/298,492	System and method for the Efficient Processing of Read Commands in a Memory System	06/06/14
US	14/325,256	Low BER Hard Decision LDPC Decoder	07/07/14
US	14/325,244	Non-volatile Memory Controller with Error Correction (ECC) Tuning via Error Statistics Collection	07/07/14
US	14/326,642	Solid State Mass Storage Media Having Data Volumes With Different Service Levels For Different Data Types	07/09/14
US	14/451,266	SYSTEM AND METHOD FOR INTERFACING BETWEEN STORAGE DEVICE AND HOST	08/04/14
US	14/458,614	Mounting Structure and Method for Dissipating Heat from a Computer Expansion Card	08/13/14
US	14/520,413	RAID Storage Systems Having Arrays of Solid State Drives and methods of Operation	10/22/14

Country	App No.	Title	Filing Date (US Format)
US	14/550,829	Integrated Storage/Processing Devices, Systems and Methods for Performing Big Data Analytics	11/21/14
US	14/571,070	Leveraging instruction ram as a data ram extension during use of a modified harvard architecture processor	12/15/14
US	14/642,609	Power Fail Savings Modes in Solid State Drive with MLC Memory	03/09/15
US	14/657,321	Computer Storage Systems and Methods of managing Database Server Applications	03/13/15
US	14/675,457	Entropy Source for Random Number Generator	03/31/15
US	14/674,721	Multistate Serial ATA Devices and Methods of Operation Therefor	03/31/15
US	14/702,560	Dynamic Power Throttling in Solid State Drives	05/01/15
US	14/712,315	Solid State Mass Storage Device and Method for Processing Forced Unit Access Write Commands	05/14/15
US	14/751,444	Solid State Mass Storage Device and Method for Persisting Volatile Data to Non-volatile Media	06/26/15
US	14/823,784	Pool level garbage collection and wear leveling of solid state devices	08/11/15
US	14/830,923	Mounting Structure and Method for Dissipating Heat from a Computer Expansion Card	08/20/15
US	14/836,107	SSD Garbage Collection Assist when SSD is a Container of Variable Length Small Objects	08/26/15
US	14/866,087	Host-Safe Firmware Upgrade of a PCI Express Device	09/25/15
US	14/867,157	Solid State Mass Storage Devices with capacitor-Based Power Supply and methods of Operation	09/28/15
US	14/871,124	A device and method for command based timing in channels to minimize the peak power requirements of solid state drive	09/30/15
US	14/976,674	Dual Buffer Solid State Drive	12/21/15
US	14/976,793	Dual Buffer Solid State Drive	12/21/15
US	14/757,468	Solid state drive with holding file for atomic updates	12/23/15
US	14/757,470	Circuit Boards and Methods of Identification and Manufacturing Thereof	12/23/15
US	14/757,469	Power loss protection for solid state drives	12/23/15

Country	App No.	Title	Filing Date (US Format)
US	14/757,458	Data Invalidation Acceleration Through Approximation Of Valid Data Counts	12/23/15