PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3829870

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
MICRON TECHNOLOGY, INC.	12/23/2009

RECEIVING PARTY DATA

Name:	ROUND ROCK RESEARCH, LLC
Street Address:	2001 ROUTE 46
Internal Address:	WATERVIEW PLAZA, SUITE 310
City:	PARSIPPANY
State/Country:	NEW JERSEY
Postal Code:	07054

PROPERTY NUMBERS Total: 1

Property Type	Number
Patent Number:	7588677

CORRESPONDENCE DATA

Fax Number: (908)654-7866

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: (908) 518-6392
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Correspondent Name: LDLK&M
Address Line 1: 600 SOUTH AVENUE WEST
Address Line 4: WESTFIELD, NEW JERSEY 07090

ATTORNEY DOCKET NUMBER:	ROUND 3.0-075 CIP III DIV
NAME OF SUBMITTER:	MELINDA C. CORMIER
SIGNATURE:	/Melinda C. Cormier/
DATE SIGNED:	04/14/2016

Total Attachments: 5
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EXHIBIT A

CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

This Confirmatory Assignment of Patent Rights (the "Agreement") is entered into this 30th day of December, 2009 (the "Closing Date"), by and between Micron Technology, Inc., a Delaware corporation ("Assignor"), and Round Rock Research, LLC, a Delaware limited liability company ("Assignee").

WHEREAS, Assignor and Assignee are party to that certain Patent Sale and Transfer Agreement dated on or about the date hereof (as in effect from time to time, the "Patent Sale and Transfer Agreement"); capitalized terms used but not otherwise defined in this Agreement shall have the respective meaning assigned thereto in the Patent Sale and Transfer Agreement;

WHEREAS, pursuant to the Patent Sale and Transfer Agreement, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all of Assignor's (and its Subsidiaries') right, title and interest, including Patent Rights, in and to the Patents listed on Schedule A hereto (collectively, the "Assigned Patents");

WHEREAS, Assignee is now desirous of acquiring the entire and exclusive right, title and interest in and to the Assigned Patents in the United States and throughout the world; and

WHEREAS, Assignor is now willing to assign to Assignee all rights, title and interest in and to the Assigned Patents in the United States and throughout the world; and

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby assigns, transfers and conveys to Assignee, its successors, legal representatives and assigns, and Assignee hereby accepts, all of Assignor's right, title and interest in the United States and throughout the world in and to the Assigned Patents and any and all Letters Patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, continuations-in-part, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Assigned Patents and any and all Letters Patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States, including, without limitation, the right, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Assigned Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Assigned Patents are or may be registered or in which applications included among the Assigned Patents are pending, to record the title of Assignee, its successors, legal representatives and assigns, as owner of all right, title and interest in and to the Assigned Patents, and to issue to Assignee, its successors, legal representatives and assigns, all Letters Patent and any legal

equivalent thereof that may be granted in any country or countries foreign to the United States and recordations of patent rights resulting from any application included among the Assigned Patents, in accordance with the terms of this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Agreement shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Agreement.

This Agreement shall be binding on, and shall inure to the benefit of, the parties hereto and their respective successors and assigns, and may be executed in two or more counterparts, each of which shall be deemed to be an original, but all of which shall constitute one and the same agreement. Each of the parties hereto agrees to accept and be bound by facsimile signatures hereto.

Each party represents that it has taken all necessary action to authorize the execution and delivery of this Agreement.

[The remainder of this page has been intentionally left blank.]

IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be executed by their respective duly authorized officers, as of the date first written above.

ASSIGNOR:

MICRON TECHNOLOGY, INC.

By: _____
Name: Steve R. Appleton
Title: Chairman and CEO

ASSIGNEE:

ROUND ROCK RESEARCH, LLC

By: _____
Name: John Desmarais
Title: Manager

On this 23rd day of December 2009, before me appeared Steven R. Appleton, the person who signed this instrument, who acknowledged that he/she signed it as a free act on his/her own behalf or on behalf of the Assignor with authority to do so.

State of IDAHO)
) ss.
County of Ada)

JAN REECE
NOTARY PUBLIC
STATE OF IDAHO

_____

[Note that federal patent assignments must also include a cover sheet. See 37 C.F.R. 3.28]

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SCHEDULE A

(to be attached)

2000-1107.00/US	US	30-Aug-01	METHOD AND APPARATUS FOR PROVIDING CLOCK SIGNALS AT DIFFERENT LOCATIONS WITH MINIMAL CLOCK SKEW	Issued	18-May-04	6737926	09/944,237
2000-1107.01/US	US	18-May-04	METHOD AND APPARATUS FOR PROVIDING CLOCK SIGNALS AT DIFFERENT LOCATIONS WITH MINIMAL CLOCK SKEW	Issued	05-Sep-06	7102450	10/849,530
2000-1128.00/US	US	15-Apr-02	CALIBRATION OF MEMORY CIRCUITS	Issued	08-Feb-05	6853938	10/123,990
2000-1128.01/US	US	19-Oct-04	CALIBRATION OF MEMORY CIRCUITS	Issued	06-Jun-06	7058533	10/969,331
2000-1130.00/US	US	21-Jun-01	METHODS AND APPARATUS FOR ELECTRICALLY AND/OR CHEMICALLY-MECHANICALLY REMOVING CONDUCTIVE MATERIAL FROM A MICROELECTRONIC SUBSTRATE	Issued	09-Jan-07	7160176	09/888,002
2000-1181.00/US	US	30-Aug-01	MEMORY CONTROLLER HAVING PINS WITH SELECTABLE FUNCTIONALITY	Issued	06-Jun-06	7058778	09/943,320
2000-1220.00/US	US	11-Jul-01	HIGH SPEED DIGITAL SIGNAL BUFFER AND METHOD	Issued	19-Nov-02	6483347	09/904,668
2000-1220.01/US	US	15-Apr-02	HIGH SPEED DIGITAL SIGNAL BUFFER AND METHOD	Issued	25-Mar-03	6538473	10/123,336
2000-1220.03/US	US	10-Jan-03	HIGH SPEED DIGITAL SIGNAL BUFFER AND METHOD	Issued	27-Jan-04	6683475	10/340,104
2001-0004.00/US	US	10-Dec-02	FLASH MEMORY ARCHITECTURE FOR OPTIMIZING PERFORMANCE OF MEMORY HAVING MULTI-LEVEL MEMORY CELLS	Issued	22-Mar-05	6870774	10/315,323
2001-0004.01/US	US	18-Oct-04	FLASH MEMORY ARCHITECTURE FOR OPTIMIZING PERFORMANCE OF MEMORY HAVING MULTI-LEVEL MEMORY CELLS	Issued	09-May-06	7042768	10/967,868
2001-0004.02/US	US	21-Feb-06	FLASH MEMORY ARCHITECTURE FOR OPTIMIZING PERFORMANCE OF MEMORY HAVING MULTI-LEVEL MEMORY CELLS	Issued	26-Jun-07	7236407	11/358,354
2001-0007.00/US	US	30-Aug-01	FLASH MEMORY WITH DOUBLE DATA RATE SDRAM INTERFACE	Issued	27-May-03	6570791	09/943,330
2001-0010.00/US	US	12-Dec-01	METHOD AND ARCHITECTURE TO CALIBRATE READ OPERATIONS IN SYNCHRONOUS FLASH MEMORY	Issued	22-Mar-05	6870770	10/017,892
2001-0010.01/US	US	27-Feb-03	METHOD AND ARCHITECTURE TO CALIBRATE READ OPERATIONS IN SYNCHRONOUS FLASH MEMORY	Issued	11-May-04	6735122	10/375,160
2001-0010.02/US	US	27-Feb-04	METHOD AND ARCHITECTURE TO CALIBRATE READ OPERATIONS IN SYNCHRONOUS FLASH MEMORY	Issued	05-Apr-05	6865111	10/788,862
2001-0010.03/US	US	14-Jan-05	METHOD AND ARCHITECTURE TO CALIBRATE READ OPERATIONS IN SYNCHRONOUS FLASH MEMORY	Issued	13-Mar-07	7190622	11/036,402
2001-0010.04/US	US	28-Jul-06	METHOD AND ARCHITECTURE TO CALIBRATE READ OPERATIONS IN SYNCHRONOUS FLASH MEMORY	Issued	25-Sep-07	7274611	11/495,404
2001-0025.00/US	US	20-Mar-01	HIGH SPEED LATCH REGISTER	Issued	18-Feb-03	6522172	09/812,757
2001-0025.01/US	US	24-Jan-02	HIGH SPEED LATCH REGISTER	Issued	12-Nov-02	6480031	10/056,384
2001-0026.00/US	US	30-Nov-01	LOW PASS FILTERS IN DLL CIRCUITS	Issued	16-Dec-03	6664830	09/997,721
2001-0026.01/US	US	17-Oct-03	LOW PASS FILTERS IN DLL CIRCUITS	Issued	12-Jul-05	6917230	10/688,861
2001-0038.00/US	US	08-Apr-02	MULTI-CHIP MODULE AND METHODS	Issued	15-Mar-05	6867500	10/118,401
2001-0038.01/US	US	16-Feb-05	MULTI-CHIP MODULE AND METHODS	Issued	01-Aug-06	7084514	11/058,984
2001-0038.02/US	US	01-Aug-06	MULTI-CHIP MODULE AND METHODS	Issued	17-Nov-09	7619313	11/497,079
2001-0038.03/US	US	13-Nov-09	MULTI-CHIP MODULE AND METHODS	Pending			12/616,526
2001-0040.00/US	US	08-Apr-02	BOND PAD REROUTING ELEMENT, REROUTED SEMICONDUCTOR DEVICES INCLUDING THE REROUTING ELEMENT, AND ASSEMBLIES INCLUDING THE REROUTED SEMICONDUCTOR DEVICES	Issued	09-Sep-08	7423336	10/118,366