PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1 Stylesheet Version v1.2 EPAS ID: PAT3872926

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
HGST, INC.	05/12/2016

RECEIVING PARTY DATA

Name:	JPMORGAN CHASE BANK, N.A., AS COLLATERAL AGENT	
Street Address:	IL 1-1145/54/63 P.O. BOX 6026	
City:	CHICAGO	
State/Country:	ILLINOIS	
Postal Code:	60680	

PROPERTY NUMBERS Total: 7

Property Type	Number	
Application Number:	14177216	
Application Number:	14177219	
Application Number:	14803091	
Application Number:	14835642	
Application Number:	14841672	
Application Number:	14956173	
Application Number:	14967025	

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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Correspondent Name: ELAINE CARRERA, LEGAL ASSISTANT

Address Line 1: 80 PINE STREET

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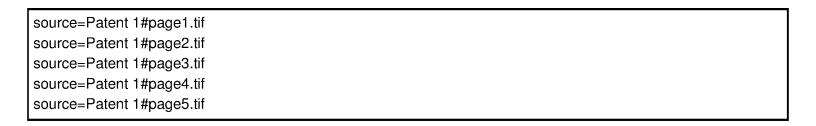
Address Line 4: NEW YORK, NEW YORK 10005

NAME OF SUBMITTER: ELAINE CARRERA

SIGNATURE: /Michael Barys/

DATE SIGNED: 05/13/2016

Total Attachments: 5



RECORDATION FORM COVER SHEET PATENTS ONLY To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below. 1. Name of conveying party(ies) 2. Name and address of receiving party(ies) HGST, Inc. Name: JPMorgan Chase Bank, N.A., as Collateral Agent Internal Address:_____ Additional name(s) of conveying party(les) attached? Yes X No 3. Nature of conveyance/Execution Date(s): Street Address: <u>IL1-:145/54/63, P.O. Box 6026</u> Execution Date(s) May 12, 2016 Assignment Merger Security Agreement City: Chicago Change of Name ___ Joint Research Agreement State: IL Government Interest Assignment Country: USA Zip: 60660 Executive Order 9424, Confirmatory License Other____ Additional name(s) & address(es) attached? Wes No This document is being filed together with a new application. 4. Application or patent number(s): A. Patent Application No.(s) B. Patent No.(s) See Schedule A See Schedule A Additional numbers attached? X Yes No 5. Name and address to whom correspondence 6. Total number of applications and patents concerning document should be mailed: involved:_7_____ Name: Elaine Carrera, Legal Assistant 7. Total fee (37 CFR 1.21(h) & 3.41) \$_____ Internal Address: Authorized to be charged to deposit account Enclosed Street Address: c/c Cahill Gordon & Reindel LLP None required (government interest not affecting title) 60 Pine Street 8. Payment Information City: New York State: NY Zip:10005 Phone Number: (212) 701-3365 Deposit Account Number _____ Docket Number: Authorized User Name Email Address: ecarrera@cahill.com 9. Signature: alla May 12, 2016 Total number of pages including cover Elaine Carrera sheet, attachments, and documents: Name of Person Signing Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to: Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

Patent Collateral Agreement

This Thursday, May 12, 2016, HGST, INC. ("Debtor"), for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, grants to JPMORGAN CHASE BANK, N.A., a national banking association (the "Agent"), acting as collateral agent hereunder for the Secured Parties as defined in the Bridge Security Agreement, dated as of May 12, 2016, among Debtor, Agent and the other debtors party thereto, as the same may be amended, restated, amended and restated or otherwise modified from time to time (the "Bridge Security Agreement") for the benefit of the Secured Parties, a lien on and security interest in, all right, title, and interest of such Debtor in and to all of the following (collectively, "Patent Collateral"):

- (i) Each patent and patent application owned by Debtor, other than to the extent the same constitutes Excluded Property, that is listed on <u>Schedule A</u> hereto (the "*Patents*"); and
- (ii) All proceeds of the foregoing, including any claim by Debtor against third parties for damages by reason of past, present or future infringement of any Patent, in each case together with the right to sue for and collect said damages.

All capitalized terms used herein without definition have the meanings given to such terms in the Bridge Security Agreement.

Debtor and Agent do hereby further acknowledge and affirm that the rights and remedies of the Agent with respect to the grant of a security interest in the Patent Collateral made hereby are more fully set forth in, and subject to, the Bridge Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Patent Collateral Agreement and the terms of the Bridge Security Agreement, the terms of the Bridge Security Agreement shall govern.

THIS PATENT COLLATERAL AGREEMENT AND THE RIGHTS AND OBLIGATIONS OF THE PARTIES HEREUNDER SHALL BE GOVERNED BY, AND CONSTRUED BY AND INTERPRETED IN ACCORDANCE WITH, THE LAW OF THE STATE OF NEW YORK.

[SIGNATURE PAGE TO FOLLOW]

IN WITNESS WHEREOF, the undersigned Debtor has caused this Patent Collateral Agreement to be duly executed as of the date and year last above written.

HGST, INC

By:

Name: Michael C. Ray

Title: Secretary

REEL: 038701 FRAME: 0019

Accepted and agreed to as of the date and year last above written.

JPMORGAN CHASE BANK, N.A., as Agent

By:

Name: Caitlin Stewart

Title: Vice President

REEL: 038701 FRAME: 0020

SCHEDULE A TO PATENT COLLATERAL AGREEMENT

U.S. PATENT APPLICATIONS

1.	MEMORY APPARATUS AND METHODS		
	THEREOF FOR PREVENTING READ ERRORS ON WEAK PAGES IN A NON-VOLATILE	14/177,216	
	MEMORY SYSTEM		
2.	SHUTDOWNS AND DATA RECOVERY TO		
	AVOID READ ERRORS WEAK PAGES IN A	14/177,219	
	NON-VOLATILE MEMORY SYSTEM		
3.	INCREMENTAL ERROR DETECTION AND	14/803091	
	CORRECTION FOR MEMOERIES		
4.	3-D PLANES MEMORY DEVICE	14/835642	
5.	4F2 SCR MEMORY DEVICE	14/841672	
6.	DEPOSITION METHOD FOR PLANAR	14/956173	
	SURFACES		
7.	METHOD FOR FORMING PCM AND RRAM 3-D MEMORY CELLS	14/967025	

RECORDED: 05/13/2016