PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3903668

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SANDISK 3D LLC	03/24/2016

RECEIVING PARTY DATA

Name:	SANDISK TECHNOLOGIES INC.
Street Address:	TWO LEGACY TOWN CENTER
Internal Address:	6900 NORTH DALLAS PARKWAY
City:	PLANO
State/Country:	TEXAS
Postal Code:	75024

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	15173104

CORRESPONDENCE DATA

Fax Number: (415)489-4150

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4154894100
Email: wgoy@vierramagen.com
Correspondent Name: DAVID E. CROMER
Address Line 1: VIERRA MAGEN MARCUS LLP
Address Line 2: 575 MARKET ST., SUITE 3750
Address Line 4: SAN FRANCISCO, CALIFORNIA 94105

ATTORNEY DOCKET NUMBER:	SAND-01678US1
NAME OF SUBMITTER:	DAVID E. CROMER
SIGNATURE:	/David E. Cromer/
DATE SIGNED:	06/03/2016

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ASSIGNMENT

WHEREAS, SanDisk 3D LLC., a limited liability company doing business at 951 SanDisk Drive, Milpitas, CA 95035 (hereinafter referred to as Assignor), holds the full and exclusive right, title and interest throughout the world in and to the patents and patent applications set forth in the attached Schedule A together with all divisions, continuations, or continuations-in-part thereof, and all patents issuing thereon including reissues, renewals, substitutions, re-examinations and extensions thereof, and any and all corresponding foreign patents and patent applications (hereinafter referred to as, collectively, THE ASSIGNED PATENT RIGHTS);

WHEREAS, SanDisk Technologies Inc., a Texas corporation, doing business at Two Legacy Town Center, 6900 North Dallas Parkway, Plano, Texas 75024, (hereinafter referred to as Assignee), is desirous of acquiring the full and exclusive right, title and interest in THE ASSIGNED PATENT RIGHTS;

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, Assignor hereby assigns, transfers and conveys unto the said Assignee, and Assignee accepts, all of Assignor's right, title and interest throughout the world in and to THE ASSIGNED PATENT RIGHTS and to all Letters Patent or applications or similar legal protection, not only in the United States and its territorial possessions, but in all countries foreign thereto to be obtained for THE ASSIGNED PATENT RIGHTS, and to any continuation, division, renewal, substitute or reissue thereof or any legal equivalent thereof in the United States or a foreign country for the full term or terms for which the same may be granted, including all priority rights under the International Convention; and Assignor hereby authorizes and requests the United States Commissioner of Patents and Trademarks and any officials of foreign countries whose duty it is to issue patents on applications as aforesaid, to issue all patents for THE ASSIGNED PATENT RIGHTS to Assignee in accordance with the terms of this ASSIGNMENT but subject to reserved rights including but not limited to those previously retained by, granted to, or owned by, the United States government, educational institutions or both and hereby transfers and conveys all rights of action, power and benefit belonging to or accruing from THE ASSIGNED PATENT RIGHTS including the right to undertake proceedings to recover past and future damages and claim all other relief in respect of any acts of infringement thereof whether such acts shall have been committed before or after the date of this assignment.

No other rights, immunities, or licenses, including, without limitation, any rights to any intellectual property owned, controlled or licensable by Assignor are granted or assigned to Assignee under this ASSIGNMENT, either expressly or by implication, estoppels, or otherwise, other than the rights expressly recited herein.

Assignor hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would knowingly conflict with this Agreement;

Assignor further covenants that Assignee will, upon its lawful request, reasonably be provided with all pertinent facts and documents relating to THE ASSIGNED PATENT RIGHTS and legal equivalents as may be known and reasonably accessible to Assignor and that Assignor will testify as to the same in any administrative contest or litigation related thereto and will promptly execute and deliver to Assignee or its legal representative any and all papers, instruments or affidavits required to

apply for, obtain, maintain, issue and enforce THE ASSIGNED PATENT RIGHTS and said equivalents in the United States or in any foreign country, which may be necessary or desirable to carry out the purposes thereof.

IN TESTIMONY WHEREOF, I hereunto set my hand as of the date indicated below:

SANDISK 3D LLC.

March 24, 2016
Date

Name: E. Earle Thompson
Title: Manager

STATE OF CALIFORNIA)
) ss.
COUNTY OF SANTA CLARA)

On March 24, 2016 before me, ***Lacra Benjamin***, *Notary Public*

Personally appeared ***E. Earle Thompson***, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Notary Public

LACRA BENJAMIN
Commission # 2078062
Notary Public - California
Santa Clara County
My Comm. Expires Aug 16, 2018

IN TESTIMONY WHEREOF, in accepting said Assignment, I hereunto set my hand as of the date indicated below:

SANDISK TECHNOLOGIES, INC.

March 24, 2016
Date

Name: E. Earle Thompson
Title: Managing Director

STATE OF CALIFORNIA)
) ss.
COUNTY OF SANTA CLARA)

On March 24, 2016 before me, ***Lacra Benjamin***, *Notary Public*

Personally appeared ***E. Earle Thompson***, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Notary Public

LACRA BENJAMIN
Commission # 2078062
Notary Public - California
Santa Clara County
My Comm. Expires Aug 16, 2018

SCHEDULE A

	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	CN	99815543.8	29-Apr-99	1339159	6-Mar-02	ZL99815543.8	18-Mar-05
2	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	EP	99921564.3	29-Apr-99	1141963	10-Oct-01		
3	Integrated Circuit Structure Including Three-Dimensional Memory Array	US	09/748,816	22-Dec-00			6,385,074	7-May-02
4	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	09/714,440	15-Nov-00		26-Feb-02	6,351,406	26-Feb-02
5	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	11/925,723	26-Oct-07	20080119027		7,816,189	19-Oct-10
6	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	12/899,634	7-Oct-10	2011-0019467	27-Jan-11	8,208,282	26-Jun-12
7	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	12/725,269	16-Mar-10	2010-0171152	8-Jul-10	7,978,492	12-Jul-11
8	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	13/526,671	19-Jun-12	2012-0250396	4-Oct-12	8,503,215	6-Aug-13
9	PILLAR-SHAPED NONVOLATILE MEMORY AND METHOD OF FABRICATION	US	13/952,990	29-Jul-13	2013-0314970	28-Nov-13	8,897,056	25-Nov-14
10	THREE-DIMENSIONAL NONVOLATILE MEMORY AND METHOD OF FABRICATION	US	14/270,409	6-May-14	2014-0239248	28-Aug-14	9,214,243	15-Dec-15
11	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	11/355,214	14-Feb-06	20060141679	29-Jun-06	7,319,053	15-Jan-08
12	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	11/354,470	14-Feb-06	20060134837	22-Jun-06	7,265,000	4-Sep-07
13	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	10/251,206	19-Sep-02	20030016553	23-Jan-03	7,160,761	9-Jan-07
14	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	09/939,498	24-Aug-01	20030206429	6-Nov-03	7,157,314	2-Jan-07
15	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	CN	200510076065.5	27-May-05	1691339	2-Nov-05		

SCHEDULE A

	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
16	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	09/939,431	24-Aug-01	20020027793	7-Mar-02	6,483,736	19-Nov-02
17	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	10/253,354	23-Sep-02	20030026121	6-Feb-03	6,780,711	24-Aug-04
18	Integrated Circuit Incorporating Three-Dimensional Memory Array with Dual Opposing Decoder Arrangement	US	10/774,818	9-Feb-04	20050105371	19-May-05	7,190,602	13-Mar-07
19	Memory Device and Method for Simultaneously Programming and/or Reading Memory Cells on Different Levels	US	10/987,091	12-Nov-04	20050063220	24-Mar-05	7,283,403	16-Oct-07
20	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	09/469,658	22-Dec-99			6,185,122	6-Feb-01
21	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	JP	2000-583042	8-Jun-01		20-Apr-05	3639786	21-Jan-05
22	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	KR	2001-7006205	16-May-01		29-Apr-04	0429083	14-Apr-04
23	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	WO	US99/09471	28-Apr-99				
24	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	SG	200102791-1	29-Apr-99			80898	30-Apr-04
25	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	TW	088108207	19-May-99	425561	11-Mar-01	NI-128709	11-Mar-01
26	Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication	US	09/192,883	16-Nov-98			6,034,882	7-Mar-00
27	Three Dimensional Memory Array and Method of Fabrication	EP	019371913	25-Apr-01	1284017	19-Feb-03		
28	Silicon Nitride Antifuse for use in Diode-Antifuse Memory Arrays	US	10/610,804	30-Jun-03	20040016991	29-Jan-04	8,575,719	5-Nov-13
29	Three Dimensional Memory Array and Method of Fabrication	US	10/689,187	20-Oct-03	20040089917	13-May-04		
30	Three Dimensional Memory Array and Method of Fabrication	US	10/805,147	19-Mar-04	20040188798	30-Sep-04	7,091,529	15-Aug-06
31	Three Dimensional Memory Array and Method of Fabrication	US	10/153,999	22-May-02	20020140051	3-Oct-02	6,653,712	25-Nov-03

SCHEDULE A

	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
32	Three Dimensional Memory Array and Method of Fabrication	MY	PI 20012022	28-Apr-01		28-Sep-07	MY-131836-A	28-Sep-07
33	Three Dimensional Memory Array and Method of Fabrication	WO	US01/13575	25-Apr-01				
34	Three Dimensional Memory Array and Method of Fabrication.	TW	090110326	22-May-01		21-Oct-02	NI-164799	21-Oct-02
35	Three Dimensional Memory Array and Method of Fabrication	US	09/814,727	21-Mar-01			6,420,215	16-Jul-02
36	Method for Programming a Three Dimensional Memory Array Incorporating Serial Chain Diode Stack	US	10/253,074	24-Sep-02	20030027378	6-Feb-03	6,754,102	22-Jun-04
37	Method for Making a Three Dimensional Memory Array Incorporating Serial Chain Diode Stack	US	10/253,076	24-Sep-02	20030031067	13-Feb-03	6,767,816	27-Jul-04
38	Three Dimensional Memory Array Incorporating Serial Chain Diode Stack	US	10/253,051	24-Sep-02	20030022420	30-Jan-03	6,784,517	31-Aug-04
39	Method for Programming a Three Dimensional Memory Array Incorporating Serial Chain Diode Stack	US	10/809,146	25-Mar-04			6,816,410	9-Nov-04
40	Three-Dimensional Memory Array Incorporating Serial Chain Diode Stack	US	09/897,705	29-Jun-01	20030053332	20-Mar-03	6,631,085	7-Oct-03
41	Nonvolatile Memory on SOI and Compound Semiconductor Substrates and Method of Fabrication	WO	US02/21318	12-Aug-02	WO 03017285	27-Feb-03		
42	Nonvolatile Memory on SOI and Compound Semiconductor Substrates and Method of Fabrication	US	09/927,642	13-Aug-01	20010055838	27-Dec-01	6,888,750	3-May-05
43	Multi-Headed Decoder Structure Utilizing Memory Arrary Line Driver with Dual Purpose Driver Device	US	10/306,887	27-Nov-02	20030214841	20-Nov-03	6,856,572	15-Feb-05
44	Three-Dimensional Memory Array and Method of Fabrication	US	09/560,626	28-Apr-00				
45	Three-Dimensional Memory Cache System	US	10/186,356	27-Jun-02	20020167829	14-Nov-02	6,711,043	23-Mar-04
46	Integrated Systems Using Vertically Stacked Three-Dimensional Memory Cells	US	10/185,588	27-Jun-02	20020163834	7-Nov-02	6,765,813	20-Jul-04
47	Modular Memory Device	US	10/342,122	13-Jan-03	20030151959	14-Aug-03	6,867,992	15-Mar-05
48	Modular Memory Device	US	11/006,465	6-Dec-04		24-Mar-05		
49	Modular Memory Device	CN	01817331.4	2-Aug-01		11-May-07	ZL01817331.4	10-Oct-07
50	Modular Memory Device	DE	019573955	2-Aug-01	1328941	23-Jul-03	1328941	22-Oct-08
51	Modular Memory Device	EP	019573955	2-Aug-01	1328941	23-Jul-03	1328941	22-Oct-08
52	Modular Memory Device	FR	019573955	2-Aug-01	1328941	23-Jul-03	1328941	22-Oct-08
53	Modular Memory Device	JP	2002-520233	2-Aug-01				
54	Modular Memory Device	MY	PI20013791	13-Aug-01			MY-119978-A	30-Aug-05
55	Modular Memory Device	NL	019573955	2-Aug-01	1328941	23-Jul-03	1328941	22-Oct-08

SCHEDULE A

	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
56	Modular Memory Device	WO	US01/24245	2-Aug-01	WO 02/15191	21-Feb-02		
57	Modular Memory Device	TW	90119760	4-Sep-01		11-May-05	I232464	11-May-05
58	Modular Memory Device	US	09/638,334	14-Aug-00			6,545,891	8-Apr-03
59	Write-Once Memory Array Controller, System and Method	US	09/638,427	14-Aug-00			6,424,581	23-Jul-02
60	Low-Cost Three-Dimensional Memory Array	US	09/928,969	13-Aug-01	20020075719	20-Jun-02	6,515,888	4-Feb-03
61	Memory Cell with Antifuse Layer Formed at Diode Junction	US	10/186,359	27-Jun-02	20030021142	30-Jan-03	6,777,773	17-Aug-04
62	Low Cost Three-Dimensional Memory Array	US	09/638,428	14-Aug-00				
63	Method for Deleting Stored Digital Data for Write-Once Memory Device	US	10/674,289	29-Sep-03	20040098416	20-May-04	7,174,351	6-Feb-07
64	Method for Deleting Stored Digital Data for Write-Once Memory Device	US	09/638,439	14-Aug-00			6,658,438	2-Dec-03
65	Multigate Semiconductor Device with Vertical Channel Current and Method of Fabrication	US	10/254,878	26-Sep-02	20030139011	24-Jul-03	6,677,204	13-Jan-04
66	Multigate Semiconductor Device with Vertical Channel Current and Method of Fabrication	MY	PI20013814	14-Aug-01				
67	Multigate Semiconductor Device with Vertical Channel Current and Method of Fabrication	WO	US01/41674	13-Aug-01		21-Feb-02		
68	Multigate Semiconductor Device with Vertical Channel Current and Method of Fabrication	TW	090119948	13-Aug-01	505998	11-Oct-02	NI-164402	21-Feb-03
69	Multigate Semiconductor Device with Vertical Channel Current and Method of Fabrication	US	09/639,577	14-Aug-00			6,580,124	17-Jun-03
70	Rail Stack Array of Charge Storage Devices and Method of Making Same	US	10/849,000	20-May-04	20040214379	28-Oct-04	6,992,349	31-Jan-06
71	Dense Arrays and Charge Storage Devices, and Methods for Making Same	CN	018031544	13-Aug-01	1401140	5-Mar-03	ZL01803154.4	26-Dec-07
72	Dense Arrays and Charge Storage Devices, and Methods for Making Same	EP	01965876.4	13-Aug-01	1312120	21-Feb-02		
73	Dense Arrays and Charge Storage Devices, and Methods for Making Same	CN	200710181784.2	13-Aug-01	2008101179079	14-May-08	ZL200710181784.2	3-Nov-10
74	Dense Arrays and Charge Storage Devices, and Methods for Making Same	DE	10011125.1	13-Aug-01	2323164	18-May-11	2323164	25-Nov-15
75	Dense Arrays and Charge Storage Devices, and Methods for Making Same	EP	10011125.1	13-Aug-01	2323164	18-May-11	2323164	25-Nov-15
76	THREE TERMINAL NONVOLATILE MEMORY DEVICE WITH VERTICAL GATED DIODE	US	12/320,351	23-Jan-09			7,825,455	2-Nov-10
77	Dense Arrays and Charge Storage Devices, and Methods for Making Same	EP	15188426.9	13-Aug-01	2988331	24-Feb-16		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
78	Dense Arrays and Charge Storage Devices	US	13/468,731	10-May-12	2012-0223380	6-Sep-12	8,981,457	17-Mar-15
79	Dense Arrays and Charge Storage Devices	US	14/227,425	27-Mar-14	2014-0217491	7-Aug-14	8,823,076	2-Sep-14
80	Dense Arrays and Charge Storage Devices	US	14/227,644	27-Mar-14	2014-0225180	14-Aug-14	8,853,765	7-Oct-14
81	Dense Arrays and Charge Storage Devices	US	14/856,131	16-Sep-15				
82	Dense Arrays and Charge Storage Devices	US	14/494,320	23-Sep-14	2015-0044833	12-Feb-15	9,171,857	27-Oct-15
83	Dense Arrays and Charge Storage Devices	US	13/027,113	14-Feb-11	2011-0156044	30-Jun-11		
84	Dense Arrays and Charge Storage Devices	US	11/544,666	10-Oct-06				
85	Dense Arrays and Charge Storage Devices, and Methods for Making Same	KR	2007-7019262	13-Aug-01			10-0821456	3-Apr-08
86	Dense Arrays and Charge Storage Devices, and Methods for Making Same	IN	IN/02/00440	13-Aug-01			239548	24-Mar-10
87	Dense Arrays and Charge Storage Devices	US	10/842,008	10-May-04	20040206996	21-Oct-04	7,129,538	31-Oct-06
88	Dense Arrays and Charge Storage Devices, and Methods for Making Same	JP	2002-520307	13-Aug-01			5792918	14-Aug-15
89	Dense Arrays and Charge Storage Devices, and Methods for Making Same	KR	2002-7004682	13-Aug-01			10-0819730	31-Mar-08
90	Monolithic Three Dimensional Array of Charge Storage Devices Containing a Planarized Surface	MY	PI20013821	14-Aug-01			MY-129228-A	30-Mar-07
91	Dense Arrays and Charge Storage Devices, and Methods for Making Same	WO	US01/25092	13-Aug-01		21-Feb-02		
92	Dense Arrays and Charge Storage Devices, and Methods for Making Same	SG	200202068-3	13-Aug-01			P-No. 88307	31-Mar-05
93	Dense Arrays and Charge Storage Devices, and Methods for Making Same	TW	90119945	13-Aug-01	540086	1-Jul-03	NI-180345	1-Jul-03
94	Monolithic Three Dimensional Array of Charge Storage Devices Containing a Planarized Surface	US	09/927,648	13-Aug-01	20020028541	7-Mar-02	6,881,994	19-Apr-05
95	TFT Mask ROM and Method for Making Same	US	11/484,757	12-Jul-06	2006-0249735A1	9-Nov-06	7,525,137	28-Apr-09
96	TFT Mask ROM and Method for Making Same	US	10/965,780	18-Oct-04	20050070060	31-Mar-05	7,250,646	31-Jul-07
97	TFT Mask ROM and Method for Making Same	US	09/983,988	26-Oct-01	20030030074	13-Feb-03	6,841,813	11-Jan-05
98	Two Mask Floating Gate EEPROM and Method of Making	US	10/849,152	20-May-04	20040207001	21-Oct-04	7,615,436	10-Nov-09
99	Two Mask Floating Gate EEPROM and Method of Making	US	10/066,376	5-Feb-02	20020142546	3-Oct-02	6,897,514	24-May-05
100	Nonvolatile Memory Cell Without a Dielectric Antifuse Having High- and Low-Impedance States	US	14/145,614	31-Dec-13	2014-0110660	24-Apr-14	9,246,089	26-Jan-16
101	Charge Trapping Memory and Method of Fabrication	US	09/639,579	14-Aug-00				
102	Two Terminal Device Using 3-D Array	US	09/639,702	14-Aug-00				
103	Three Terminal Stackable Device and Method of Fabrication	US	09/639,749	17-Aug-00				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
104	Thermal Processing for Three Dimensional Circuits	US	10/256,116	26-Sep-02	20030025176	6-Feb-03	6,770,939	3-Aug-04
105	Thermal Processing for Three-Dimensional Circuits	US	09/639,750	14-Aug-00			6,624,011	23-Sep-03
106	Memory Devices and Methods for Use Therewith	US	10/840,815	6-May-04	20040206982	21-Oct-04	7,203,084	10-Apr-07
107	Memory Devices and Methods for Use Therewith	TW	95131400	25-Aug-06		16-Feb-07	I283347	1-Jul-07
108	System and Method for Storing First and Second Files in a Memory Device	US	10/253,163	23-Sep-02	20030023821	30-Jan-03	6,697,928	24-Feb-04
109	Memory Devices and Methods for Use Therewith	TW	95131398	25-Aug-06		11-Jul-07	I283860	11-Jul-07
110	Methods for Overwriting Data in a Memory Device	US	10/253,089	23-Sep-02	20030028734	6-Feb-03	6,647,471	11-Nov-03
111	Method for overwriting data in a memory device	TW	95131397	25-Aug-06		1-Apr-07	I283858	11-Jul-07
112	Method and Data Storage Device for Writing a Minimum Number of Memory Cells in a Memory Device	US	10/253,218	23-Sep-02	20030028717	6-Feb-03	6,651,133	18-Nov-03
113	Configuring File Structures and File System Structures in a Memory Device	US	10/806,826	22-Mar-04	2004-0177229	9-Sep-04	6,925,545	2-Aug-05
114	Memory Devices and Methods for Use Therewith	TW	95131402	25-Aug-06		1-Apr-07	I283859	11-Jul-07
115	Configuring File Structures and File System Structures in a Memory Device	US	10/253,049	23-Sep-02	20030023828	30-Jan-03	6,738,883	18-May-04
116	Memory Devices and Methods for Use Therewith	MY	PI20013939	22-Aug-01			MY128904A	28-Feb-07
117	Memory Devices and Methods for Use Therewith	WO	US01/41585	6-Aug-01		21-Mar-02		
118	Memory Devices and Methods for Use Therewith	TW	090122929	14-Sep-01		21-Apr-07	I279674	21-Apr-07
119	Memory Devices and Methods for Use Therewith	US	09/748,589	22-Dec-00	20030120858	26-Jun-03		
120	Memory Devices and Methods for Use Therewith	TW	95131410	25-Aug-06		1-Apr-07	I282812	11-Jul-07
121	Methods for Identifying Memory Cells Storing Replacement Data in a Memory Device	US	10/253,048	23-Sep-02	20030023820	30-Jan-03	6,820,185	16-Nov-04
122	Memory Devices and Methods for Use Therewith	TW	95131407	25-Aug-06		1-Aug-07	I284805	1-Aug-07
123	Methods for Permanently Preventing Modification of a Partition or File	US	10/253,022	23-Sep-02	20030018871	23-Jan-03	6,694,415	17-Feb-04
124	Memory Devices & Methods for Use Therewith (Abandoned in favor of MA-012-1)	US	09/662,953	15-Sep-00				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
125	Method for Storing Digital Information First in a Re-Writable Memory and Then in a Write-Once	US	09/727,229	30-Nov-00	20020065983	30-May-02	6,584,541	24-Jun-03
126	Three-Dimensional Memory Array and Method for Storing Data Bits and ECC Bits Therein	MY	PI20015545	5-Dec-01			PA 20015545	29-Jun-07
127	Three-Dimensional Memory Array and Method for Storing Data Bits and ECC Bits Therein	WO	US01/46687	30-Nov-01		4-Jul-02		
128	Three-Dimensional Memory Array and Method for Storing Data Bits and ECC Bits Therein	TW	090130904	13-Dec-01	578159	1-Mar-04	198355	9-Jul-04
129	Three-Dimensional Memory Array and Method for Storing Data Bits and ECC Bits Therein	US	09/747,574	22-Dec-00	20020083390	27-Jun-02	6,591,394	8-Jul-03
130	Patterning Three Dimensional Structures	US	10/255,884	26-Sep-02	20030025210	6-Feb-03	7,071,565	4-Jul-06
131	Patterning Three-Dimensional Structures	US	09/746,204	22-Dec-00	20020081833	27-Jun-02	6,627,530	30-Sep-03
132	Methods of Forming Nonvolatile Memory Devices Utilizing a Hard Mask	US	09/746,469	22-Dec-00	2002-0081851	27-Jun-02	6,486,065	26-Nov-02
133	Non-Volatile Reprogrammable Semiconductor Memory in Transition Metal Crystallized Silicon	US	09/801,233	6-Mar-01				
134	Nonvolatile Reprogrammable Semiconductor Memory and Methods of Fabrication and Utilization	US	09/745,125	21-Dec-00				
135	Formation of Antifuse Structure in a Three-Dimensional Memory	US	10/114,451	1-Apr-02	2002-0106838	8-Aug-02	6,768,185	27-Jul-04
136	Formation of Antifuse Structure in a Three-Dimensional Memory	US	09/746,083	22-Dec-00	2003-0003632	2-Jan-03	6,541,312	1-Apr-03
137	Contact and Via Structure and Method of Fabrication	US	09/939,321	24-Aug-01	20020081782	27-Jun-02	6,534,403	18-Mar-03
138	Contact and Via Structure and Method of Fabrication	MY	PI20014592	1-Oct-01			MY122843-A	31-May-06
139	Contact and Via Structure and Method of Fabrication	WO	US01/29150	17-Sep-01				
140	Contact and Via Structure and Method of Fabrication	TW	090124687	5-Oct-01	583749	11-Apr-04	I199481	11-Apr-04
141	Contact and Via Structure and Method of Fabrication	US	09/746,341	22-Dec-00	20020079553	27-Jun-02	6,664,639	16-Dec-03
142	Charge Pump Circuit	US	10/002,856	15-Nov-01			6,483,728	19-Nov-02
143	Charge Pump Circuit	US	09/748,815	22-Dec-00			6,525,949	25-Feb-03
144	Partial Selection of Passive Element Memory Cell Sub-Arrays for Write Operation	US	10/310,225	5-Dec-02	20030081489	1-May-03	6,633,509	14-Oct-03

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
145	Partial Selection of Passive Element Memory Cell Sub-Arrays for Write Operation	US	09/748,649	22-Dec-00			6,661,730	9-Dec-03
146	Memory Device and Method for Reading Data Stored in a Portion of a Memory Device Unreadable by a File System of a Host Device	US	09/775,939	2-Feb-01	20020107862	8-Aug-02	6,778,974	17-Aug-04
147	Solid-State Memory Device Storing Program Code and Methods for Use Therewith	US	11/021,238	23-Dec-04	20050223243	6-Oct-05		
148	Solid-State Memory Device Storing Program Code and Methods for Use Therewith	US	09/775,745	2-Feb-01	20020108054	8-Aug-02		
149	Integrated Circuit Feature Layout for Improved Chemical Mechanical Polishing	US	10/800,078	12-Mar-04	20040173904	9-Sep-04	6,982,476	3-Jan-06
150	Integrated Circuit Feature Layout for Improved Chemical Mechanical Polishing	US	09/935,862	22-Aug-01	20020104991	8-Aug-02	6,730,931	4-May-04
151	Method of Generating Integrated Circuit Feature Layout for Improved Chemical Mechanical Polishing	US	09/775,761	2-Feb-01	20020106837	8-Aug-02	6,486,066	26-Nov-02
152	Memory Array Organization and Related Test Method Particularly Well Suited for Integrated Circuits Having Write-Once Memory Arrays	US	10/002,268	15-Nov-01			6,515,923	4-Feb-03
153	Memory Array Organization and Related Test Method Particularly Well Suited for Integrated Circuits Having a Write-Once Memory Arrays	US	60/265,810	31-Jan-01				
154	Memory Array Organization and Related Test Method Particularly Well Suited for Integrated Circuits Having Write-Once Memory Arrays	US	09/775,956	2-Feb-01			6,407,953	18-Jun-02
155	METHODS OF MAKING AND USING MEMORY CARD WITH ENHANCED TESTABILITY	US	12/019,161	24-Jan-08			7,806,324	5-Oct-10
156	Memory Card with Enhanced Testability and Methods of Making and Using the Same	US	09/788,864	20-Feb-01	20020116668	22-Aug-02	7,352,199	1-Apr-08
157	Multi-Stage Charge Pump	US	09/809,878	13-Mar-01	20020130701	19-Sep-02	6,486,728	26-Nov-02
158	Integrated Circuit Current Source with Switched Capacitor Feedback	US	09/809,884	16-Mar-01	20020130706	19-Sep-02	6,515,537	4-Feb-03
159	Method and Apparatus for Writing Memory Arrays Using External Source of High Programming Voltage	US	09/897,785	29-Jun-01			6,545,898	8-Apr-03
160	Method and Apparatus for Biasing Selected and Unselected Array Lines When Writing a Memory Array	CN	02809659.2	21-Mar-02			ZL02809659.2	4-Jul-12
161	Method and Apparatus for Biasing Selected and Unselected Array Lines When Writing a Memory Array	MY	PI 20020457	8-Feb-02	MY01229855-A	31-May-06	122955	31-May-06

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
162	Method and Apparatus for Biasing Selected and Unselected Array Lines When Writing a Memory Array	WO	US02/08675	21-Mar-02	WO 02/078003 A3	3-Oct-02		
163	Method and Apparatus for Biasing Selected and Unselected Array Lines When Writing a Memory Array	TW	91102672	18-Feb-02		1-Sep-03	186483	29-Jan-04
164	Method and Apparatus for Biasing Selected and Unselected Array Lines When Writing a Memory Array	US	09/897,771	29-Jun-01	20020136047	26-Sep-02	6,618,295	9-Sep-03
165	Method and Apparatus for Discharging Memory Array Lines	US	09/897,784	29-Jun-01			6,504,753	7-Jan-03
166	Current sensing Method and Apparatus For a Memory Array	US	12/405,160	16-Mar-09	2009-0175094	9-Jul-09	7,773,443	10-Aug-10
167	Memory Array Incorporating Noise Detection Line	US	12/847,378	30-Jul-10	2010-0290301	18-Nov-10	8,094,510	10-Jan-12
168	Current Sensing Method and Apparatus Particularly Useful for a Memory Array of Cells Having Diode-Like Characteristics	US	10/253,075	24-Sep-02	20030026120	6-Feb-03	6,937,495	30-Aug-05
169	Current sensing Method and Apparatus Particularly Useful for a Memory Array of Cells Having Diode-Like Characteristics	US	10/253,024	24-Sep-02	20030021148	30-Jan-03	7,505,344	17-Mar-09
170	Current Sensing Method and Apparatus Particularly Useful for a Memory Array of Cells Having Diode-Like Characteristics	US	09/896,468	29-Jun-01			7,177,181	13-Feb-07
171	Memory Array Incorporating Noise Detection Line	US	09/897,704	29-Jun-01			6,522,594	18-Feb-03
172	Passive Element Memory Array and Related Circuits Useful Therefor	US	60/277,815	21-Mar-01				
173	Memory Device with Row and Column Decoder Circuits Arranged in a Checkerboard Pattern Under a Plurality of Memory Arrays	US	10/440,377	16-May-03	20030202404	30-Oct-03	6,735,104	11-May-04
174	Memory Device with Row and Column Decoder Circuits Arranged in a Checkerboard Pattern Under a Plurality of Memory Arrays	MY	PI 20020963	19-Mar-02			MY126198-A	29-Sep-06
175	Memory Device with Row and Column Decoder Circuits Arranged in a Checkerboard Pattern Under a Plurality of Memory Arrays	WO	US02/08202	13-Mar-02		3-Oct-02		
176	Memory Device with Row and Column Decoder Circuits Arranged in a Checkerboard Pattern under a Plurality of Memory Array	US	60/277,794	21-Mar-01				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
177	Memory Device with Row and Column Decoder Circuits Arranged in a Checkerboard Pattern Under a Plurality of Memory Arrays	TW	091105361	20-Mar-02	559826	1-Nov-03	190553	11-Mar-04
178	Memory Device with Row and Column Decoder Circuits Arranged in a Checkerboard Pattern Under a Plurality of Memory Arrays	US	09/896,814	29-Jun-01	20020136045	26-Sep-02	6,567,287	20-May-03
179	Three Dimensional Memory Array	US	60/277,738	21-Mar-01				
180	Non-Volatile Thin Film Transistor Memory and Method of Fabrication	US	60/279,855	28-Mar-01				
181	High Voltage Transistor and Fabrication Process	US	10/247,073	18-Sep-02	20030022452	30-Jan-03	7,101,764	5-Sep-06
182	High Voltage Transistor and Fabrication Process	US	09/823,503	30-Mar-01	20030011033	16-Jan-03	6,501,139	31-Dec-02
183	Method for Field-Programming a Solid State Memory Device with a Digital Media File	US	12/228,961	15-Aug-08	2010-0005223	7-Jan-10		
184	Method for Field-Programming a Solid State Memory Device with a Digital Media File	US	09/823,489	30-Mar-01	20020144277	3-Oct-02	7,424,201	9-Sep-08
185	Method for Reading Data in a Write-Once Memory Device Using a Write-Many File System	US	09/878,138	8-Jun-01	n/a		7,062,602	13-Jun-06
186	Method for Making a Write-Once Memory Device Read Compatible with a Write-Many File System	US	10/023,468	14-Dec-01			6,895,490	17-May-05
187	Method for Reading Data in a Write-Once Memory Device Using a Write-Many File System	US	60/282,790	9-Apr-01				
188	Method for Re-Directing Data Traffic in a Write Once Memory Device	US	60/282,723	9-Apr-01				
189	Method for Re-Directing Data Traffic in a Write-Once Memory Device	US	09/877,691	8-Jun-01				
190	Method of Preventing Autodoping	US	10/624,580	21-Jul-03	20040018731	3-Feb-04		
191	Method of Preventing Autodoping	US	09/859,282	17-May-01			6,635,556	21-Oct-03
192	Memory Device and Method for Storing and Reading Data in a Write-Once Memory Array	US	09/877,720	8-Jun-01			6,996,660	7-Feb-06
193	Memory Device and Method for Storing and Reading a File System Structure in a Write-Once Memory Array	US	09/877,719	8-Jun-01			7,003,619	21-Feb-06
194	Method And System for Increasing Programming Bandwidth in a Non-Volatile Memory Device	US	09/895,960	29-Jun-01	20020136059	26-Sep-02	6,515,904	4-Feb-03

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
195	Memory Device and Method for Sensing While Programming a Non-Volatile Memory Cell	US	09/896,815	29-Jun-01	20020136076	26-Sep-02	6,574,145	3-Jun-03
196	Three-Dimensional Memory Cache System	US	60/308,330	26-Jul-01				
197	Process for Fabricating Dielectric Film Using Plasma Oxidation	US	09/918,853	30-Jul-01	20030022526	30-Jan-03	7,816,188	19-Oct-10
198	Anti-Fuse Memory Cell with Asymmetric Breakdown Voltage	US	10/027,466	20-Dec-01	20030026158	6-Feb-03	6,704,235	9-Mar-04
199	Anti-fuse Memory Cell with Asymmetric Breakdown Voltage	US	09/918,307	30-Jul-01	20030026157	6-Feb-03		
200	Vertically Stacked, Field Programmable, Nonvolatile Memory and Method of Fabrication	US	10/313,763	6-Dec-02	20030124802	3-Jul-03	6,780,683	24-Aug-04
201	Vertically Stacked, Field Programmable, Nonvolatile Memory and Method of Fabrication	US	10/848,601	17-May-04	20050026334	3-Feb-05	7,488,625	10-Feb-09
202	Vertically-Stacked, Field Programmable, Nonvolatile-Memory and Method of Fabrication	US	10/128,188	22-Apr-02	20030064572	3-Apr-03	6,689,644	10-Feb-04
203	Vertically Stacked, Field Programmable, Non-Volatile Memory and Method of Fabrication	MY	PI 20022874	31-Jul-02			MY-122896-A	31-May-06
204	Vertically-Stacked, Field Programmable, Non-Volatile Memory and Method of Fabrication	WO	US02/23748	26-Jul-02	WO 03/017427 A2	27-Feb-03		
205	Vertically Stacked, Field Programmable, Non-Volatile Memory and Method of Fabrication	TW	91117223	31-Jul-02		11-Dec-06	I268604	11-Dec-06
206	Vertically-Stacked, Field Programmable, Nonvolatile-Memory and Method of Fabrication	US	09/928,536	13-Aug-01			6,525,953	25-Feb-03
207	Low Resistivity Titanium Silicide on Heavily Doped Semiconductor	US	10/247,071	18-Sep-02	20030030147	13-Feb-03	7,144,807	5-Dec-06
208	Low Resistivity Titanium Silicide on Heavily Doped Semiconductor	US	09/928,975	13-Aug-01	20030030148	13-Feb-03	7,148,570	12-Dec-06
209	Molded Memory Module and Method of Making the Module Absent a Substrate Support	US	09/928,767	13-Aug-01	20030029920	13-Feb-03	6,843,421	18-Jan-05
210	Digital Memory Method and System for Storing Multiple-Bit Digital Data	US	09/932,701	17-Aug-01			6,490,218	3-Dec-02
211	Memory Device and Method for Selectable Sub-Array Activation	US	10/623,266	18-Jul-03	20040066671	8-Apr-04	6,894,936	17-May-05
212	Memory Device and Method for Selectable Sub-Array Activation	US	09/943,655	31-Aug-01	20030043643	6-Mar-03	6,724,665	20-Apr-04
213	Inverted Staggered Thin Film Transistor with Salicided Source/Drain Structures and Method of Making Same	US	10/270,394	15-Oct-02	20040036124	26-Feb-04	6,815,781	9-Nov-04

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
214	Thin Film Transistors with Vertically Offset Drain Reigons	US	10/617,886	14-Jul-03				
215	Thin Film Transistors with Vertically Offset Drain Reigons	US	09/961,278	25-Sep-01	20030057435	27-Mar-03	6,593,624	15-Jul-03
216	Three-Dimensional, Mask-Programmed Read Only Memory	US	10/010,643	5-Nov-01	20030086284	8-May-03	6,624,485	23-Sep-03
217	Integrated Circuit Incorporating Dual Organization Memory Array	US	09/990,901	16-Nov-01			6,889,307	3-May-05
218	Integrated Circuit Memory Array with Fast Test Mode Utilizing Multiple Word Line Selection and Method Therefor	US	09/990,894	16-Nov-01			6,768,685	27-Jul-04
219	Method for Altering a Word Stored in a Write-Once Memory Device	US	10/023,200	14-Dec-01	20030115535	19-Jun-03	6,901,549	31-May-05
220	Memory Device and Method for Redundancy/Self-Repair	US	10/024,646	14-Dec-01	20030115518	19-Jun-03	7,219,271	15-May-07
221	Memory Device and Method for Storing Bits in Non-Adjacent Storage Locations in a Memroy Array	US	10/024,647	14-Dec-01	20030115514	19-Jun-03	6,928,590	9-Aug-05
222	Memory Device and Method for Dynamic Bit Inversion	US	10/023,466	14-Dec-01			6,563,745	13-May-03
223	Method for Fabricating and Identifying Integrated Circuits and Self-Identifying Integrated Circuits	US	10/636,036	6-Aug-03	20040029357	12-Feb-04	6,947,305	20-Sep-05
224	Method for Fabricating and Identifying Integrated Circuits and Self-Identifying Integrated Circuits	US	10/068,195	4-Feb-02	20030147266	7-Aug-03	6,649,505	18-Nov-03
225	Diverse Band Gap Energy Level Semiconductor Device	US	10/254,123	25-Sep-02	20030164492	4-Sep-03	7,049,678	23-May-06
226	Diverse Band Gap Energy Level Semiconductor Device	US	10/254,129	25-Sep-02	20030164493	4-Sep-03	6,657,278	2-Dec-03
227	Diverse Band Gap Energy Level Semiconductor Device	US	10/254,172	25-Sep-02			6,686,646	3-Feb-04
228	Diverse Band Gap Energy Level Semiconductor Device	US	10/254,326	25-Sep-02	20030164494	4-Sep-03	7,199,418	3-Apr-07
229	Diverse Band Gap Energy Level Semiconductor Device	US	10/077,108	15-Feb-02	20030164491	4-Sep-03	7,038,248	2-May-06
230	Gate Dielectric Structures for Integrated Circuits and Methods for Making and Using Such Gate Dielectric Structures	US	10/079,472	19-Feb-02	20030155582	21-Aug-03		
231	Memory Module Having Interconnected and Stacked Integrated Circuits	US	11/326,074	5-Jan-06	20060118927	8-Jun-06	7,432,599	7-Oct-08
232	Memory Module Having Interconnected and Stacked Integrated Circuits	US	10/793,407	4-Mar-04	20040169285	2-Sep-04	7,005,730	28-Feb-06

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233	Memory Module Having Interconnected and Stacked Integrated Circuits	US	10/080,036	19-Feb-02	20030155659	21-Aug-03	6,731,011	4-May-04
234	Use in Semiconductor Devices of Dielectric Antifuses Grown on Silicide	US	10/727,765	3-Dec-03	20040108573	10-Jun-04		
235	Silicide-Silicon Oxide-Semiconductor Antifuse Device and Method of Making	US	11/898,622	12-Sep-07	2008-0009105	10-Jan-08	7,655,509	2-Feb-10
236	Silicide-Silicon Oxide-Semiconductor Antifuse Device and Method of Making	US	12/656,016	13-Jan-10	2010-0177549	15-Jul-10	7,915,095	29-Mar-11
237	Silicide-Silicon Oxide-Semiconductor Antifuse Device and Method of Making	US	10/986,196	12-Nov-04	20050112804	26-May-05	7,329,565	12-Feb-08
238	Silicide-Silicon Oxide-Semiconductor Antifuse Device and Method of Making	US	10/095,962	13-Mar-02	20030173643	18-Sep-03	6,853,049	8-Feb-05
239	Memory Device and Method for Reliably Reading Multi-Bit Data from a Write-Many Memory Cell	US	10/144,451	9-May-02			6,567,304	20-May-03
240	Multiple-Mode Memory and Method for Forming Same	US	10/813,455	29-Mar-04	20040184296	23-Sep-04	6,839,262	4-Jan-05
241	Multiple-Mode Memory and Method for Forming Same	WO	US03/19382	20-Jun-03	WO 2004/003929	8-Jan-04		
242	Multiple-Mode Memory and Method for Forming Same	US	10/184,578	27-Jun-02	20040001348	1-Jan-04	6,768,661	27-Jul-04
243	Three Dimensional Memory	US	10/665,697	22-Sep-03	20040062094	1-Apr-04	6,875,641	5-Apr-05
244	Three Dimensional Memory	US	10/666,971	18-Sep-03	20050099856	12-May-05	7,115,967	3-Oct-06
245	Three Dimensional Memory	US	10/185,508	27-Jun-02	20040002184	1-Jan-04	7,081,377	25-Jul-06
246	High Density 3D Rail Stack Arrays and Method of Making	US	10/779,760	18-Feb-04	20040159860	19-Aug-04	6,940,109	6-Sep-05
247	High Density 3D Rail Stack Arrays	US	10/180,046	27-Jun-02	200400000679	1-Jan-04	6,737,675	18-May-04
248	Electrically Isolated Pillars in Active Devices	US	10/681,504	7-Oct-03	20040087072	6-May-04	7,245,000	17-Jul-07
249	Electrically Isolated Pillars in Active Devices	US	10/681,507	7-Oct-03	20040071034	15-Apr-04	7,413,945	19-Aug-08
250	Electrically Isolated Pillars in Active Devices	US	10/185,507	27-Jun-02	20040002186	1-Jan-04	6,952,043	4-Oct-05
251	Same Conductivity Type Highly-Doped Regions for Antifuse Memory	US	10/185,515	27-Jun-02			6,642,603	4-Nov-03
252	Low Cost, Serially-Connected Multilevel Mask ROM	WO	US03/20051	25-Jun-03	WO 2004/003926 A2	8-Jan-04		
253	Low Cost, Serially-Connected Multilevel Mask ROM	US	10/185,208	27-Jun-02	20040001355	1-Jan-04		
254	A Dynamic Sub-Array Group Selection Scheme	US	10/217,182	12-Aug-02	20040027855	12-Feb-04	6,781,878	24-Aug-04
255	Thin Film Transistor with Metal Oxide Layer and Method of Making	US	10/270,127	15-Oct-02	20040069990	15-Apr-04	6,858,899	22-Feb-05
256	Inverted Staggered Thin Film Transistor with Etch Stop Layer and Method of Making Same	US	10/756,356	14-Jan-04	20040145005	29-Jul-04	6,825,533	30-Nov-04
257	Inverted Staggered Thin Film Transistor with Etch Stop Layer and Method of Making Same	US	10/270,309	15-Oct-02			6,710,409	23-Mar-04

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258	A Multibank Memory on a Die	US	10/305,715	27-Nov-02	20040100827	27-May-04	6,965,527	15-Nov-05
259	Tree Decoder Structure Particularly Well Suited to Interfacing array Lines Having Extremely Small Layout Pitch	US	10/306,888	27-Nov-02	20040100852	27-May-04	6,859,410	22-Feb-05
260	Integrated Circuit and Method for Selecting a Set of Memory Cell Layer Dependent or Temperature Dependent Operating Conditions	US	10/307,270	27-Nov-02	20040100831	27-May-04	6,954,394	11-Oct-05
261	Nonvolatile Memory Cell Without a Dielectric Antifuse Having High- and Low-Impedance States	US	10/955,549	29-Sep-04	20050052915	10-Mar-05	8,637,366	28-Jan-14
262	Method for Forming a Nonvolatile Memory Cell Comprising a Reduced Height Vertical Diode	US	13/228,109	8-Sep-11	2011-0318911	29-Dec-11	8,252,644	28-Aug-12
263	Nonvolatile Memory Cell Comprising a Reduced Height Vertical Diode	US	12/481,684	10-Jun-09	2010-0181657	22-Jul-10	8,018,025	13-Sep-11
264	Nonvolatile Memory Cell Comprising a Reduced Height Vertical Diode	US	11/866,403	2-Oct-07	2008-0026510	31-Jan-08	7,560,339	14-Jul-09
265	Nonvolatile Memory Cell Comprising a Reduced Height Vertical Diode	US	11/015,824	17-Dec-04	20050098800	12-May-05	7,285,464	23-Oct-07
266	A Non-Volatile Memory Cell Comprising a Dielectric Layer and a Phase Change Material in Series	WO	US06/00774	11-Jan-06	WO 06/078505	27-Jul-06		
267	A Non-Volatile Memory Cell Comprising a Dielectric Layer and a Phase Change Material in Series	US	11/040,255	19-Jan-05	20050158950	21-Jul-05		
268	Nonvolatile Memory Cell Operating by Increasing Order in Polycrystalline Semiconductor Material	CN	200680027149.2	6-Jun-06				
269	One Time Programmale Crosspoint Memory with a Diode as an Antifuse	EP	06760714.3	6-Jun-06	889294	6-Apr-07		
270	Nonvolatile Memory Cell Operating by Increasing Order in Polycrystalline Semiconductor Material	US	13/568,834	7-Aug-12	2012-0300533	29-Nov-12	8,482,973	9-Jul-13
271	Nonvolatile Memory Cell Operating by Increasing Order in Polycrystalline Semiconductor Material	US	13/925,917	25-Jun-13	2013-0286728	31-Oct-13	8,730,720	20-May-14
272	Nonvolatile Memory Cell Operating by Increasing Order in Polycrystalline Semiconductor Material	US	13/074,509	29-Mar-11	2011-0176352	21-Jul-11	8,243,509	14-Aug-12
273	Nonvolatile Memory Cell Operating by Increasing Order in Polycrystalline Semiconductor Material	JP	2008-514846	6-Jun-06	P2008/546213A	18-Dec-08		

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274	One-time Programmable Crosspoint Memory with a Diode as an Antifuse	KR	2007-7029690	6-Jun-06				
275	Nonvolatile Memory Cell Operating by Increasing Order in Polycrystalline Semiconductor Material	WO	US06/22023	6-Jun-06	WO 07/046883	26-Apr-06		
276	Nonvolatile Memory Cell Operating by Increasing Order in Polycrystalline Semiconductor Material	TW	095120206	5-Jun-06				
277	Nonvolatile Memory Cell Operating by Increasing Order in Polycrystalline Semiconductor Material	US	11/148,530	8-Jun-05	20050226067	13-Oct-05		
278	Ultrathin Chemically Grown Oxide Film as a Dopant Diffusion Barrier in Semiconductor Devices	US	11/215,951	31-Aug-05	20060006495	12-Jan-06	7,265,049	4-Sep-07
279	Method to Minimize Formation of Recess at Surface Planarized by Chemical Mechanical Planarization	US	11/237,169	28-Sep-05	20060054962	16-Mar-06	7,238,607	3-Jul-07
280	High-Density Three-Dimensional Memory Cell	US	10/855,784	26-May-04	20050012119	20-Jan-05	6,952,030	4-Oct-05
281	Method for Making High Density Nonvolatile Memory	US	10/855,775	26-May-04	20050014322	20-Jan-05	7,026,212	11-Apr-06
282	Method for Making Contacts in a High-Density Memory	US	10/855,785	26-May-04	20050012220	20-Jan-05	6,960,495	1-Nov-05
283	Method for Making High Density Nonvolatile Memory	US	10/855,880	26-May-04	20050012154	20-Jan-05	7,009,275	7-Mar-06
284	Method for Making High Density Nonvolatile Memory	US	10/855,804	26-May-04	20050014334	20-Jan-05	6,984,561	10-Jan-06
285	A High-Density Three-Dimensional Memory	US	10/855,778	26-May-04	20050012120	20-Jan-05	6,995,422	7-Feb-06
286	METHODS OF MAKING A HIGH-DENSITY NONVOLATILE MEMORY	US	13/776,193	25-Feb-13	2013-0164921	27-Jun-13	8,951,861	10-Feb-15
287	High-Density Nonvolatile Memory and Methods of Making the Same	US	13/195,518	1-Aug-11	2011-0287615	24-Nov-11	8,383,478	26-Feb-13
288	High-Density Nonvolatile Memory and Methods of Making the Same	US	12/477,216	3-Jun-09	2009-0261343	22-Oct-09	8,004,033	23-Aug-11
289	High-density nonvolatile memory	US	11/401,073	10-Apr-06	2006-0189077	24-Aug-06	7,557,405	7-Jul-09
290	An Improved Method for Making High Density Nonvolatile Memory	JP	2004-565422	12-Dec-03				
291	An Improved Method for Making High Density Nonvolatile Memory	WO	US03/39612	12-Dec-03	WO 2004061851	22-Jul-04		
292	An Improved Method for Making High Density Nonvolatile Memory	US	10/326,470	19-Dec-02				
293	Formation of Thin Channels for TFT Devices to Ensure Low Variability of Threshold Voltages	US	10/334,649	31-Dec-02	20040124415	1-Jul-04	6,960,794	1-Nov-05

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294	Method for Storing Data in a Write-Once Memory Array Using a Write-Many File System	US	10/327,680	20-Dec-02	20040123064	24-Jun-04	7,051,251	23-May-06
295	Array Containing Charge Storage and Dummy Transistors and Method of Operating the Array	US	10/325,737	23-Dec-02	20040120186	24-Jun-04	6,807,119	19-Oct-04
296	Semiconductor Device with Localized Charge Storage Dielectric and Method of Making Same	US	10/965,763	18-Oct-04	20050079675	14-Apr-05	7,132,335	7-Nov-06
297	Semiconductor Device with Localized Charge Storage Dielectric and Method of Making Same	US	10/325,951	23-Dec-02	20040119122	24-Jun-04	6,849,905	1-Feb-05
298	NAND Memory Array Incorporating Capacitance Boosting of Channel Regions in Unselected Memory Cells and Method for Operation of Same	US	11/764,793	18-Jun-07			7,433,233	7-Oct-08
299	NAND Memory Array Incorporating Capacitance Boosting of Channel Regions in Unselected Memory Cells and Method for Operation of Same	WO	US03/41848	31-Dec-03	WO 2004/061861	22-Jul-04		
300	NAND Memory Array Incorporating Capacitance Boosting of Channel Regions in Unselected Memory Cells and Method for Operation of Same	US	10/729,831	5-Dec-03	20040145024	29-Jul-04	7,233,522	19-Jun-07
301	Programmable Memory Array Structure Incorporating Series-Connected Transistor Strings and Methods for Fabrication and Operation of Same	JP	2004-565772	24-May-05	512776/2006	13-Apr-06		
302	Programmable Memory array Structure Incorporating Series-Connected Transistor Strings and Methods for Fabrication and Operation of Same	WO	US03/41446	29-Dec-03	WO 2004061863	22-Jul-04		
303	Programmable Memory Array Structure Incorporating Series-Connected Transistor Strings and Methods for Fabrication and Operation of Same	US	10/335,078	31-Dec-02	20040125629	1-Jul-04	7,505,321	17-Mar-09
304	Method for Fabricating Programmable Memory Array Structures Incorporating Series-Connected Transistor Strings	US	10/335,089	31-Dec-02	20040124466	1-Jul-04	7,005,350	28-Feb-06
305	System Architecture and Method for Three-Dimensional Memory	US	60/446,910	11-Feb-03				
306	System Architecture and Method for Three-Dimensional Memory	US	10/774,758	9-Feb-04	20040250183	9-Dec-04	7,383,476	3-Jun-08

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307	Method to Form Large Grain Size Polysilicon Films by Nuclei-Induced Solid Phase Crystallization	US	11/614,915	21-Dec-06	2007-0105305	10-May-07	7,361,578	22-Apr-08
308	Large Grain Size Polysilicon Films Formed by Nuclei-Induced Solid Phase Crystallization	US	10/767,525	29-Jan-04	20040183073	23-Sep-04	7,227,188	5-Jun-07
309	Large Grain Size Polysilicon Films Formed by Nuclei-Induced Solid Phase Crystallization	US	10/391,142	17-Mar-03			6,713,371	30-Mar-04
310	Redundant Memory Structure Using Bad Bit Pointers	US	10/961,501	8-Oct-04	20050044459	24-Feb-05	6,996,017	7-Feb-06
311	Redundant Memory Structure Using Bad Bit Pointers	JP	2006-507266	3-Aug-05				
312	Redundant Memory Structure Using Bad Bit Pointers	US	10/402,385	28-Mar-03			6,868,022	15-Mar-05
313	Redundant Memory Structure Using Bad Bit Pointers	WO	US04/08117	15-Mar-04	WO 2004/095461	19-May-05		
314	Three-Dimensional Memory Device Incorporating Segmented Bit Line Memory Array	US	11/764,789	18-Jun-07	2007-0263423	15-Nov-07	8,659,028	25-Feb-14
315	Three-Dimensional Memory Device Incorporating Segmented Array Line Memory Array	US	13/348,336	11-Jan-12	2012-0106253	3-May-12	8,637,870	28-Jan-14
316	Three-Dimensional Memory Device Incorporating Segmented Bit Line Memory Array	WO	US04/09756	31-Mar-04	WO 2004/090905	2-Jun-05		
317	Three-Dimensional Memory Device Incorporating Segmented Bit Line Memory Array	US	10/403,752	31-Mar-03	20040188714	30-Sep-04	7,233,024	19-Jun-07
318	Word Line Arrangement Having Multi-Layer Word Line Segments for Three-Dimensional Memory Array	US	11/103,185	11-Apr-05	20050180247	18-Aug-05	7,177,169	13-Feb-07
319	Word Line Arrangement Having Segmented Word Lines	US	11/103,184	11-Apr-05	20050180244	18-Aug-05	7,002,825	21-Feb-06
320	Word Line Arrangement Having Multi-Layer Word Line Segments for Three-Dimensional Memory Array	US	11/103,249	11-Apr-05	20050180248	18-Aug-05	7,106,652	12-Sep-06
321	Word Line Arrangement Having Multi-Layer Word Line Segments for Three-Dimensional Memory Array	US	10/403,844	31-Mar-03	20040190360	30-Sep-04	6,879,505	12-Apr-05
322	Manufacturing Method for Integrated Circuit Having Disturb-Free Programming of Passive Element Memory Cells	US	10/994,020	19-Nov-04	20050101088	12-May-05	7,022,572	4-Apr-06
323	Apparatus and Method for Disturb-Free Programming of Passive Element Memory Cells	US	10/994,016	19-Nov-04	20050073898	7-Apr-05	6,963,504	8-Nov-05

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324	Apparatus and Method for Disturb-Free Programming of Passive Element Memory Cells	US	10/403,488	31-Mar-03	20040190359	30-Sep-04	6,822,903	23-Nov-04
325	Rail Schottky Device and Method of Making	US	10/440,882	19-May-03	20040232509	25-Nov-04	7,511,352	31-Mar-09
326	Low Temperature, Low-Resistivity Heavily Doped P-Type Polysilicon Deposition	US	10/769,047	30-Jan-04	20040235278	25-Nov-04	7,419,701	2-Sep-08
327	Low Temperature, Low-Resistivity Heavily Doped P-Type Polysilicon Deposition	US	10/441,601	20-May-03	20040234781	25-Nov-04	6,815,077	9-Nov-04
328	Pipeline Circuit for Low Latency Memory	US	10/461,295	13-Jun-03	20040255088	16-Dec-04	7,243,203	10-Jul-07
329	Post Vertical Interconnects Formed with Silicide Etch Stop and Method of Making	US	11/849,174	31-Aug-07	2008-0029901	7-Feb-08	7,768,038	3-Aug-10
330	Post Vertical Interconnects Formed with Silicide Etch Stop and Method of Making	US	10/611,246	30-Jun-03	20040266206	30-Dec-04	7,307,012	11-Dec-07
331	Low-Density, High-Resistivity Titanium Nitride Layer for Use as a Contact for Low-Leakage Dielectric Layers and Method of Making	US	11/249,212	13-Oct-05	20060033180	16-Feb-06		
332	Low-Density, High-Resistivity Titanium Nitride Layer for use as a Contact for Low-Leakage Dielectric Layers	US	10/611,245	30-Jun-03	20040262702	30-Dec-04	6,956,278	18-Oct-05
333	Storage Layer Optimization of a Non Volatile Memory Device	US	10/668,693	23-Sep-03	20050062098	24-Mar-05	7,012,299	14-Mar-06
334	Method and System for Temperature Compensation for Memory Cells with Temperature-Dependent Behavior	US	10/676,862	30-Sep-03	20050078537	14-Apr-05	7,057,958	6-Jun-06
335	Multiple Twin Cell Non-Volatile Memory Array and Logic Block Structure and Method Therefor	US	10/675,212	30-Sep-03	20050078514	14-Apr-05	7,177,183	13-Feb-07
336	Uniform Seeding to Control Grain and Defect Density of Crystallized Silicon for Use in Sub-Micron Thin Film Transistors	US	11/615,819	22-Dec-06				
337	Method of Uniform Seeding to Control Gain and Defect Density of Crystallized Silicon for Use in Sub-Micron Thin Film Transistors	US	10/681,509	7-Oct-03	20050072976	7-Apr-05	7,195,992	27-Mar-07
338	Method for Forming a Memory Cell Comprising a Semiconductor Junction Diode Crystallized Adjacent to a Silicide	US	11/613,151	19-Dec-06	2007-0105284	19-Dec-06	7,833,843	16-Nov-10
339	Memory Cell Comprising a Semiconductor Junction Diode Crystallized Adjacent to a Silicide	US	10/954,510	29-Sep-04	20050121743	9-Jun-05	7,176,064	13-Feb-07
340	P-I-N Diode Crystallized Adjacent to a Silicide in Series with a Dielectric Antifuse and Methods of Forming The Same	CN	200780042606.X	13-Nov-07	CN101553925A	7-Oct-09	ZL200780042606.X	14-Aug-13

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341	P-I-N Diode Crystallized Adjacent to a Silicide in Series with A Dielectric Antifuse And Method Of Forming The Same	EP	07840040.5	13-Nov-07	2092562	26-Aug-09		
342	P-I-N Diode Crystallized Adjacent to a Silicide in Series with A Dielectric Antifuse And Method Of Forming The Same	JP	2009-537188	13-Nov-07	P2010-510656A	2-Apr-10		
343	P-I-N Diode Crystallized Adjacent to a Silicide in Series with A Dielectric Antifuse And Method Of Forming The Same	KR	2009-7009978	13-Nov-07				
344	P-I-N Diode Crystallized Adjacent to a Silicide in Series with A Dielectric Antifuse and Methods of Forming the Same	TW	096143253	15-Nov-07	200837897	16-Sep-08	I424535	21-Jan-14
345	P-I-N Diode Crystallized Adjacent to a Silicide in Series with A Dielectric Antifuse And Method Of Forming The Same	WO	US07/023855	13-Nov-07	WO08/060543	22-May-08		
346	Method for Making a P-I-N Diode Crystallized Adjacent to a Silicide in Series with A Dielectric Antifuse	US	12/698,253	2-Feb-10	2010-0136751	3-Jun-10	8,003,477	23-Aug-11
347	Method for Making a P-I-N Diode Crystallized Adjacent to a Silicide in Series with A Dielectric Antifuse	US	11/560,283	15-Nov-06	20070087508	19-Apr-07	7,682,920	23-Mar-10
348	P-I-N DIODE CRYSTALLIZED ADJACENT TO A SILICIDE IN SERIES WITH A DIELECTRIC MATERIAL	US	13/229,747	11-Sep-11	2012-0001296	5-Jan-12	8,330,250	11-Dec-12
349	DEVICES I NCLUDING A P-I-N DIODE DISPOSED ADJACENT A SILICIDE IN SERIES WITH A DIELECTRIC MATERIAL	US	13/705,227	5-Dec-12	2013-0119510	16-May-13	8,633,567	21-Jan-14
350	Semiconductor Device Including Junction Diode Contacting Contact-Antifuse Unit Comprising Silicide	US	10/728,230	3-Dec-03	20050121742	9-Jun-05	6,946,719	20-Sep-05
351	Optimization of Critical Dimensions and Pitch of Patterned Features in and Above a Substrate	US	13/613,956	13-Sep-12	2013-0009230	10-Jan-13	8,766,332	1-Jul-14
352	Optimization of Critical Dimensions and Pitch of Patterned Features in and Above a Substrate	US	12/136,766	10-Jun-08	2008-0310231	18-Dec-08	8,283,706	9-Oct-12
353	Optimization of Critical Dimensions and Pitch of Patterned Features in and Above a Substrate	US	10/728,437	5-Dec-03	20050121790	9-Jun-05	7,423,304	9-Sep-08
354	Photomask Features with Interior Nonprinting Window Using Alternating Phase Shifting	US	11/615,830	22-Dec-06	2007-0184360	9-Aug-07	7,635,545	22-Dec-09

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355	Photomask Features with Interior Nonprinting Window Using Alternating Phase Shifting	US	10/728,436	5-Dec-03	2005-0123837	9-Jun-05	7,172,840	6-Feb-07
356	High Density Contact to Relaxed Geometry Layers	US	10/728,451	5-Dec-03	20050127519	16-Jun-05	7,474,000	6-Jan-09
357	NAND Memory Array Incorporating Multiple Series Selection Devices and Method for Operation of Same	CN	200480040896.0	2-Dec-04	CN1906700A	31-Jan-07		
358	NAND Memory Array Incorporating Multiple Series Selection Devices and Method for Operation of Same	EP	04812730.2	2-Dec-04	1695356	30-Aug-06		
359	NAND Memory Array Incorporating Multiple Series Selection Devices and Method for Operation of Same	JP	2006-542728	2-Dec-04	2007-513455	24-May-07		
360	NAND Memory Array Incorporating Multiple Series Selection Devices and Method for Operation of Same	KR	2006-7013554	2-Dec-04				
361	NAND Memory Array Incorporating Multiple Series Selection Devices and Method for Operation of Same	WO	US04/40283	2-Dec-04	WO 05/057586	23-Jun-05		
362	NAND Memory Array Incorporating Multiple Series Selection Devices and Method for Operation of Same	US	10/729,865	5-Dec-03	20050128807	16-Jun-05		
363	NAND Memory Array Incorporating Multiple Write Pulse Programming of Individual Memory Cells and Method for Operation of Same	CN	200480041184.0	2-Dec-04	CN1910701A	7-Feb-07		
364	NAND Memory Array Incorporating Multiple Write Pulse Programming of Individual Memory Cells and Method for Operation of Same	EP	04817933.7	2-Dec-04	1695357	30-Aug-06		
365	NAND Memory Array Incorporating Multiple Write Pulse Programming of Individual Memory Cells and Method for Operation of Same	JP	2006-542737	2-Dec-04	2007-513456	24-May-07		
366	NAND Memory Array Incorporating Multiple Write Pulse Programming of Individual Memory Cells and Method for Operation of Same	KR	2006-7013555	2-Dec-04				
367	NAND Memory Array Incorporating Multiple Write Pulse Programming of Individual Memory Cells and Method for Operation of Same	WO	US04/40318	2-Dec-04	WO 05/057585	23-Jun-05		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
368	NAND Memory Array Incorporating Multiple Write Pulse Programming of Individual Memory Cells and Method for Operation of Same	US	10/729,844	5-Dec-03	20050122780	9-Jun-05	7,023,739	4-Apr-06
369	Memory Array Incorporating Mirrored NAND Strings and Non-Shared Global Bit Lines Within a Block	US	11/751,567	21-May-07	2007-0217263	20-Sep-07	7,508,714	24-Mar-09
370	Memory Array Incorporating Memory Cells Arranged in NAND Strings	US	10/729,843	5-Dec-03	20050122779	9-Jun-05	7,221,588	22-May-07
371	Selective Oxidation of Silicon in Diode, TFT, and Monolithic Three Dimensional Memory Arrays	US	11/861,694	26-Sep-07	2008-0013355	17-Jan-08	7,414,274	19-Aug-08
372	Selective Oxidation of Silicon in Diode, TFT, and Monolithic Three Dimensional Memory Arrays	US	11/237,162	28-Sep-05	20060024868	2-Feb-06	7,276,403	2-Oct-07
373	Selective Oxidation of Silicon in Diode, TFT, and Monolithic Three Dimensional Memory Arrays	US	10/742,204	18-Dec-03			6,951,780	4-Oct-05
374	Method For Patterning Photoresist Pillars Using A Photomask Having A Plurality Of Chromeless Nonprinting Phase Shifting Windows	US	11/559,620	14-Nov-06	2007-0072094A1	29-Mar-07	7,494,765	24-Feb-09
375	Photomask Features with Chromeless Nonprinting Phase Shifting Window	US	10/815,312	1-Apr-04	20050221200	6-Oct-05		
376	Nonselective Unpatterned Etchback to Expose Buried Patterned Features	US	10/883,417	30-Jun-04	2006003586	5-Jan-06	7,307,013	11-Dec-07
377	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	AU	2005277792	22-Jul-05				
378	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	CA	2,572,788	22-Jul-05				
379	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	CN	200580027871.1	22-Jul-05			ZL200580027871.1	18-May-11
380	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	DE	057735268	22-Jul-05			1782209	13-Apr-11

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381	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	EP	05773526.8	22-Jul-05			1782209	13-Apr-11
382	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	FR	057735268	22-Jul-05			1782209	13-Apr-11
383	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	GB	057735268	22-Jul-05			1782209	13-Apr-11
384	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	CN	201110064163.2	22-Jul-05	CN102163133	24-Aug-11	ZL201110064163.2	10-Jul-13
385	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	EP	09006070.8	22-Jul-05				
386	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	US	12/917,293	1-Nov-10			8,209,476	26-Jun-12
387	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	EP	09006071.6	22-Jul-05				
388	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	US	11/796,828	27-Apr-07	2007-0208907	6-Sep-07	7,861,058	28-Dec-10
389	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	US	11/796,882	27-Apr-07	2007-0208908	6-Sep-07	7,689,805	30-Mar-10
390	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	JP	2007-529862	22-Jul-05			4852548	28-Oct-11
391	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	KR	2007-7002998	22-Jul-05			10-1139224	10-Apr-12

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392	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	NL	057735268	22-Jul-05			1782209	13-Apr-11
393	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	WO	US05/26054	22-Jul-05				
394	Method and Apparatus for Using A One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	US	60/604,353	24-Aug-04				
395	Method and Apparatus for Using a One-Time or Few-Time Programmable Memory with a Host Device Designed for Erasable/Rewriteable Memory	US	10/956,463	30-Sep-04	20060047920	2-Mar-06	7,398,348	8-Jul-08
396	Large-Grain P-Doped Polysilicon Films for Use in Thin Film Transistors	US	10/936,168	8-Sep-04	20060051911	9-Mar-06	7,432,141	7-Oct-08
397	Deposited Semiconductor Structure to Minimize N-Type Dopant Diffusion and Method of Making	US	13/247,723	28-Sep-11	2012-0012808	19-Jan-12	8,314,477	20-Nov-12
398	Deposited Semiconductor Structure to Minimize N-Type Dopant Diffusion and Method of Making	US	13/679,610	16-Nov-12	2013-0313505	28-Nov-13	8,766,414	1-Jul-14
399	Deposited Semiconductor Structure to Minimize N-Type Dopant Diffusion and Method of Making	US	12/632,013	7-Dec-09	2010-00163831	1-Jul-10	8,030,740	4-Oct-11
400	Deposited Semiconductor Structure to Minimize N-Type Dopant Diffusion and Method of Making	US	12/181,317	28-Jul-08	2009-0026582	29-Jan-09	7,648,896	19-Jan-10
401	DEPOSITED SEMICONDUCTOR STRUCTURE TO MINIMIZE N-TYPE DOPANT DIFFUSION AND METHOD OF MAKING (MA-121-1WO)	CN	200680052354.4	30-Nov-06	CN101336478A	31-Dec-08	ZL200680052354.4	16-Feb-11
402	DEPOSITED SEMICONDUCTOR STRUCTURE TO MINIMIZE N-TYPE DOPANT DIFFUSION AND METHOD OF MAKING (MA-121-1WO)	EP	06838859.4	30-Nov-06	1961044	27-Aug-08		
403	DEPOSITED SEMICONDUCTOR STRUCTURE TO MINIMIZE N-TYPE DOPANT DIFFUSION AND METHOD OF MAKING (MA-121-1WO)	JP	2008-544400	30-Nov-06	P2009-518861A	7-May-09	5042233	20-Jul-12
404	DEPOSITED SEMICONDUCTOR STRUCTURE TO MINIMIZE N-TYPE DOPANT DIFFUSION AND METHOD OF MAKING (MA-121-1WO)	KR	2008-7016485	30-Nov-06				

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405	DEPOSITED SEMICONDUCTOR STRUCTURE TO MINIMIZE N-TYPE DOPANT DIFFUSION AND METHOD OF MAKING (MA-121-1TW)	TW	095146055	8-Dec-06	200739683	16-Oct-07	I331769	11-Oct-10
406	Deposited Semiconductor Structure to Minimize N-Type Dopant Diffusion and Method of Making	US	11/298,331	9-Dec-05	20060087005	27-Apr-06	7,405,465	29-Jul-08
407	DEPOSITED SEMICONDUCTOR STRUCTURE TO MINIMIZE N-TYPE DOPANT DIFFUSION AND METHOD OF MAKING (MA-121-1WO)	WO	US06/046133	30-Nov-06				
408	Junction Diode Comprising Varying Semiconductor Compositions	US	10/954,577	29-Sep-04	20060073657	6-Apr-06	7,224,013	29-May-07
409	Fuse Memory Cell Comprising a Diode, the Diode Serving as the Fuse Element	CN	200580026092.X	28-Sep-05	CN101432823	13-May-09		
410	Fuse Memory Cell Comprising a Diode, the Diode Serving as the Fuse Element	EP	05800174.4	28-Sep-05	1803129	13-Apr-06		
411	Fuse Memory Cell Comprising a Diode, the Diode Serving as the Fuse Element	JP	2007-533773	28-Sep-05				
412	Fuse Memory Cell Comprising a Diode, the Diode Serving as the Fuse Element	KR	2007-7004309	28-Sep-05				
413	Fuse Memory Cell Comprising a Diode, the Diode Serving as the Fuse Element	WO	US05/034936	28-Sep-05	WO06/039370	13-Apr-06		
414	Fuse Memory Cell Comprising a Diode, the Diode Serving as the Fuse Element	US	10/955,387	29-Sep-04	20060067117	30-Mar-06		
415	Method For Forming Doped Polysilicon Via Connecting Polysilicon Layers	US	12/897,696	4-Oct-10	2011-0021019	27-Jan-11	7,915,164	29-Mar-11
416	Method For Forming Doped Polysilicon Via Connecting Polysilicon Layers	US	12/489,214	23-Jun-09	2009-0258462	15-Oct-09	7,915,163	29-Mar-11
417	Doped Polysilicon Via Connecting Polysilicon Layers	US	10/955,710	29-Sep-04	20060071074	6-Apr-06	7,566,974	28-Jul-09
418	Method of Programming a Monolithic Three-Dimensional Memory	US	10/955,049	30-Sep-04				
419	System and Method of Controlling a Three-Dimensional Memory	US	10/955,048	30-Sep-04			7,149,119	12-Dec-06
420	A Method for Cleaning Slurry Particles from a Surface Polished by Chemical Mechanical Polishing	US	11/013,067	14-Dec-04	20060128153	15-Jun-06	7,300,876	27-Nov-07
421	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	CN	200580042742.X	29-Nov-05			ZL200580042742.X	15-Sep-10
422	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	DE	05852375.4	29-Nov-05			1825475	19-Jan-11

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423	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	EP	05852375.4	29-Nov-05			1825475	19-Jan-11
424	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	FR	05852375.4	29-Nov-05			1825475	19-Jan-11
425	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	GB	05852375.4	29-Nov-05			1825475	19-Jan-11
426	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	JP	2007-546708	29-Nov-05			5285277	7-Jun-13
427	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	KR	2007-7013751	29-Nov-05			10-1100805	23-Dec-11
428	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	NL	05852375.4	29-Nov-05			1825475	19-Jan-11
429	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	WO	US05/43074	29-Nov-05	WO 06/065523	5-Oct-06		
430	Apparatus and Method for Memory Operations Using Address-Dependent Conditions	US	11/015,440	17-Dec-04	20060133125	22-Jun-06	7,218,570	15-May-07
431	Method and Apparatus for Improving Yield in Semiconductor Devices by Guaranteeing Health of Redundancy Information	US	11/894,861	21-Aug-07	2007-0291563	20-Dec-08	7,545,689	9-Jun-09
432	Method and Apparatus for Improving Yield in Semiconductor Devices by Guaranteeing Health of Redundancy Information	US	11/024,516	28-Dec-04	2006-0140026	29-Jun-06	7,277,336	2-Oct-07
433	Dual-Mode Decoder Circuit, Integrated Circuit Memory Array Incorporating Same, and Related Methods of Operation	US	11/026,493	30-Dec-04	2006-0145193	6-Jul-06	7,298,665	20-Nov-07
434	Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	US	11/876,563	22-Oct-07	20080101149	1-May-08	7,633,829	15-Dec-09
435	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	CN	200580045171.5	16-Dec-05			ZL200580045171.5	18-May-11
436	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	DE	05854312.5	16-Dec-05	1831891	12-Sep-07	1831891	8-Jul-15

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437	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	EP	05854312.5	16-Dec-05	1831891	12-Sep-07	1831891	8-Jul-15
438	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	CN	201110073431.7	16-Dec-05	CN102201254A	28-Sep-11	ZL201110073431.7	14-Nov-12
439	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	DE	111844700	16-Dec-05	2450902	9-May-12	2450902	19-Mar-14
440	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	EP	11184470.0	16-Dec-05	2450902	9-May-12	2450902	19-Mar-14
441	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	GB	111844700	16-Dec-05	2450902	9-May-12	2450902	19-Mar-14
442	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	JP	2007-549434	16-Dec-05	527858/2008	24-Jul-08	5032336	6-Jul-12
443	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	KR	2007-7016213	16-Dec-05			10-1194353	18-Oct-12
444	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	WO	US05/045564	16-Dec-05	WO 06/073735	13-Jul-06		
445	Apparatus and Method for Hierarchical Decoding of Dense Memory Arrays Using Multiple Levels of Multiple-Headed Decoders	US	11/026,470	30-Dec-04	2006-0146639	6-Jul-06	7,286,439	23-Oct-07
446	Integrated Circuit Including Memory Array Incorporating Multiple Types of NAND String Structures	US	11/026,492	30-Dec-04	2006-0146608	6-Jul-06	7,177,191	13-Feb-07
447	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	US	13/750,917	25-Jan-13	2013-0135925	30-May-13	8,576,609	5-Nov-13
448	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	US	13/221,711	30-Aug-11	2011-0310662	22-Dec-11	8,385,141	26-Feb-13

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449	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	US	12/952,944	23-Nov-10	2011-0110149	12-May-11	8,102,698	24-Jan-12
450	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	US	11/930,620	31-Oct-07	2008-0130352	5-Jun-08	7,859,884	28-Dec-10
451	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	CN	200680006301.9	11-Jan-06	CN101189679A	28-May-08	ZL200680006301.9	10-Apr-13
452	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	EP	06717919.2	11-Jan-06	1846954	24-Oct-07		
453	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	JP	2007-552166	11-Jan-06	2008-527613	24-Jul-08	4746634	20-May-11
454	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	KR	2007-7018952	11-Jan-06			10-0987503	6-Oct-10
455	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	WO	US06/00776	11-Jan-06	WO 06/078506	27-Jul-06		
456	Structure and Method for Biasing Phase Change Memory Array for Reliable Writing	US	11/040,262	19-Jan-05	2006-0157679	20-Jul-06	7,307,268	11-Dec-07
457	Nonvolatile Phase Change Memory Cell Having a Reduced Thermal Contact Area	US	11/839,490	15-Aug-07	2007-0272913	29-Nov-07	7,351,992	1-Apr-08
458	Nonvolatile Phase Change Memory Cell Having a Reduced Thermal Contact Area	US	11/040,465	19-Jan-05	2006-157683	20-Jul-06	7,259,038	21-Aug-07
459	Write-Once Nonvolatile Phase Change Memory Array	US	11/040,256	19-Jan-05	2006-0157682	20-Jul-06	7,465,951	16-Dec-08
460	Patterning of Submicron Pillars in a Memory Array	US	12/422,072	10-Apr-09	2009-0224244	10-Sep-09	8,759,176	24-Jun-14
461	Method for Patterning Submicron Pillars	WO	US06/04195	7-Feb-06	WO 06/088689	24-Aug-06		
462	Method for Patterning Submicron Pillars	TW	095105515	17-Feb-06	200731469	16-Aug-07		
463	Method for Patterning Submicron Pillars	US	11/061,952	17-Feb-05	2006-0183282	17-Aug-06	7,517,796	14-Apr-09
464	Bottom-Gate SONOS-Type Cell Having a Silicide Gate	US	11/931,586	31-Oct-07	2008-0079063	3-Apr-08	7,838,350	23-Nov-10
465	Bottom-Gate SONOS-Type Cell Having a Silicide Gate	US	11/077,901	11-Mar-05	2006-0205124	14-Sep-06	7,303,959	4-Dec-07
466	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	US	12/363,588	30-Jan-09	2009-0142921	4-Jun-09	7,928,007	19-Apr-11
467	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	US	13/087,646	11-Apr-11	2011-0189840	4-Aug-11	8,497,204	30-Jul-13
468	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	CN	200680015585.8	21-Mar-06	CN 101189714A	28-May-08	ZL200680015585.8	28-Mar-12
469	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	US	13/938,975	10-Jul-13	2013-0295764	7-Nov-13	8,741,768	3-Jun-14

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470	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	EP	06739347.0	21-Mar-06				
471	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	CN	201210013376.7	21-Mar-06	CN102683267A	19-Sep-12	ZL201210013376.7	8-Apr-15
472	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	JP	2008-503170	21-Mar-06	2008-536300	4-Sep-08		
473	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	KR	2007-7022850	21-Mar-06	10-2008-0005494	14-Jan-08		
474	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	WO	US06/010520	21-Mar-06	WO 06/104817	23-Sep-06		
475	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	TW	095110444	24-Mar-06	200703559	16-Jan-07	I329904	1-Sep-10
476	Method for Reducing Dielectric Overetch When Making Contact to Conductive Features	US	11/089,771	25-Mar-05	20060216931	28-Sep-06	7,521,353	21-Apr-09
477	Method for Reducing Dielectric Overetch Using a Dielectric Etch Stop at a Planar Surface	EP	06739506.1	24-Mar-06	1941542	9-Jul-08		
478	Method for Reducing Dielectric Overetch Using a Dielectric Etch Stop at a Planar Surface	US	12/849,292	3-Aug-10	2010-0297834	25-Nov-10	8,008,187	30-Aug-11
479	Method for Reducing Dielectric Overetch Using a Dielectric Etch Stop at a Planar Surface	US	13/215,836	23-Aug-11	2011-0306177	15-Dec-11		
480	Method for Reducing Dielectric Overetch Using a Dielectric Etch Stop at a Planar Surface	US	11/923,687	25-Oct-07	2008-0254615	16-Oct-08	7,790,607	7-Sep-10
481	Method for Reducing Dielectric Overetch Using a Dielectric Etch Stop at a Planar Surface	JP	2008-503220	24-Mar-06				
482	MASKING OF REPEATED OVERLAY AND ALIGNMENT MARKS TO ALLOW REUSE OF PHOTOMASKS IN A VERTICAL STRUCTURE	KR	2007-7024320	24-Mar-06				
483	Method for Reducing Dielectric Overetch Using a Dielectric Etch Stop at a Planar Surface	WO	US06/10757	24-Mar-06	WO06/104877	21-Dec-06		

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484	Method for Reducing Dielectric Overetch Using a Dielectric Etch Stop at a Planar Surface	TW	095110471	24-Mar-06	200707576	16-Feb-07	I313896	21-Aug-09
485	Method for Reducing Dielectric Overetch Using a Dielectric Etch Stop at a Planar Surface	US	11/090,526	25-Mar-05	20060216937	28-Sep-06	7,422,985	9-Sep-08
486	Masking of Repeated Overlay and Alignment Marks to Allow Reuse of Photomasks in a Vertical Structure	CN	200680017181.2	31-Mar-06	CN 101198909A	11-Jun-08		
487	Masking of Repeated Overlay and Alignment Marks to Allow Reuse of Photomasks in a Vertical Structure	EP	06748959.1	31-Mar-06	1866701	19-Dec-07		
488	Masking of Repeated Overlay and Alignment Marks to Allow Reuse of Photomasks in a Vertical Structure	US	12/470,886	22-May-09	2009-0230571	17-Sep-09	7,982,273	19-Jul-11
489	Masking of Repeated Overlay and Alignment Marks to Allow Reuse of Photomasks in a Vertical Structure	JP	2008-504378	31-Mar-06	P2008-537642A	18-Sep-08		
490	Masking of Repeated Overlay and Alignment Marks to Allow Reuse of Photomasks in a Vertical Structure	KR	2007-7023188	31-Mar-06	10-2008-0005365	11-Jan-08		
491	Masking of Repeated Overlay and Alignment Marks to Allow Reuse of Photomasks in a Vertical Structure	WO	US06/011715	31-Mar-06	WO/ 06/105326	5-Oct-06		
492	Overlay and Alignmnet Marks for Reusing Photomasks in a Monolithic Vertical Structure and Method Thereof	TW	095111700	31-Mar-06	200705135	1-Feb-07	I302643	1-Nov-08
493	Masking of Repeated Overlay and Alignment Marks to Allow Reuse of Photomasks in a Vertical Structure	US	11/097,496	31-Mar-05	2006-0222962	5-Oct-06	7,553,611	30-Jun-09
494	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	CN	200680010766.1	31-Mar-06	CN101167139A	23-Apr-08	ZL200680010766.1	8-Sep-10
495	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	DE	067697912	31-Mar-06	1864291	12-Dec-07	1864291	13-Jun-12
496	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	EP	06769791.2	31-Mar-06	1864291	12-Dec-07	1864291	13-Jun-12
497	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	FR	067697912	31-Mar-06	1864291	12-Dec-07	1864291	13-Jun-12
498	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	GB	067697912	31-Mar-06	1864291	12-Dec-07	1864291	13-Jun-12
499	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	JP	504454/2008	31-Mar-06	535142/2008	28-Aug-08	5015135	15-Jun-12
500	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	KR	2007-7022445	31-Mar-06			10-1253217	4-Apr-13

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501	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	NL	067697912	31-Mar-06	1864291	12-Dec-07	1864291	13-Jun-12
502	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	WO	US06/012107	31-Mar-06	WO 06/121529	16-Nov-06		
503	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	TW	095111306	30-Mar-06	200709215	1-Mar-07	I326880	1-Jul-10
504	Method and Apparatus for Incorporating Block Redundancy in a Memory Array	US	11/095,907	31-Mar-05	20060221728	5-Oct-06	7,142,471	28-Nov-06
505	Decoding Circuit for Non-Binary Groups of Memory Line Drivers	CN	200680009988.1	14-Feb-06			ZL200680009988.1	19-May-10
506	Decoding Circuit for Non-Binary Groups of Memory Line Drivers	EP	06720714.2	14-Feb-06				
507	Decoding Circuit for Non-Binary Groups of Memory Line Drivers	JP	2008-504039	14-Feb-06			4939528	2-Mar-12
508	Decoding Circuit for Non-Binary Groups of Memory Line Drivers	KR	2007-7021573	14-Feb-06			10-1204021	16-Nov-12
509	Decoding Circuit for Non-Binary Groups of Memory Line Drivers	WO	US06/05067	14-Feb-06	WO06/107409	12-Oct-06		
510	Decoding Circuit for Non-Binary Groups of Memory Line Drivers	US	11/146,952	7-Jun-05	20060221702	5-Oct-06	7,272,052	18-Sep-07
511	Transistor Layout Configuration for Tight-Pitched Memory Array Lines	US	11/420,787	29-May-06	20060221758	5-Oct-06	7,177,227	13-Feb-07
512	Transistor Layout Configuration for Tight-Pitched Memory Array Lines	CN	200680009938.3	31-Mar-06	CN101151512A	26-Mar-08	ZL200680009938.3	11-Jul-12
513	Transistor Layout Configuration for Tight-Pitched Memory Array Lines	EP	06740254.5	31-Mar-06	1864094	12-Dec-07		
514	Transistor Layout Configuration for Tight-Pitched Memory Array Lines	JP	2008-504441	31-Mar-06	535267/2008	28-Aug-08		
515	Transistor Layout Configuration for Tight-Pitched Memory Array Lines	KR	2007-7022453	31-Mar-06				
516	Transistor Layout Configuration for Tight-Pitched Memory Array Lines	WO	US06/012039	31-Mar-06	WO0610543	5-Oct-06		
517	Transistor Layout Configuration for Tight-Pitched Memory Array Lines	TW	095111308	30-Mar-06	200705456	1-Feb-07	I326882	1-Jul-10
518	Transistor Layout Configuration for Tight-Pitched Memory Array Lines	US	11/095,905	31-Mar-05			7,054,219	30-May-06
519	Integrated Circuit Memory Array Configuration Including Decoding Compatibility with Partial Implementation of Multiple Memory Layers	US	12/102,801	14-Apr-08	2008-0192524	14-Aug-08	7,697,366	13-Apr-10
520	INTEGRATED CIRCUITS AND METHODS FOR USE IN AN INTEGRATED CIRCUIT MEMORY ARRAY	CN	200680010795.8	31-Mar-06	CN101164118A	16-Apr-08	ZL200680010795.8	6-Apr-11

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521	Integrated Circuit Memory Array Configuration Including Decoding Compatibility with Partial Implementation of Multiple Memory Layers	DE	06749086.2	31-Mar-06	1938331	2-Jul-08	1938331	3-Jul-13
522	Integrated Circuit Memory Array Configuration Including Decoding Compatibility with Partial Implementation of Multiple Memory Layers	EP	06749086.2	31-Mar-06	1938331	2-Jul-08	1938331	3-Jul-13
523	Integrated Circuit Memory Array Configuration Including Decoding Compatibility with Partial Implementation of Multiple Memory Layers	GB	06749086.2	31-Mar-06	1938331	2-Jul-08	1938331	3-Jul-13
524	Integrated Circuit Memory Array Configuration Including Decoding Compatibility with Partial Implementation of Multiple Memory Layers	JP	2008-504453	31-Mar-06	535269/2008	28-Aug-08	5344908	23-Aug-13
525	Integrated Circuit Memory Array Configuration Including Decoding Compatibility with Partial Implementation of Multiple Memory Layers	KR	2007-7022461	31-Mar-06			10-1287396	12-Jul-13
526	Integrated Circuit Memory Array Configuration Including Decoding Compatibility with Partial Implementation of Multiple Memory Layers	WO	US06/012106	31-Mar-06	WO06/105433	5-Oct-06		
527	Integrated Circuit Memory Array Configuration Including Decoding Compatibility with Partial Implementation of Multiple Memory Layers	TW	095111304	30-Mar-06	200707457	16-Feb-07	I326883	1-Jul-10
528	Integrated Circuit Memory Array Configuration Including Decoding Compatibility with Partial Implementation of Multiple Memory Layers	US	11/095,415	31-Mar-05	20060221752	5-Oct-06	7,359,279	15-Apr-08
529	Apparatus for Adaptive Trip Point Detection	US	11/752,807	23-May-07			7,863,950	4-Jan-11
530	Methods for Adaptive Trip Point Detection	US	11/752,819	23-May-07			7,863,951	4-Jan-11
531	Apparatus and Methods for Adaptive Trip Point Detection	CN	200680011696.1	31-Mar-06			ZL200680011696.1	8-Dec-10
532	Apparatus and Methods for Adaptive Trip Point Detection	EP	06740364.2	31-Mar-06	1869768	26-Oct-06		
533	Apparatus and Methods for Adaptive Trip Point Detection	CN	201010221360.6	31-Mar-06			ZL201010221360.6	2-Jan-13
534	Apparatus and Methods for Adaptive Trip Point Detection	JP	2008-506505	31-Mar-06				
535	Apparatus and Methods for Adaptive Trip Point Detection	KR	2007-7023417	31-Mar-06				

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536	Apparatus and Methods for Adaptive Trip Point Detection	TW	095113525	14-Apr-06			I329989	1-Sep-10
537	Apparatus and Methods for Adaptive Trip Point Detection	US	11/106,288	14-Apr-05			7,236,023	26-Jun-07
538	Apparatus and Methods for Adaptive Trip Point Detection	WO	US06/012248	31-Mar-06				
539	Method and Apparatus for Dynamically Reconfiguring a Charge Pump During Output Transients	WO	US06/011783	9-May-06				
540	Method and Apparatus for Dynamically Reconfiguring a Charge Pump During Output Transients	TW	095113650	17-Apr-06	095113650	16-Jan-07		
541	Method and Apparatus for Dynamically Reconfiguring a Charge Pump During Output Transients	US	11/125,000	9-May-05				
542	High-Density Nonvolatile Memory Array Fabricated at Low Temperature Comprising Semiconductor Diodes	CN	200680022945.7	5-May-06	CN 101297402A	29-Oct-08	ZL200680022945.7	19-May-10
543	High-Density Nonvolatile Memory Array Fabricated at Low Temperature Comprising Semiconductor Diodes	EP	06770054.2	5-May-06	EP1883963	16-Nov-06		
544	High-Density Nonvolatile Memory Array Fabricated at Low Temperature Comprising Semiconductor Diodes	KR	2012-7017783	5-May-06				
545	High-Density Nonvolatile Memory Array Fabricated at Low Temperature Comprising Semiconductor Diodes	JP	2008-511205	5-May-06	P2008-544481A	4-Dec-08	5139269	22-Nov-12
546	High-Density Nonvolatile Memory Array Fabricated at Low Temperature Comprising Semiconductor Diodes	KR	2007-7027839	5-May-06	10-2008-0022085	10-Mar-08	10-1287015	11-Jul-13
547	High-Density Nonvolatile Memory Array Fabricated at Low Temperature Comprising Semiconductor Diodes	US	11/125,606	9-May-05	2006-0249753	9-Nov-06		
548	High-Density Nonvolatile Memory Array Fabricated at Low Temperature Comprising Semiconductor Diodes	WO	US06/17525	5-May-06	WO 06/121924	1-Mar-07		
549	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	CN	200680020806.0	5-May-06			ZL200680020806.0	29-Feb-12
550	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	DE	067591370	5-May-06	1880389	23-Jan-08	1880389	21-Sep-11
551	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	EP	06759137.0	5-May-06	1880389	23-Jan-08	1880389	21-Sep-11
552	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	FR	067591370	5-May-06	1880389	23-Jan-08	1880389	21-Sep-11

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553	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	GB	067591370	5-May-06	1880389	23-Jan-08	1880389	21-Sep-11
554	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	CN	201110447977.4	5-May-06	CN102592666	18-Jul-12		
555	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	EP	10009111.5	5-May-06	2256747	1-Dec-10		
556	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	US	14/183,797	19-Feb-14	2014-0166968	19-Jun-14		
557	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	EP	10009110.7	5-May-06	2256746	1-Dec-10		
558	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	EP	10009109.9	5-May-06	2256745	1-Dec-10		
559	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	US	13/734,536	4-Jan-13	2013-0121061	16-May-13	8,687,410	1-Apr-14
560	Nonvolatile Memory Cells, monolithic Three Dimensional Memory Arrays And Method For Programming Such Memory Arrays	TW	099141295	30-Mar-07	201142844	1-Dec-11	I462099	21-Nov-14
561	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	US	12/855,462	12-Aug-10	2010-0302836	2-Dec-10	8,349,664	8-Jan-13
562	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	EP	10009108.1	5-May-06	2256744	1-Dec-10		
563	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	JP	2008-511196	5-May-06	P2008-541452A	20-Nov-08		
564	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	KR	2007-7027841	5-May-06			10-1335383	26-Nov-13
565	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	NL	067591370	5-May-06	1880389	23-Jan-08	1880389	21-Sep-11
566	Nonvolatile Memory Cells, monolithic Three Dimensional Memory Arrays And Method For Programming Such Memory Arrays	TW	096111498	30-Mar-07	200805376	16-Jan-08	I345783	21-Jul-11
567	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	US	11/395,995	31-Mar-06	2006-0250837	9-Nov-06	7,812,404	12-Oct-10
568	Nonvolatile Memory Cell Comprising a Diode and a Resistance-Switching Material	WO	US06/17376	5-May-06	WO 06/121837	4-Jan-07		
569	Rewriteable Memory Cell Comprising a Diode and a Resistance-Switching Material	US	11/125,939	9-May-05	2006-0250836	9-Nov-06		
570	TFT Charge Storage Memory Cell Having High-Mobility Corrugated Channel	CN	200680027101.1	1-Jun-06	CN101228619A	23-Jul-08	ZL200680027101.1	3-Nov-10
571	TFT Charge Storage Memory Cell Having High-Mobility Corrugated Channel	EP	06760637.6	1-Jun-06	1894231	5-Mar-08		
572	Method of Making a TFT Charge Storage Memory Cell Having High-Mobility Corrugated Channel	US	13/351,456	17-Jan-12	2012-0115289	10-May-12	8,946,017	3-Feb-15

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573	TFT Charge Storage Memory Cell Having High-Mobility Corrugated Channel	JP	2008-514877	1-Jun-06	P2008-546205A	18-Dec-08		
574	TFT Charge Storage Memory Cell Having High-Mobility Corrugated Channel	KR	2007-7028223	1-Jun-06				
575	TFT Charge Storage Memory Cell Having High-Mobility Corrugated Channel	US	11/143,355	1-Jun-05	2006-0273404	7-Dec-06	8,110,863	7-Feb-12
576	TFT Charge Storage Memory Cell Having High-Mobility Corrugated Channel	WO	US06/21373	1-Jun-06	WO 06/130801	7-Dec-06		
577	Rewriteable Memory Cell Comprising a Transistor and Resistance-Switching Material in Series	WO	US06/21372	1-Jun-06	WO 06/130800	7-Dec-06		
578	Rewriteable Memory Cell Comprising a Transistor and Resistance-Switching Material in Series	TW	095119722	2-Jun-06	200711047	16-Mar-07		
579	Rewriteable Memory Cell Comprising a Transistor and Resistance-Switching Material in Series	US	11/143,269	2-Jun-05	2006-0273298	7-Dec-06		
580	Floating Body Memory Cell System and Method of Manufacture	US	12/888,020	22-Sep-10	2011-0007541	13-Jan-11	9,111,800	18-Aug-15
581	Floating Body Memory Cell System and Method of Manufacture	US	11/923,713	25-Oct-07	2009-0116270	7-May-09	7,830,722	9-Nov-10
582	Floating Body Memory Cell System and Method of Manufacture	WO	US06/23707	19-Jun-06	WO 07/001942	4-Jan-07		
583	Floating Body Memory Cell System and Method of Manufacture	TW	095122125	20-Jun-06				
584	Floating Body Memory Cell System and Method of Manufacture	US	11/157,293	20-Jun-05	2006-0285422	21-Dec-06	7,764,549	27-Jul-10
585	Volatile Memory Cell Two-Pass Writing Method	WO	US06/23931	19-Jun-06	WO 07/002054	4-Jan-07		
586	Volatile Memory Cell Two-Pass Writing Method	TW	095122129	20-Jun-06	200802404	1-Jan-08	I408694	11-Sep-13
587	Volatile Memory Cell Two-Pass Writing Method	US	11/157,317	20-Jun-05	2006-0285423	21-Dec-06	7,317,641	8-Jan-08
588	Method and Apparatus for Programming a Memory Array	CN	200680019980.3	13-Jun-06			ZL200680019980.3	15-Oct-14
589	Method and Apparatus for Programming a Memory Array	EP	06773121.6	13-Jun-06				
590	Method and Apparatus for Programming a Memory Array	JP	2008-518227	13-Jun-06				
591	Method and Apparatus for Programming a Memory Array	KR	2007-7028379	13-Jun-06				
592	Method and Apparatus for Programming a Memory Array	WO	US06/023107	13-Jun-06	WO 07/001852	4-Jan-07		

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593	Method and Apparatus for Programming a Memory Array	TW	095122300	21-Jun-07				
594	Method and Apparatus for Programming a Memory Array	US	11/158,396	22-Jun-05		28-Dec-06	7,212,454	1-May-07
595	Method of Depositing Germanium Films	CN	200680030684.3	22-Jun-06	CN101248209A	20-Aug-08		
596	Method of Depositing Germanium Films	EP	06773983.9	22-Jun-06	1893783	5-Mar-08		
597	Method of Depositing Germanium Films	JP	2008-518493	22-Jun-06	P2008-544556A	4-Dec-08		
598	Method of Depositing Germanium Films	KR	2008-7000112	22-Jun-06				
599	Method of Depositing Germanium Films	WO	US06/24768	22-Jun-06	WO 07/002569	4-Jan-07		
600	Method of Depositing Germanium Films	US	11/159,031	22-Jun-05	2006-0292301	28-Dec-06	7,678,420	16-Mar-10
601	Reverse-Bias Method for Writing Memory Cells in a Memory Array	US	11/174,234	1-Jul-05	2007-0002610	4-Jan-07	7,304,888	4-Dec-07
602	Memory Cell with High-K Antifuse for Reverse Bias Programming	CN	200680032247.5	19-Jun-06	CN101258558A	3-Sep-08		
603	Memory Cell with High-K Antifuse for Reverse Bias Programming	DE	06785167.5	19-Jun-06	1899978	19-Mar-08	1899978	1-Dec-10
604	Memory Cell with High-K Antifuse for Reverse Bias Programming	EP	06785167.5	19-Jun-06	1899978	19-Mar-08	1899978	1-Dec-10
605	Memory Cell with High-K Antifuse for Reverse Bias Programming	FR	06785167.5	19-Jun-06	1899978	19-Mar-08	1899978	1-Dec-10
606	Memory Cell with High-K Antifuse for Reverse Bias Programming	GB	06785167.5	19-Jun-06	1899978	19-Mar-08	1899978	1-Dec-10
607	Memory Cell with High-K Antifuse for Reverse Bias Programming	JP	2008-519385	19-Jun-06	P2008-545276A	11-Dec-08		
608	Memory Cell with High-K Antifuse for Reverse Bias Programming	KR	2008-7001653	19-Jun-06			10-1226172	18-Jan-13
609	Memory Cell with High-K Antifuse for Reverse Bias Programming	NL	06785167.5	19-Jun-06	1899978	19-Mar-08	1899978	1-Dec-10
610	Memory Cell with High-K Antifuse for Reverse Bias Programming	WO	US06/023936	19-Jun-06				
611	Memory Cell with High-K Antifuse for Reverse Bias Programming	TW	095124029	30-Jun-06				
612	Memory Cell with High-K Antifuse for Reverse Bias Programming	US	11/174,240	1-Jul-05			7,453,755	18-Nov-08
613	Memory with High Dielectric Constant Antifuses Adapted for Use at Low Voltage	US	12/367,214	6-Feb-09	2009-0140299	4-Jun-09	7,781,805	24-Aug-10
614	Memory with High Dielectric Constant Antifuses Adapted for Use at Low Voltage	US	12/836,320	14-Jul-10	2010-0276660	4-Nov-10	8,350,299	8-Jan-13
615	RESISTANCE-SWITCHING MEMORY CELLS ADAPTED FOR USE AT LOW VOLTAGE	US	13/734,517	4-Jan-13	2013-0119338	16-May-13	8,686,476	1-Apr-14
616	RESISTANCE-SWITCHING MEMORY CELLS ADAPTED FOR USE AT LOW VOLTAGE	US	14/180,818	14-Feb-14	2014-0158974	12-Jun-14	9,006,795	14-Apr-15

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617	Methods Involving Memory With High Dielectric Constant Antifuses Adapted For Use At Low Voltage	US	13/678,894	16-Nov-12	2013-0314971	28-Nov-13		
618	Methods Involving Memory With High Dielectric Constant Antifuses Adapted For Use At Low Voltage	US	12/367,258	6-Feb-09	2009-0141535	4-Jun-09	8,314,023	20-Nov-12
619	Memory with High Dielectric Constant Antifuses and Method for Using at Low Voltage	US	11/173,973	1-Jul-05	20070069241	29-Mar-07		
620	Integrated Circuit Embodying a Non-Volatile Memory Cell	WO	US06/23705	19-Jun-06	WO 07/008344	18-Jan-07		
621	Integrated Circuit Embodying a Non-Volatile Memory Cell	TW	095122534	22-Jun-06				
622	Integrated Circuit Embodying a Non-Volatile Memory Cell	US	11/175,688	6-Jul-05	2007-0007577	11-Jan-07		
623	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	CN	200680029924.8	11-Jul-06	CN101258600A	3-Sep-08	ZL200680029924.8	30-Mar-11
624	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	DE	06774623.0	11-Jul-06	1908110	9-Apr-08	1908110	29-Dec-10
625	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	EP	06774623.0	11-Jul-06	1908110	9-Apr-08	1908110	29-Dec-10
626	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	FR	06774623.0	11-Jul-06	1908110	9-Apr-08	1908110	29-Dec-10
627	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	GB	06774623.0	11-Jul-06	1908110	9-Apr-08	1908110	29-Dec-10
628	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	JP	2008-521531	11-Jul-06			5122451	2-Nov-12
629	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	KR	2008-7003254	11-Jul-06			10-1230874	1-Feb-13
630	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	NL	06774623.0	11-Jul-06	1908110	9-Apr-08	1908110	29-Dec-10
631	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	WO	US06/026897	11-Jul-06	WO 07/008902	18-Jan-07		
632	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	TW	095125294	11-Jul-06		11-Nov-09	I317128	11-Nov-09
633	Nonvolatile Memory Cell Comprising Switchable Resistor and Transistor	US	11/179,122	11-Jul-05	2007-0008773	11-Jan-07	7,426,128	16-Sep-08
634	Memory Cell Comprising A Thin Film Three-Terminal Switching Device Having a Metal Source and/or Drain Region	WO	US06/26898	11-Jul-06	WO 07/008903	18-Jan-07		
635	Memory Cell Comprising A Thin Film Three-Terminal Switching Device Having a Metal Source and/or Drain Region	TW	095125293	11-Jul-06	200711102	16-Mar-07	I326915	1-Jul-10

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636	Memory Cell Comprising A Thin Film Three-Terminal Switching Device Having a Metal Source and/or Drain Region	US	11/179,095	11-Jul-05	2007-0007579	11-Jan-07		
637	Apparatus and Method for Reading an Array of Nonvolatile Memory Cells Including Switchable Resistor Memory Elements	WO	US06/026579	10-Jul-06	WO 07/008699	18-Jan-07		
638	Apparatus and Method for Reading an Array of Nonvolatile Memory Cells Including Switchable Resistor Memory Elements	TW	095125287	11-Jul-06	200710678	16-Mar-07		
639	Apparatus and Method for Reading an Array of Nonvolatile Memory Cells Including Switchable Resistor Memory Elements	US	11/179,123	11-Jul-05	2007-0008786	11-Jan-07	7,345,907	18-Mar-08
640	Apparatus and Method For Programming an Array of Nonvolatile Memory Cells Including Switchable Resistor Memory Elements	WO	US06/026581	10-Jul-06	WO 07/008701	18-Jan-07		
641	Apparatus and Method For Programming an Array of Nonvolatile Memory Cells Including Switchable Resistor Memory Elements	TW	095125337	11-Jul-06	200713276	1-Apr-07		
642	Apparatus and Method For Programming an Array of Nonvolatile Memory Cells Including Switchable Resistor Memory Elements	US	11/179,077	11-Jul-05	2007-0008785	11-Jan-07	7,362,604	22-Apr-08
643	Method of Plasma Etching Transition Metal Oxides	CN	200880006814.9	29-Feb-08	CN101657567A	24-Feb-10		
644	Method of Plasma Etching Transition Metal Oxides	EP	08726277.0	29-Feb-08	2115187			
645	Method of Plasma Etching Transition Metal Oxides	JP	2009-551738	29-Feb-08	P2010-521062A	17-Jun-10	5042319	3-Oct-12
646	Method of Plasma Etching Transition Metal Oxides	KR	2009-7018135	29-Feb-08				
647	Method of Plasma Etching Transition Metal Oxides	TW	097107254	29-Feb-08	200842976	1-Nov-08	I445077	11-Jul-14
648	Method of Plasma Etching Transition Metal Oxides	WO	US08/002706	29-Feb-08				
649	Method of Plasma Etching Transition Metals and Their Compounds	TW	095125311	11-Jul-06	200804623	16-Jan-08		
650	Method of Plasma Etching Transition Metals and Their Compounds	US	11/179,423	11-Jul-05	2007-0010100	11-Jan-07		
651	Method of Plasma Etching Transition Metals and Their Compounds	WO	US06/026896	11-Jul-06				
652	Three-Dimensional Nonvolatile SRAM Incorporating Thin-Film Device Layer	US	11/179,360	11-Jul-05	2007-0008776	11-Jan-07	7,280,397	9-Oct-07
653	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	CN	200680035454.6	27-Sep-06	CN101288169A	15-Oct-08	ZL200680035454.6	11-Apr-12

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654	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	DE	06815745.2	27-Sep-06	1929525		1929525	22-Dec-10
655	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	EP	06815745.2	27-Sep-06	1929525		1929525	22-Dec-10
656	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	FR	06815745.2	27-Sep-06	1929525		1929525	22-Dec-10
657	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	GB	06815745.2	27-Sep-06	1929525		1929525	22-Dec-10
658	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	JP	2008-533629	27-Sep-06	P2009-510664A	12-Mar-09		
659	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	KR	2008-7007845	27-Sep-06			10-1256967	16-Apr-13
660	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	NL	06815745.2	27-Sep-06	1929525		1929525	22-Dec-10
661	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	TW	095135852	27-Sep-06		21-Apr-09	I309081	21-Apr-09
662	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	US	11/496,986	31-Jul-06	2007-0072360	29-Mar-07	7,800,933	21-Sep-10
663	Method For Using A Memory Cell Comprising Switchable Semiconductor Memory Element With Trimmable Resistance	WO	US06/037963	27-Sep-06	WO 07/038709	5-Apr-07		
664	Multi-Use Memory Cell and Memory Array and Method for Use Therewith	TW	096123304	27-Jun-07			I441182	11-Jun-14
665	Multi-Use Memory Cell and Memory Array and Method for Use Therewith	WO	US07/013770	12-Jun-07				
666	Method for using a Multi-Use Memory Cell and Memory Array	US	11/496,984	31-Jul-06	20070070690	29-Mar-07	7,447,056	4-Nov-08
667	Multi-Use Memory Cell and Memory Array	US	11/496,985	31-Jul-06	20070069276	29-Mar-07		
668	Mixed-Use Memory Array and Method for Use Therewith	TW	096123305	27-Jun-07			I455130	1-Oct-14
669	Mixed-Use Memory Array and Method for Use Therewith	WO	US07/013769	12-Jun-07				
670	Method for Using a Mixed-Use Memory Array	US	11/496,983	31-Jul-06	2008-0025118	31-Jan-08	7,450,414	11-Nov-08
671	Mixed Use Memory Array	US	11/496,874	31-Jul-06	2008-0023790	31-Jan-08		

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672	Mixed-Use Memory Array with Different Data States and Method for Use Therewith	TW	096123303	27-Jun-07			I483262	1-May-15
673	Mixed-Use Memory Array with Different Data States and Method for Use Therewith	WO	US07/013772	12-Jun-07				
674	Method for Using a Mixed-Use Memory Array with Different Data States	US	11/497,021	31-Jul-06	2008-0025062	31-Jan-08	7,486,537	3-Feb-09
675	Mixed-Use Memory Array with Different Data States	US	11/496,870	31-Jul-06	2008-0025069	31-Jan-08		
676	Memory Cell Comprising Switchable Semiconductor Memory Element with Trimmable Resistance	TW	095135851	26-Sep-06		21-Apr-09	I309083	21-Apr-09
677	Memory Cell Comprising Switchable Semiconductor Memory Element with Trimmable Resistance	US	11/237,167	28-Sep-05	20070090425	26-Apr-07	7,800,932	21-Sep-10
678	Memory Cell Comprising Switchable Semiconductor Memory Element with Trimmable Resistance	WO	US06/037803	27-Sep-06	WO 07/038665	5-Apr-07		
679	Vertical Diode Doped with Antimony to Avoid or Limit Dopant Diffusion	CN	200680042220.4	8-Nov-06				
680	Vertical Diode Doped with Antimony to Avoid or Limit Dopant Diffusion	EP	06837153.3	8-Nov-06	1946385	23-Jul-08		
681	Vertical Diode Doped with Antimony to Avoid or Limit Dopant Diffusion	JP	2008-540158	8-Nov-06	P2009-416374A	16-Apr-09		
682	Vertical Diode Doped with Antimony to Avoid or Limit Dopant Diffusion	KR	2008-7011321	8-Nov-06				
683	Vertical Diode Doped with Antimony to Avoid or Limit Dopant Diffusion	WO	US06/043482	8-Nov-06	WO2007/058845	24-May-07		
684	VERTICAL DIODE DOPED WITH ANTIMONY TO AVOID OR LIMIT DOPANT DIFFUSION (MA-164TW)	TW	095141513	9-Nov-06	200731547	16-Aug-07		
685	Vertical Diode Doped with Antimony to Avoid or Limit Dopant Diffusion	US	11/271,078	10-Nov-05	200700102724	10-May-07		
686	MEMORY CELL COMPRISING NICKEL-COBALT OXIDE SWITCHING ELEMENT(MA-165-1WO)	CN	200680043951.0	20-Nov-06	CN101313423A	26-Nov-08	ZL200680043951.0	17-Nov-10
687	MEMORY CELL COMPRISING NICKEL-COBALT OXIDE SWITCHING ELEMENT(MA-165-1WO)	EP	06844459.5	20-Nov-06				
688	MEMORY CELL COMPRISING NICKEL-COBALT OXIDE SWITCHING ELEMENT(MA-165-1WO)	JP	2008-542405	20-Nov-06	P2009-517863A	30-Apr-09		
689	MEMORY CELL COMPRISING NICKEL-COBALT OXIDE SWITCHING ELEMENT(MA-165-1WO)	KR	2008-7014993	20-Nov-06				
690	MEMORY CELL COMPRISING NICKEL-COBALT OXIDE SWITCHING ELEMENT	TW	095143275	22-Nov-06				
691	Memory Cell Comprising Nickel-Cobalt Oxide Switching Element	US	11/440,899	24-May-06	20070114509	24-May-07	7,834,338	16-Nov-10

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692	MEMORY CELL COMPRISING NICKEL-COBALT OXIDE SWITCHING ELEMENT(MA-165-1WO)	WO	US06/045017	20-Nov-06				
693	REVERSIBLE RESISTIVITY-SWITCHING METAL OXIDE OR NITRIDE LAYER WITH ADDED METAL	CN	200680043939.X	20-Nov-06	CN101313422A	26-Nov-08	ZL200680043939.X	10-Mar-10
694	REVERSIBLE RESISTIVITY-SWITCHING METAL OXIDE OR NITRIDE LAYER WITH ADDED METAL	EP	06838165.6	20-Nov-06	1952451	6-Aug-08		
695	REVERSIBLE RESISTIVITY-SWITCHING METAL OXIDE OR NITRIDE LAYER WITH ADDED METAL	CN	201010004252.3	20-Nov-06	CN101853921A	6-Oct-10	ZL201010004252.3	21-Aug-13
696	REVERSIBLE RESISTIVITY-SWITCHING METAL OXIDE OR NITRIDE LAYER WITH ADDED METAL	JP	2008-542407	20-Nov-06	P2009-517864A	30-Apr-09	5237105	5-Apr-13
697	REVERSIBLE RESISTIVITY-SWITCHING METAL OXIDE OR NITRIDE LAYER WITH ADDED METAL	KR	2008-7014988	20-Nov-06				
698	REVERSIBLE RESISTIVITY-SWITCHING METAL OXIDE OR NITRIDE LAYER WITH ADDED METAL	TW	095143253	22-Nov-06	200733113	1-Sep-07	I323463	11-Apr-10
699	Devices Having Reversible Resistivity-Switching Metal Oxide or Nitride Layer with added Metal	US	11/287,452	23-Nov-05	20070114508	24-May-07	7,816,659	19-Oct-10
700	REVERSIBLE RESISTIVITY-SWITCHING METAL OXIDE OR NITRIDE LAYER WITH ADDED METAL	WO	US06/045034	20-Nov-06				
701	Method to Form Topography in a Deposited Layer Above a Substrate	US	11/298,015	9-Dec-05	20070134923	14-Jun-07	7,291,562	6-Nov-07
702	Laser Anneal of Vertically Oriented Semiconductor Structures While Maintaining a Dopant Profile	US	11/303,229	16-Dec-05	2007-0141858	21-Jun-07	7,615,502	10-Nov-09
703	Laser Anneal of Vertically Oriented Semiconductor Structures While Maintaining a Dopant Profile	WO	US06/048242	18-Dec-06	WO 07/075568	5-Jul-07		
704	Nonvolatile Rewritable Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	CN	200780012107.6	22-Mar-07	CN101416252A	22-Apr-09	ZI200780012107.6	30-Nov-11
705	Nonvolatile Rewritable Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	EP	07753755.3	22-Mar-07	2002444	17-Dec-08		
706	Nonvolatile Rewritable Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	JP	2009-502873	22-Mar-07	P2009-535793A	1-Oct-09		
707	Nonvolatile Rewritable Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	KR	2008-7026474	22-Mar-07				
708	Nonvolatile Rewritable Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	TW	096110614	27-Mar-07	200802822	1-Jan-08	I348757	11-Sep-11

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709	Nonvolatile Rewritable Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	US	11/395,421	31-Mar-06	2007-0228354	4-Oct-07	7,829,875	9-Nov-10
710	Nonvolatile Rewritable Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	WO	US07/007153	22-Mar-07	WO 07/126678	8-Nov-07		
711	Multilevel Nonvolatile Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	TW	096110615	27-Mar-07	200805629	16-Jan-08		
712	Multilevel Nonvolatile Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	US	11/394,903	31-Mar-06	2007-0236981	11-Oct-07	7,808,810	5-Oct-10
713	Multilevel Nonvolatile Memory Cell Comprising a Resistivity-Switching Oxide or Nitride and an Antifuse	WO	US07/007109	22-Mar-07				
714	Heterojunction Device Comprising a Semiconductor and a Resistivity-Switching Oxide or Nitride	US	13/553,963	20-Jul-12	2012-0280202	8-Nov-12	8,592,792	26-Nov-13
715	Heterojunction Device Comprising a Semiconductor and a Resistivity-Switching Oxide or Nitride	US	13/007,812	17-Jan-11	2011-0114913	19-May-11	8,227,787	24-Jul-12
716	Heterojunction Device Comprising a Semiconductor and a Resistivity-Switching Oxide or Nitride	TW	096110611	27-Mar-07			I380434	21-Dec-12
717	Heterojunction Device Comprising a Semiconductor and a Resistivity-Switching Oxide or Nitride	US	11/395,419	31-Mar-06	2007-0228414	4-Oct-07	7,875,871	25-Jan-11
718	Heterojunction Device Comprising a Semiconductor and a Resistivity-Switching Oxide or Nitride	WO	US07/007155	22-Mar-07	WO2007/126679	24-Apr-08		
719	Low-Temperature Metal-Induced Crystallization of Silicon-Germanium Films	US	11/395,420	31-Mar-06	2007-0246764	25-Oct-07	7,501,331	10-Mar-09
720	Memory Device with Improved Temperature Sensor Circuit	US	14/242,632	1-Apr-14				
721	Memory Device with Improved Temperature Sensor Circuit	US	11/649,569	4-Jan-07			7,277,343	2-Oct-07
722	Method for Improving the Precision of a Temperature-Sensor Circuit	US	14/242,623	1-Apr-14				
723	Method for Improving the Precision of a Temperature-Sensor Circuit	TW	096116905	11-May-07				
724	Method for Improving the Precision of a Temperature-Sensor Circuit	US	11/441,389	24-May-06			7,283,414	16-Oct-07
725	Method for Improving the Precision of a Temperature-Sensor Circuit	WO	US07/010307	27-Apr-07				

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726	Conductive Hard Mask to Protect Patterned Features During Trench Etch	CN	200780025175.6	22-May-07	CN101496174A	29-Jul-09		
727	Conductive Hard Mask to Protect Patterned Features During Trench Etch	EP	07784023.9	22-May-07	2025000	18-Feb-09		
728	Methods For Protecting Patterned Features During Trench Etch	US	13/890,321	9-May-13	2013-0244395	19-Sep-13	8,722,518	13-May-14
729	Conductive Hard Mask to Protect Patterned Features During Trench Etch	US	12/502,796	14-Jul-09	2009-0273022	5-Nov-09		
730	Conductive Hard Mask to Protect Patterned Features During Trench Etch	JP	2009-513377	22-May-07	P2009-539263A	12-Nov-09		
731	Conductive Hard Mask to Protect Patterned Features During Trench Etch	KR	2008-7031549	22-May-07				
732	Conductive Hard Mask to Protect Patterned Features During Trench Etch	TW	096119005	28-May-07	200807641	1-Feb-08	I357638	1-Feb-12
733	Conductive Hard Mask to Protect Patterned Features During Trench Etch	US	11/444,936	31-May-06	2007-0284656	13-Dec-07	7,575,984	18-Aug-09
734	Conductive Hard Mask to Protect Patterned Features During Trench Etch	WO	US07/069450	22-May-07	WO2007/143387	13-Dec-07		
735	Ultrashallow Semiconductor Contact By Outdiffusion from a Solid Source	TW	096119387	30-May-07	200810018	16-Feb-08		
736	Ultrashallow Semiconductor Contact By Outdiffusion from a Solid Source	US	11/478,706	30-Jun-06			7,754,605	13-Jul-10
737	Ultrashallow Semiconductor Contact By Outdiffusion from a Solid Source	WO	US07/015321	29-Jun-07	WO08/005412	8-May-08		
738	Controlled Pulse Operations in Non-Volatile Memory	TW	096127572	27-Jul-07	200826117	16-Jun-08	I397924	1-Jun-13
739	Controlled Pulse Operations in Non-Volatile Memory	WO	US07/074507	26-Jul-07	2008/016833	7-Feb-08		
740	Controlled Pulse Operations in Non-Volatile Memory	US	11/461,393	31-Jul-06	2008-0025076	31-Jan-08	7,522,448	21-Apr-09
741	Systems for Controlled Pulse Operations in Non-Volatile Memory	US	11/461,399	31-Jul-06	2008-0025077	31-Jan-08	7,719,874	18-May-10
742	High Bandwidth One Time Field-Programmable Memory	TW	096127589	27-Jul-07	200826279	16-Jun-08	I346383	1-Aug-11
743	High Bandwidth One Time Field-Programmable Memory	WO	US07/074520	26-Jul-07	2008/016835	7-Feb-08		
744	High Bandwidth One Time Field-Programmable Memory	US	11/461,410	31-Jul-06	2008-0025061	31-Jan-08	7,499,355	3-Mar-09
745	Systems for High Bandwidth One Time Field-Programmable Memory	US	11/461,419	31-Jul-06	2008-0025067	31-Jan-08	7,499,304	3-Mar-09
746	Method Of Operating Non-Volatile Storage And Non-Volatile Memory System	TW	096127570	27-Jul-07	200830315	16-Jul-08	I356415	11-Jan-12
747	Reverse Bias Trim Operations in Non-Volatile Memory	WO	US07/074564	27-Jul-07	2008/016844	7-Feb-08		

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748	Reverse Bias Trim Operations in Non-Volatile Memory	US	11/461,424	31-Jul-06	2008-0025068	31-Jan-08	7,495,947	24-Feb-09
749	Systems for Reverse Bias Trim Operations in Non-Volatile Memory	US	11/461,431	31-Jul-06	2008-0025078	31-Jan-08	7,492,630	17-Feb-09
750	Method and Apparatus for using a passive element memory arry incorporating reversible polarity word line and bit line decoders	CN	200780031665.7	31-Jul-07	CN101506898A	12-Aug-09	ZL200780031665.7	4-Jul-12
751	Method and Apparatus for using a passive element memory array incorporating reversible polarity word line and bit line decoders	DE	07840617.0	31-Jul-07	2062262	27-May-09	2062262	7-May-14
752	Method and Apparatus for using a passive element memory array incorporating reversible polarity word line and bit line decoders	EP	07840617.0	31-Jul-07	2062262	27-May-09	2062262	7-May-14
753	Method and Apparatus for using a passive element memory array incorporating reversible polarity word line and bit line decoders	GB	07840617.0	31-Jul-07	2062262	27-May-09	2062262	7-May-14
754	Method and Apparatus for using a passive element memory arry incorporating reversible polarity word line and bit line decoders	JP	2009-523020	31-Jul-07	545835/2009	24-Dec-09	5252233	26-Apr-13
755	Method and Apparatus for passive element memory array incorporating reversible polarity word line and bit line decoders	KR	2009-7004221	31-Jul-07			10-1478193	24-Dec-14
756	Method and Apparatus for using a passive element memory arry incorporating reversible polarity word line and bit line decoders	TW	096128079	31-Jul-07	200814067	16-Mar-08	I345785	21-Jul-11
757	Method and Apparatus for using a passive element memory arry incorporating reversible polarity word line and bit line decoders	WO	US07/074883	31-Jul-07	WO2008/016932	7-Feb-08		
758	Method for Using a Passive Element Memory Array Incorporating Reversible Polarity Word Line and Bit Line Decoders	US	11/461,364	31-Jul-06	2008-0025132	31-Jan-08	7,463,546	9-Dec-08
759	Passive Element Memory Array Incorporating Reversible Polarity Word Line and Bit Line Decoders	US	11/461,339	31-Jul-06	2008-0025066	31-Jan-08	7,554,832	30-Jun-09
760	Method and Apparatus for Reading a Multi-Level Passive Element Memory Cell Array	CN	200780033061.6	31-Jul-07	CN101512663A	19-Aug-09	ZL200780033061.6	28-Aug-13

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761	Method and Apparatus for Reading a Multi-Level Passive Element Memory Cell Array	DE	07799950.6	31-Jul-07	2052390	29-Apr-09	2052390	3-Jun-15
762	Method and Apparatus for Reading a Multi-Level Passive Element Memory Cell Array	EP	07799950.6	31-Jul-07	2052390	29-Apr-09	2052390	3-Jun-15
763	Method and Apparatus for Reading a Multi-Level Passive Element Memory Cell Array	JP	2009-523027	31-Jul-07	545836/2009	24-Dec-09	5207081	1-Mar-13
764	Method and Apparatus for Reading a Multi-Level Passive Element Memory Cell Array	KR	2009-7004237	31-Jul-07			10-1446581	25-Sep-14
765	Method and Apparatus for Reading a Multi-Level Passive Element Memory Cell Array	TW	096128067	31-Jul-07	200816453	1-Apr-08	I378551	1-Dec-12
766	Method and Apparatus for Reading a Multi-Level Passive Element Memory Cell Array	WO	US07/074899	31-Jul-07	WO2008/016946	7-Feb-08		
767	Method for Reading a Multi-Level Passive Element Memory Cell Array	US	11/461,367	31-Jul-06	2008-0025089	31-Jan-08	7,542,338	2-Jun-09
768	Method and Apparatus for Reading a Multi-Level Passive Element Memory Cell Array	US	12/476,242	1-Jun-09				
769	Apparatus for Reading a Multi-Level Passive Element Memory Cell Array	US	11/461,343	31-Jul-06	2008-0025088	31-Jan-08	7,542,337	2-Jun-09
770	Method and Apparatus for using dual data dependent busses for coupling read/write	CN	200780031596.X	31-Jul-07	CN101506897A	12-Aug-09	ZL200780031596.X	13-Feb-13
771	Method and Apparatus for using dual data dependent busses for coupling read/write	DE	078406212	31-Jul-07	2062263	27-May-09	2062263	2-May-12
772	Method and Apparatus for using dual data dependent busses for coupling read/write	EP	07840621.2	31-Jul-07	2062263	27-May-09	2062263	2-May-12
773	Method and Apparatus for using dual data dependent busses for coupling read/write	FR	078406212	31-Jul-07	2062263	27-May-09	2062263	2-May-12
774	Method and Apparatus for using dual data dependent busses for coupling read/write	GB	078406212	31-Jul-07	2062263	27-May-09	2062263	2-May-12
775	Method and Apparatus for using dual data dependent busses for coupling read/write	JP	2009-523029	31-Jul-07	545837/2009	24-Dec-09	5201143	22-Feb-13
776	DUAL DATA-DEPENDENT BUSSES FOR COUPLING READ/WRITE CIRCUITS TO A MEMORY ARRAY	KR	2009-7004226	31-Jul-07			10-1465557	20-Nov-14
777	Method and Apparatus for using dual data dependent busses for coupling read/write	NL	078406212	31-Jul-07	2062263	27-May-09	2062263	2-May-12
778	Method and Apparatus for using dual data dependent busses for coupling read/write	TW	096128071	31-Jul-07	200823921	1-Jun-08	I345790	21-Jul-11
779	Method and Apparatus for using dual data dependent busses for coupling read/write	WO	US07/074901	31-Jul-07	WO2008/016948	7-Feb-08		
780	DECODER CIRCUITRY PROVIDING FORWARD AND REVERSE MODES OF MEMORY ARRAY OPERATION AND METHOD FOR BIASING SAME	CN	201180047497.7	31-Aug-11	CN103155042A	12-Jun-13	ZL201180047497.7	

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781	DECODER CIRCUITRY PROVIDING FORWARD AND REVERSE MODES OF MEMORY ARRAY OPERATION AND METHOD FOR BIASING SAME	JP	2013-531604	31-Aug-11	2013-539152	17-Oct-13		
782	DECODER CIRCUITRY PROVIDING FORWARD AND REVERSE MODES OF MEMORY ARRAY OPERATION AND METHOD FOR BIASING SAME	KR	2013-7010985	31-Aug-11				
783	DECODER CIRCUITRY PROVIDING FORWARD AND REVERSE MODES OF MEMORY ARRAY OPERATION AND METHOD FOR BIASING SAME	TW	100131818	2-Sep-11	201214460	1-Apr-12		
784	DECODER CIRCUITRY PROVIDING FORWARD AND REVERSE MODES OF MEMORY ARRAY OPERATION AND METHOD FOR BIASING SAME	US	12/895,523	30-Sep-10	2011-0019495	27-Jan-11	8,279,704	2-Oct-12
785	DECODER CIRCUITRY PROVIDING FORWARD AND REVERSE MODES OF MEMORY ARRAY OPERATION AND METHOD FOR BIASING SAME	WO	US11/050012	31-Aug-11	WO/044433	5-Apr-12		
786	Reversible-Polarity Decoder Circuit And Method	US	12/396,461	2-Mar-09	2009-0161474	25-Jun-09	8,004,927	23-Aug-11
787	Memory Array Circuit Incorporating Multiple Array Block Selection and Related Method	US	13/215,134	22-Aug-11	2011-0299354	8-Dec-11	8,509,025	13-Aug-13
788	Method for using dual data dependent busses for coupling read/write circuits to a memory array	US	11/461,369	31-Jul-06	2008-0025133	31-Jan-08	7,499,366	3-Mar-09
789	Dual Data dependent busses for coupling read/write circuits to a memory array	US	11/461,352	31-Jul-06	2008-0025131	31-Jan-08	7,486,587	3-Feb-09
790	Method and Apparatus for Memory Array Incorporating Two Data Busses for Memory Array Block Selection	CN	200780031655.3	31-Jul-07	CN101506896A	12-Aug-09	ZL200780031655.3	8-May-13
791	Method and Apparatus for Memory Array Incorporating Two Data Busses for Memory Array Block Selection	DE	07840623.8	31-Jul-07	2062264	27-May-09	2062264	7-Oct-15
792	Method and Apparatus for Memory Array Incorporating Two Data Busses for Memory Array Block Selection	EP	07840623.8	31-Jul-07	2062264	27-May-09	2062264	7-Oct-15
793	Method and Apparatus for Memory Array Incorporating Two Data Busses for Memory Array Block Selection	JP	2009-523031	31-Jul-07	545838/2009	24-Dec-09	5279139	31-May-13
794	Method and Apparatus for Memory Array Incorporating Two Data Busses for Memory Array Block Selection	KR	2009-7004228	31-Jul-07			10-1494333	11-Feb-15
795	Method and Apparatus for Using Two Data Busses for Memory Array Block Selection	TW	096128052	31-Jul-07	200828340	1-Jul-08	I345791	21-Jul-11

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796	Method and Apparatus for Memory Array Incorporating Two Data Busses for Memory Array Block Selection	WO	US07/074903	31-Jul-07	WO2008/016950	7-Feb-08		
797	Method for Using Two Data Busses for Memory Array Block Selection	US	11/461,372	31-Jul-06	2008-0025134	31-Jan-08	7,570,523	4-Aug-09
798	Memory Array Incorporating Two Data Busses for Memory Array Block Selection	US	11/461,359	31-Jul-06	2008-0025085	31-Jan-08	7,463,536	9-Dec-08
799	Method and Apparatus for Using Hierarchical Bit Line Bias Bus for Block Selectable Memory Array	TW	096128078	31-Jul-07	200826114	16-Jun-08	I345787	21-Jul-11
800	Method and Apparatus for Using Hierarchical Bit Line Bias Bus for Block Selectable Memory Array	WO	US07/074904	31-Jul-07	WO2008/016951	7-Feb-08		
801	Method for Using Hierarchical Bit Line Bias Bus for Block Selectable Memory Array	US	11/461,376	31-Jul-06	2008-0025094	31-Jan-08	7,596,050	29-Sep-09
802	Hierarchical Bit Line Bias Bus for Block Selectable Memory Array	US	11/461,362	31-Jul-06	2008-0025093	31-Jan-08	7,633,828	15-Dec-09
803	Method of Mask Making to Prevent Phase Edge for Chromeless Phase Shifting Mask	TW	096133284	6-Sep-07				
804	Method of Mask Making to Prevent Phase Edge And Overlay Shift For Chrome-Less Phase Shifting Mask	US	11/470,359	6-Sep-06			7,662,521	16-Feb-10
805	Method of Mask Making to Prevent Phase Edge for Chromeless Phase Shifting Mask	WO	US07/077746	6-Sep-07				
806	Bandgap Engineered Charge Storage Layer for 3D TFT	TW	096125083	10-Jul-07	200814337	16-Mar-08		
807	Bandgap Engineered Charge Storage Layer for 3D TFT	US	11/483,671	11-Jul-06	2008-0012065	17-Jan-08		
808	Bandgap Engineered Charge Storage Layer for 3D TFT	WO	US07/14732	26-Jun-07	WO2008/008171	17-Jan-08		
809	A Smart Write Circuit for Diode-Based Memory Cells	US	11/537,633	30-Sep-06				
810	Method for Protecting Memory Cells During Programming	US	11/552,441	24-Oct-06	2008-0094892	24-Apr-08	7,589,989	15-Sep-09
811	Memory Device for Protecting Memory Cells During Programming	US	12/140,991	17-Jun-08	2008-0248213	9-Oct-08	7,593,249	22-Sep-09
812	Memory device for protecting memory cells during programming	US	11/552,426	24-Oct-06	2008-0094913	24-Apr-08	7,391,638	24-Jun-08
813	Method for Controlling Current During Programming of Memory Cells	TW	096139712	23-Oct-07	200828323	1-Jul-08		
814	Method to Achieve Current Control During a Write Operation in a Diode-Based Non-Volatile Memory	US	11/537,632	30-Sep-06				

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815	Method for Controlling Current During Programming of Memory Cells	WO	US07/081936	19-Oct-07	WO08/051840	2-May-08		
816	Method for Controlling Current During Programming of Memory Cells	US	11/552,462	24-Oct-06	2008-0094915	24-Apr-08	7,420,850	2-Sep-08
817	Memory Device for Controlling Current During Programming of Memory Cells	US	11/552,472	24-Oct-06	2008-0094916	24-Apr-08	7,420,851	2-Sep-08
818	METHOD OF MAKING A NONVOLATILE PHASE CHANGE MEMORY CELL HAVING A REDUCED CONTACT AREA (MXA-187-X) (MD-302)	TW	096143406	16-Nov-07	200840033	1-Oct-08		
819	MAKING A NONVOLATILE PHASE CHANGE MEMORY CELL HAVING A REDUCED CONTACT AREA AND METHOD OF MAKING (MXA-187-X) (MD-302)	WO	US07/084841	15-Nov-07				
820	METHOD OF MAKING A NONVOLATILE PHASE CHANGE MEMORY CELL HAVING A REDUCED CONTACT AREA (MXA-187-X) (MD-302)	US	11/560,792	16-Nov-06	2008-0119007	22-May-08	8,163,593	24-Apr-12
821	NONVOLATILE PHASE CHANGE MEMORY CELL HAVING A REDUCED CONTACT AREA	US	11/560,791	16-Nov-06	2008-0116441	22-May-08	7,728,318	1-Jun-10
822	Method for Isotropic Doping of a Non-Planar Surface Exposed in a Void	US	11/610,090	13-Dec-06	20080145994	19-Jun-08	7,811,916	12-Oct-10
823	Hybrid Mask and Method of Forming Same	TW	096150899	28-Dec-07	200842509	1-Nov-08		
824	Hybrid Mask and Method of Forming Same	US	11/648,245	29-Dec-06	2008-0160424	3-Jul-08	7,759,023	20-Jul-10
825	Hybrid Mask and Method of Forming Same	WO	US07/088683	21-Dec-07				
826	Multiple Polarity Reversible Charge Pump Circuit And Related Methods	CN	200780050895.8	19-Dec-07				
827	Multiple Polarity Reversible Charge Pump Circuit And Related Methods	DE	07865875.4	19-Dec-07	2109936	21-Oct-09	2109936	16-Apr-14
828	Multiple Polarity Reversible Charge Pump Circuit And Related Methods	EP	07865875.4	19-Dec-07	2109936	21-Oct-09	2109936	16-Apr-14
829	Multiple Polarity Reversible Charge Pump Circuit And Related Methods	GB	07865875.4	19-Dec-07	2109936	21-Oct-09	2109936	16-Apr-14
830	Multiple Polarity Reversible Charge Pump Circuit And Related Methods	JP	2009-544197	19-Dec-07	515423/2010	6-May-10	5273681	24-May-13
831	Multiple Polarity Reversible Charge Pump Circuit And Related Methods	KR	2009-7016001	19-Dec-07				
832	Multiple Polarity Reversible Charge Pump Circuit and Related Methods	TW	096150856	28-Dec-07	200842888	1-Nov-08	I360131	11-Mar-12
833	Multiple Polarity Reversible Charge Pump Circuit And Related Methods	WO	US07/088159	19-Dec-07	WO2008/082994	10-Jul-08		
834	Method for Using a Multiple Polarity Reversible Charge Pump Circuit	US	11/618,838	31-Dec-06	2008-0157853	3-Jul-08	7,495,500	24-Feb-09
835	Cooperative Charge Pump Circuit And Method	US	12/352,489	12-Jan-09	2009-0115498	7-May-09	7,696,812	13-Apr-10

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836	Multiple Polarity Reversible Charge Pump Circuit	US	11/618,841	31-Dec-06	2008-0157854	3-Jul-08	7,477,093	13-Jan-09
837	Method for Using a Reversible Polarity Decoder Circuit	CN	200780050936.3	19-Dec-07	CN101627437A	13-Jan-10	ZL200780050936.3	5-Sep-12
838	Reversible Polarity Decoder Circuit and Related Methods	DE	07869534.3	19-Dec-07	2109863	21-Oct-09	2109863	18-Jun-14
839	Reversible Polarity Decoder Circuit and Related Methods	EP	07869534.3	19-Dec-07	2109863	21-Oct-09	2109863	18-Jun-14
840	Reversible Polarity Decoder Circuit and Related Methods	GB	07869534.3	19-Dec-07	2109863	21-Oct-09	2109863	18-Jun-14
841	Reversible Polarity Decoder Circuit and Related Methods	JP	2009-544198	19-Dec-07	2010-515200	6-May-10	5164279	28-Dec-12
842	Reversible Polarity Decoder Circuit and Related Methods	KR	2009-7016003	19-Dec-07			10-1376213	13-Mar-14
843	Reversible Polarity Decoder Circuit and Related Methods	TW	096150872	28-Dec-07	200842894	1-Nov-08	I377579	21-Nov-12
844	Method for Using a Reversible Polarity Decoder Circuit	WO	US07/088161	19-Dec-07	WO2008/082995	10-Jul-08		
845	Method for Using a Reversible Polarity Decoder Circuit	US	11/618,843	31-Dec-06	2008-0159052	3-Jul-08	7,525,869	28-Apr-09
846	REVERSIBLE POLARITY DECODER CIRCUIT AND RELATED METHODS	US	12/476,244	1-Jun-09				
847	Reversible Polarity Decoder Circuit	US	11/618,844	31-Dec-06	2008-0159053	3-Jul-08	7,542,370	2-Jun-09
848	Imaging Post Structures Using X and Y Double Dipole Optics and a Single Mask	US	12/796,449	8-Jun-10			7,968,277	28-Jun-11
849	Imaging Post Structures Using X and Y Double Dipole Optics and a Single Mask	TW	096150644	27-Dec-07	200846836	1-Dec-08	I386764	21-Feb-13
850	Imaging Post Structures Using X and Y Dipole Optics and a Single Mask	US	11/618,776	30-Dec-06	2008-0160423	3-Jul-08	7,794,921	14-Sep-10
851	Imaging Post Structures Using X and Y Double Dipole Optics and a Single Mask	WO	US07/088901	27-Dec-07	WO2008/083197	10-Jul-08		
852	Methods and Apparatus for Employing Redundant Arrays to Configure Non-Volatile Memory	US	11/669,917	31-Jan-07	2008-0184057	31-Jul-08	7,870,471	11-Jan-11
853	Methods and Apparatus for Employing Redundant Arrays to Configure Non-Volatile Memory	US	11/669,918	31-Jan-07	2008-0184065	31-Jul-08	7,870,472	11-Jan-11
854	Methods and Apparatus for Using a Configuration Array Similar to an Associated Data Array	US	12/955,377	29-Nov-10	2011-0075466	31-Mar-11	8,351,259	8-Jan-13
855	Methods and Apparatus for Using a Configuration Array Similar to an Associated Data Array	US	11/669,919	31-Jan-07	2008-0184004	31-Jul-08	7,843,729	30-Nov-10

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856	Methods and Apparatus for Using a Configuration Array Similar to an Associated Data Array	US	11/669,923	31-Jan-07	2008-0184005	31-Jul-08	7,697,329	13-Apr-10
857	Embedded Memory in a CMOS Circuit and Methods of Forming the Same	US	11/669,859	31-Jan-07	2008-0182367	31-Jul-08	7,888,200	15-Feb-11
858	Embedded Memory in a CMOS Circuit and Methods of Forming the Same	US	11/669,850	31-Jan-07	2008-0179685	31-Jul-08	7,868,388	11-Jan-11
859	MEMORY ARRAYS INCLUDING MEMORY LEVELS THAT SHARE CONDUCTORS, AND METHODS OF FORMING SUCH MEMORY ARRAYS	US	12/844,037	27-Jul-10	2010-0288996	18-Nov-10		
860	Method to Form Upward Pointing P-I-N Diodes Having Large and Uniform Current	US	11/692,151	27-Mar-07	2007-0190722	16-Aug-07	7,767,499	3-Aug-10
861	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	CN	200880017712.7	26-Mar-08	CN101681914A	24-Mar-10	ZL200880017712.7	22-Feb-12
862	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	DE	08826319.9	26-Mar-08	2130227	9-Dec-09	2130227	15-May-13
863	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	EP	08826319.9	26-Mar-08	2130227	9-Dec-09	2130227	15-May-13
864	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	FR	08826319.9	26-Mar-08	2130227	9-Dec-09	2130227	15-May-13
865	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	GB	08826319.9	26-Mar-08	2130227	9-Dec-09	2130227	15-May-13
866	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current and Methods of Forming the Same	CN	201210012173.6	26-Mar-08	102522419	27-Jun-12		
867	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current and Methods of Forming the Same	JP	2010-500979	26-Mar-08	2010-522990	8-Jul-10	5735271	24-Apr-15
868	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current and Methods of Forming the Same	KR	2009-7019777	26-Mar-08			10-1517913	29-Apr-15
869	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	NL	08826319.9	26-Mar-08	2130227	9-Dec-09	2130227	15-May-13
870	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current and Methods of Forming the Same	TW	097111125	27-Mar-08	200901331	1-Jan-09	I441263	11-Jun-14
871	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	WO	US2008/003975	26-Mar-08	WO2009/008919	15-Jan-09		
872	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	US	12/940,251	5-Nov-10	2011-0049466	3-Mar-11	8,059,444	15-Nov-11
873	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	US	13/294,224	11-Nov-11	2012-0056147	8-Mar-12	8,427,858	23-Apr-13

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874	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	US	13/863,027	15-Apr-13	2013-0228738	5-Sep-13	8,737,110	27-May-14
875	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	US	14/249,628	10-Apr-14	2014-0217354	7-Aug-14	9,025,372	5-May-15
876	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	US	12/478,481	4-Jun-09	2009-0316468	24-Dec-09	7,830,694	9-Nov-10
877	Large Array of Upward Pointing P-I-N Diodes Having Large and Uniform Current	US	11/692,153	27-Mar-07	2008-0239787	2-Oct-08	7,586,773	8-Sep-09
878	Method to Program a Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element	US	13/083,746	11-Apr-11	2011-0210305	1-Sep-11	8,203,864	19-Jun-12
879	Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element and Methods for Forming the Same	CN	200880016582.5	26-Mar-08	CN101681921A	24-Mar-10	ZL200880016582.5	27-Mar-13
880	Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element and Methods for Forming the Same	EP	08742323.2	26-Mar-08	2140492	6-Jan-10		
881	Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element and Methods for Forming the Same	JP	2010-500999	26-Mar-08	P2010-522991A	8-Jul-10		
882	Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element and Methods for Forming the Same	KR	2009-7019877	26-Mar-08				
883	Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element and Methods for Forming the Same	TW	097111114	27-Mar-08	200903782	16-Jan-09		
884	Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element and Methods for Forming the Same	WO	US2008/004018	26-Mar-08	WO2008/118486	2-Oct-08		
885	Method to Program a Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element	US	12/693,782	26-Jan-10	2010-0142255	10-Jun-10	7,924,602	12-Apr-11
886	Method to Form a Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element	US	11/692,144	27-Mar-07	2008-0239790	2-Oct-08	7,667,999	23-Feb-10
887	Memory Cell Comprising a Carbon Nanotube Fabric Element and a Steering Element	US	13/182,960	14-Jul-11	2011-0266514	3-Nov-11	8,847,200	30-Sep-14
888	Memory Cell Comprising a Carbon Nantube Fabric Element and a Steering Element	US	11/692,148	27-Mar-07	2008-0237599	2-Oct-08	7,982,209	19-Jul-11
889	Three Dimensional NAND Memory and Method of Making Thereof	TW	097110923	26-Mar-08			I424536	21-Jan-14
890	Three Dimensional NAND Memory and Method of Making Thereof	WO	US08/003908	26-Mar-08	WO2008/118433	2-Oct-08		

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891	Method of Making Three Dimensional NAND Memory	US	11/691,917	27-Mar-07			7,575,973	18-Aug-09
892	Three-Dimensional NAND Memory	US	11/691,939	27-Mar-07	2008-0237602	2-Oct-08	7,851,851	14-Dec-10
893	Three Dimensional NAND Memory and Method of Making Thereof	WO	US08/003910	26-Mar-08	WO2008/118435	2-Oct-08		
894	Method of Making Three Dimensional NAND Memory	US	11/691,885	27-Mar-07	2008-0242008	2-Oct-08	7,745,265	29-Jun-10
895	Three-Dimensional NAND Memory	US	11/691,901	27-Mar-07			7,848,145	7-Dec-10
896	Three Dimensional NAND Memory and Method of Making Thereof	CN	200880017752.1	26-Mar-08	CN101681884A	24-Mar-10	ZL200880017752.1	18-Jul-12
897	Three Dimensional NAND Memory and Method of Making Thereof	EP	08742252.3	26-Mar-08				
898	Three Dimensional NAND Memory and Method of Making Thereof	JP	2010-500961	26-Mar-08	P2010-522988A	8-Jul-10		
899	Three Dimensional NAND Memory and Method of Making Thereof	KR	2009-7022157	26-Mar-08			10-1437892	29-Aug-14
900	Three Dimensional NAND Memory and Method of Making Thereof	WO	US08/003906	26-Mar-08	WO08/118432	2-Oct-08		
901	Method of Making Three Dimensional NAND Memory	US	11/691,840	27-Mar-07	20080242034	2-Oct-08	7,514,321	7-Apr-09
902	Three Dimensional NAND Memory	US	11/691,858	27-Mar-07	2008-0237698	2-Oct-08	7,808,038	5-Oct-10
903	Diffusion Barrier in 3D Memory and Method for Implementing	TW	097111290	28-Mar-08				
904	Diffusion Barrier in 3D Memory and Method for Implementing	WO	US08/058358	27-Mar-08	WO2008/121674	9-Oct-08		
905	Method for Implementing Diffusion Barrier in 3D Memory	US	11/731,579	30-Mar-07	2008-0242080	2-Oct-08	7,629,253	8-Dec-09
906	Implementation of Diffusion Barrier in 3D Memory	US	11/731,676	30-Mar-07	2008-0237862	2-Oct-08	8,124,971	28-Feb-12
907	Method of Making a Diode Read/Write Memory Cell in a Programmed State	US	12/588,088	2-Oct-09	2010-0110752	6-May-10	7,915,094	29-Mar-11
908	Method of Making a Diode Read/Write Memory Cell in a Programmed State	US	11/693,845	30-Mar-07	2007-0164309A1	19-Jul-07	7,618,850	17-Nov-09
909	Memory Cell Comprising a Diode Fabricated in a Low Resistivity, Programmed State	US	11/693,858	30-Mar-07				
910	Method of Load-Based Voltage Generation	US	11/694,798	30-Mar-07	2008-0239856	2-Oct-08	7,515,488	7-Apr-09
911	Device with Load-Based Voltage Generation	US	11/694,760	30-Mar-07	2008-0239802	2-Oct-08	7,558,129	7-Jul-09
912	Method for Managing Electrical Load on an Electronic Device	US	11/694,746	30-Mar-07	2008-0239836	2-Oct-08	7,580,298	25-Aug-09
913	Load Management for Memory Device	US	11/694,714	30-Mar-07	2008-0239801	2-Oct-08	7,580,296	25-Aug-09
914	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	CN	200880018315.1	31-Mar-08	CN101682328A	24-Mar-10	ZL200880018315.1	30-Apr-14
915	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	DE	08744804.9	31-Mar-08	2132873	16-Dec-09	2132873	22-Aug-12

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916	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	EP	08744804.9	31-Mar-08	2132873	16-Dec-09	2132873	22-Aug-12
917	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	FR	08744804.9	31-Mar-08	2132873	16-Dec-09	2132873	22-Aug-12
918	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	GB	08744804.9	31-Mar-08	2132873	16-Dec-09	2132873	22-Aug-12
919	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	JP	2010-501285	31-Mar-08	P2010-524303A	15-Jul-10	4926275	17-Feb-12
920	Level Shifter Circuit Incorporating Transistor Snap-Back Protection	KR	2009-7022680	31-Mar-08			10-1505396	18-Mar-15
921	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	NL	08744804.9	31-Mar-08	2132873	16-Dec-09	2132873	22-Aug-12
922	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	TW	097111717	31-Mar-08	200847627	1-Dec-08	I350055	1-Oct-11
923	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	WO	US08/058933	31-Mar-08	WO2008/121977	9-Oct-08		
924	Method for Incorporating Transistor Snap-Back Protection in a Level Shifter Circuit	US	11/695,011	31-Mar-07	2008-0238522	2-Oct-08	7,696,804	13-Apr-10
925	Level Shifter Circuit Incorporating Transistor Snap-Back Protection	US	11/695,013	31-Mar-07	2008-0238523	2-Oct-08	7,696,805	13-Apr-10
926	Spatially Distributed Amplifier Circuit	CN	200880018235.6	31-Mar-08	CN101715594A	26-May-10	ZL200880018235.6	30-Apr-14
927	Spatially Distributed Amplifier Circuit	DE	08744808.0	31-Mar-08	2132747	16-Dec-09	2132747	24-Apr-13
928	Spatially Distributed Amplifier Circuit	EP	08744808.0	31-Mar-08	2132747	16-Dec-09	2132747	24-Apr-13
929	Spatially Distributed Amplifier Circuit	GB	08744808.0	31-Mar-08	2132747	16-Dec-09	2132747	24-Apr-13
930	Spatially Distributed Amplifier Circuit	JP	2010-501287	31-Mar-08	P2010-524304A	15-Jul-10	5171934	11-Jan-13
931	Spatially Distributed Amplifier Circuit	KR	2009-7022690	31-Mar-08			10-1459312	3-Nov-14
932	Spatially Distributed Amplifier Circuit and Method for Operating the Same	TW	097111716	31-Mar-08	200907999	16-Feb-09	I378466	1-Dec-12
933	Spatially Distributed Amplifier Circuit	WO	US08/058937	31-Mar-08	WO2008/121979	9-Oct-08		
934	Method for Using a Spatially Distributed Amplifier Circuit	US	11/695,015	31-Mar-07	2008-0239839	2-Oct-08	7,558,140	7-Jul-09
935	Spatially Distributed Amplifier Circuit	US	11/695,017	31-Mar-07	2008-0238541	2-Oct-08	7,554,406	30-Jun-09
936	Method to Form Low-Defect Polycrystalline Semiconductor Material for Use in a Transistor	TW		13-Jun-08				
937	Method to Form Low-Defect Polycrystalline Semiconductor Material for Use in a Transistor	US	11/763,671	15-Jun-07	2008-0311710	18-Dec-08	7,790,534	7-Sep-10
938	Method to Form Low-Defect Polycrystalline Semiconductor Material for Use in a Transistor	WO	US08/007321	12-Jun-08	WO08/156624	24-Dec-08		
939	Forming Polycrystalline Thin Film Bipolar Transistors and Methods of Making Same	TW	097122362	13-Jun-08	200908296	16-Feb-09		

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940	Polycrystalline Thin Film Bipolar Transistors and Methods of Making the Same	WO	US2008/007439	13-Jun-08	WO2008/156694	24-Dec-08		
941	Method for Forming Polycrystalline Thin Film Bipolar Transistors	US	11/763,876	15-Jun-07	2008-0311722	18-Dec-08	7,855,119	21-Dec-10
942	Polycrystalline Thin Film Bipolar Transistors	US	11/763,816	15-Jun-07	2008-0308903	18-Dec-08	8,004,013	23-Aug-11
943	Junction Diode with Reduced Reverse Current	CN	200880020493.8	18-Jun-08	CN101720510A	2-Jun-10	ZL200880020493.8	12-Jun-13
944	Junction Diode with Reduced Reverse Current	EP	08768531.9	18-Jun-08	2162921	17-Mar-10		
945	Junction Diode with Reduced Reverse Current	JP	2010-513225	18-Jun-08	2010-530642	9-Sep-10	5363474	13-Sep-13
946	Junction Diode with Reduced Reverse Current	KR	2010-7000954	18-Jun-08			10-1438420	1-Sep-14
947	Junction Diode with Reduced Reverse Current	TW	097122707	18-Jun-08			I446523	21-Jul-14
948	Junction Diode with Reduced Reverse Current	US	11/765,254	19-Jun-07	2008-0318397	25-Dec-08	7,537,968	26-May-09
949	Junction Diode with Reduced Reverse Current	WO	US08/07530	18-Jun-08	WO2008/156754	24-Dec-08		
950	Method to Form HIghly Scalable Thin Film Transistor	TW	097122706	18-Jun-08				
951	Method to Form HIghly Scalable Thin Film Transistor	WO	US08/007532	18-Jun-08	WO2008/156756	24-Dec-08		
952	Method to Form HIghly Scalable Thin Film Transistor	US	11/765,274	19-Jun-07				
953	HIghly Scalable Thin Film Transistor	US	12/659,480	10-Mar-10	2010-0173457	8-Jul-10	7,888,205	15-Feb-11
954	HIghly Scalable Thin Film Transistor	US	11/765,269	19-Jun-07	2008-0315206	25-Dec-08		
955	Non-Volatile Memory Device Containing Carbon or Nitrogen Doped Diode and Method of Making Thereof	CN	200880021404.1	23-Jun-08	CN101720507A	2-Jun-10	ZL200880021404.1	11-Jan-12
956	Non-Volatile Memory Device Containing Carbon or Nitrogen Doped Diode and Method of Making Thereof	DE	08768725.7	23-Jun-08	2168161	31-Dec-08	2168161	23-Sep-15
957	Non-Volatile Memory Device Containing Carbon or Nitrogen Doped Diode and Method of Making Thereof	EP	08768725.7	23-Jun-08	2168161	31-Dec-08	2168161	23-Sep-15
958	Non-Volatile Memory Device Containing Carbon or Nitrogen Doped Diode and Method of Making Thereof	JP	2010-513271	23-Jun-08	P2011-517364A	2-Jun-11	5545872	23-May-14
959	Non-Volatile Memory Device Containing Carbon or Nitrogen Doped Diode and Method of Making Thereof	KR	2010-7001563	23-Jun-08				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
960	Method of Making Non-Volatile Memory Device Containing Carbon or Nitrogen Doped Diode	TW	097123543	24-Jun-08				
961	Non-Volatile Memory Device Containing Carbon or Nitrogen Doped Diode and Method of Making Thereof	WO	US08/007801	23-Jun-08	WO2009/002476	31-Dec-08		
962	Method of Making Non-Volatile Memory Device Containing Carbon or Nitrogen Doped Diode	US	11/819,041	25-Jun-07	2008-0316795	25-Dec-08	8,072,791	6-Dec-11
963	Non-Volatile Memory Device Containing Carbon or Nitrogen Doped Diode	US	11/819,042	25-Jun-07	2008-0316808	25-Dec-08	8,102,694	24-Jan-12
964	Programming Methods of a Diode Using Forward Bias	CN	200880022070.X	23-Jun-08	CN101711112A	19-May-10		
965	Programming Methods to Increase Window for Reverse Write 3D Cell	EP	08768724.0	23-Jun-08	2165335	24-Mar-10		
966	Programming Methods to Increase Window for Reverse Write 3D Cell	JP	2010-513270	23-Jun-08	P2010-531522A	24-Sep-10		
967	Programming Methods to Increase Window for Reverse Write 3D Cell	KR	2010-7001566	23-Jun-08				
968	Programming Methods to Increase Window for Reverse Write 3D Cell	TW	097123541	24-Jun-08				
969	Programming Methods to Increase Window for Reverse Write 3D Cell	WO	US08/007800	23-Jun-08	WO 09/002475	31-Dec-08		
970	Programming Methods to Increase Window for Reverse Write 3D Cell	US	11/819,077	25-Jun-07	2008-0007989	10-Jan-08	7,800,934	21-Sep-10
971	Method of Making High Forward Current Diodes for Reverse Write 3D Cell	CN	200880021393.7	23-Jun-08	CN101720485A	2-Jun-10		
972	Method of Making High Forward Current Diodes for Reverse Write 3D Cell	EP	08768726.5	23-Jun-08	2165336	24-Mar-10		
973	Method of Making High Forward Current Diodes for Reverse Write 3D Cell	JP	2010-513272	23-Jun-08	P2010-531543A	24-Sep-10		
974	Method of Making High Forward Current Diodes for Reverse Write 3D Cell	KR	2010-7001565	23-Jun-08				
975	Method of Making High Forward Current Diodes for Reverse Write 3D Cell	TW	097123542	24-Jun-08				
976	Method of Making High Forward Current Diodes for Reverse Write 3D Cell	WO	US08/007802	23-Jun-08	WO2009/002477	31-Dec-08		
977	Method of Making High Forward Current Diodes for Reverse Write 3D Cell	US	11/819,079	25-Jun-07	2008-0316796	25-Dec-08	7,684,226	23-Mar-10
978	High Forward Current Diodes for Reverse Write 3D Cell	US	11/819,078	25-Jun-07	2008-0316809	25-Dec-08	7,830,697	9-Nov-10
979	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	CN	200880022667.4	27-Jun-08	CN101720508A	2-Jun-10	ZL200880022667.4	23-May-12

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980	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	EP	08768806.5	27-Jun-08	2162917	17-Mar-10		
981	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	CN	201210124956.3	27-Jun-08			ZL201210124956.3	24-Dec-14
982	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	JP	2010-514823	27-Jun-08	2010-532568A	7-Oct-10		
983	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	KR	2009-7027300	27-Jun-08				
984	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	TW	097124406	27-Jun-08	200915543	1-Apr-09		
985	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	WO	US08/007985	27-Jun-08	WO2009/005699	8-Jan-09		
986	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	US	12/915,290	29-Oct-10	2011-0042639	24-Feb-11	8,173,486	8-May-12
987	Memory Cell that Employs a Selectively Grown Reversible Resistance-Switching Element and Methods of Forming the Same	US	13/964,157	12-Aug-13	2013-0320287	5-Dec-13	8,809,114	19-Aug-14
988	Memory Cell that Employs a Selectively Grown Reversible Resistance-Switching Element and Methods of Forming the Same	US	13/464,115	4-May-12	2012-0217462	30-Aug-12	8,507,315	13-Aug-13
989	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	US	11/772,082	29-Jun-07	2009-0001342	1-Jan-09	7,824,956	2-Nov-10
990	Memory Cell that Employs a Selectively Grown Reversible Resistance-Switching Element and Methods of Forming the Same	US	13/037,591	1-Mar-11	2011-0147693	23-Jun-11	8,373,150	12-Feb-13
991	Memory Cell that Employs a Selectively Grown Reversible Resistance-Switching Element and Methods of Forming the Same	US	13/764,065	11-Feb-13	2013-0146832	13-Jun-13	8,816,315	26-Aug-14
992	Memory Cell that Employs a Selectively Grown Reversible-Switching Element and Methods of Forming the Same	US	11/772,088	29-Jun-07	2009-0001344	1-Jan-09	7,902,537	8-Mar-11
993	Semiconductor Structures	US	12/872,468	31-Aug-10	2012-0049186	1-Mar-12		
994	Test Structure, Test Structure Formation and Mask Reuse in Semiconductor Processing	CN	200880022858.0.	26-Jun-08			ZL200880022858.0.	29-Feb-12
995	Test Structure, Test Structure Formation and Mask Reuse in Semiconductor Processing	KR	2009-7027314	26-Jun-08				

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996	Test Structure Formation in Semicondutor Processing	TW	097124580	30-Jun-08	200903687	16-Jan-09		
997	Test Structure, Test Structure Formation and Mask Reuse in Semiconductor Processing	WO	US08/068273	26-Jun-08	WO2009/006175	8-Jan-09		
998	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	CN	200880022647.7	27-Jun-08	CN101720506A	2-Jun-10	ZL200880022647.7	16-May-12
999	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	DE	08779800.5	27-Jun-08	2162916	17-Mar-10	2162916	20-Mar-13
1000	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	EP	08779800.5	27-Jun-08	2162916	17-Mar-10	2162916	20-Mar-13
1001	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	FR	08779800.5	27-Jun-08	2162916	17-Mar-10	2162916	20-Mar-13
1002	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	GB	08779800.5	27-Jun-08	2162916	17-Mar-10	2162916	20-Mar-13
1003	Method of Forming a Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element	DE	121664619	27-Jun-08			2485258	26-Mar-14
1004	Method of Forming a Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element	EP	12166461.9	27-Jun-08			2485258	26-Mar-14
1005	Method of Forming a Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element	GB	121664619	27-Jun-08			2485258	26-Mar-14
1006	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	KR	2014-7008191	27-Jun-08				
1007	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	KR	2014-7008185	27-Jun-08			10-1494335	11-Feb-15
1008	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	JP	2010-514824	27-Jun-08	P2010-532569A	7-Oct-10	5624463	3-Oct-14
1009	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	KR	2009-7027303	27-Jun-08			10-1447176	26-Sep-14
1010	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	NL	08779800.5	27-Jun-08	2162916	17-Mar-10	2162916	20-Mar-13

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1011	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	TW	097124473	27-Jun-08	200913171	16-Mar-09	I433276	1-Apr-14
1012	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	WO	US08/007986	27-Jun-08	WO2009/005700	8-Jan-09		
1013	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	US	11/772,090	29-Jun-07	2009-0001345	1-Jan-09	7,846,785	7-Dec-10
1014	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	US	13/556,312	24-Jul-12	2012-0286233	15-Nov-12	8,913,417	16-Dec-14
1015	Memory Cell that Employs a Selectively Deposited Reversible Resistance-Switching Element and Methods of Forming the Same	US	11/772,084	29-Jun-07	2009-0001343	1-Jan-09	8,233,308	31-Jul-12
1016	Method to Form a Rewriteable Memory Cell Comprising a Diode and a Resistivity-Switching Grown Oxide	TW	097124467	27-Jun-08	200915540	1-Apr-09		
1017	Method to Form a Rewriteable Memory Cell Comprising a Diode and a Resistivity-Switching Grown Oxide	WO	US08/07992	27-Jun-08	WO2009/005706	8-Jan-09		
1018	Method to Form a Rewriteable Memory Cell Comprising a Diode and a Resistivity-Switching Grown Oxide	US	11/772,081	29-Jun-07				
1019	Methods and Apparatus for Extending the Effective Thermal Operating Range of a Memory	US	11/772,103	29-Jun-07	2009-0003110	1-Jan-09	7,656,734	2-Feb-10
1020	Methods and Apparatus for Extending the Effective Thermal Operating Range of a Memory	US	13/205,820	9-Aug-11	2011-0292751	1-Dec-11	8,531,904	10-Sep-13
1021	Methods and Apparatus for Extending the Effective Thermal Operating Range of a Memory	US	12/828,846	1-Jul-10	2010-0271894	28-Oct-10	8,004,919	23-Aug-11
1022	Methods and Apparatus for Extending the Effective Thermal Operating Range of a Memory	US	11/772,097	29-Jun-07	2009-0003109	1-Jan-09	7,773,446	10-Aug-10
1023	Forming Complimentary Metal Features Using Conformal Insulator Layer	CN	200880022789.3	27-Jun-08	CN101730928A	9-Jun-10	ZL200880022789.3	27-Jul-11
1024	Forming Complimentary Metal Features Using Conformal Insulator Layer	KR	2010-7001617	27-Jun-08				
1025	Forming Complimentary Metal Features Using Conformal Insulator Layer	TW	097123943	26-Jun-08	200917368	16-Apr-09	I371798	1-Sep-12
1026	Forming Complimentary Metal Features Using Conformal Insulator Layer	WO	US08/068499	27-Jun-08	WO2009/006263	8-Jan-09		

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1027	Forming Complimentary Metal Features Using Conformal Insulator Layer	US	11/771,137	29-Jun-07	2009-0004844	1-Jan-09	7,927,990	19-Apr-11
1028	Method of Making Memory Cell with Voltage Modulated Sidewall Polyresistor	US	11/819,561	28-Jun-07	2009-0003082	1-Jan-09	7,701,746	20-Apr-10
1029	Memory Cell with Voltage Modulated Sidewall Polyresistor	US	11/819,562	28-Jun-07				
1030	Nonvolatile Memory Cell Without a Dielectric Antifuse Having High- and Low-Impedance States	US	11/819,595	28-Jun-07	2008-0013364	17-Jan-08	7,660,181	9-Feb-10
1031	Nonvolatile Memory Cell With Embedded Antifuse	US	11/819,618	28-Jun-07			8,008,700	30-Aug-11
1032	3D R/W Cell with Diode and Resistive Semiconductor Element and Method of Making Thereof	CN	200880024858.4	23-Jun-08			ZL200880024858.4	24-Jul-13
1033	Method of Making 3D R/W Cell with Reduced Reverse Leakage	EP	08779718.9	23-Jun-08	2165337	24-Mar-10		
1034	3D R/W Cell with Reduced Reverse Leakage and Method of Making Thereof	JP	2010-514766	23-Jun-08	P2010-532564A	7-Oct-10	5695417	13-Feb-15
1035	Method of Making 3D R/W Cell with Reduced Reverse Leakage	KR	2010-7001752	23-Jun-08				
1036	Method of Making 3D R/W Cell with Reduced Reverse Leakage	TW	097124455	24-Jun-08	200908205	16-Feb-09		
1037	Method of Making 3D R/W Cell with Reduced Reverse Leakage	WO	US08/007758	23-Jun-08	WO 09/005614	8-Jan-09		
1038	Method of Making 3D R/W Cell with Reduced Reverse Leakage	US	11/819,895	29-Jun-07	2009-0003036	1-Jan-09	7,800,939	21-Sep-10
1039	3D R/W Cell with Reduced Reverse Leakage	US	11/819,989	29-Jun-07	2009-0001347	1-Jan-09	7,759,666	20-Jul-10
1040	Method for Fabricating a 3-D Integrated Circuit using a Hard Mask of Silicon-Oxynitride on Amorphous Carbon	CN	200880022217.5	26-Jun-08	CN101743626A	16-Jun-10	ZL200880022217.5	30-Jan-13
1041	Method for Fabricating a 3-D Integrated Circuit using a Hard Mask of Silicon-Oxynitride on Amorphous Carbon	KR	2010-7001615	26-Jun-08				
1042	Method for Fabricating a 3-D Integrated Circuit using a Hard Mask of Silicon-Oxynitride on Amorphous Carbon	TW	097123944	26-Jun-08	200915495	1-Apr-09	I393221	11-Apr-13
1043	Method for Fabricating a 3-D Integrated Circuit using a Hard Mask of Silicon-Oxynitride on Amorphous Carbon	WO	US08/068307	26-Jun-08	WO2009/003091	31-Dec-08		
1044	Method for Fabricating a 3-D Integrated Circuit using a Hard Mask of Silicon-Oxynitride on Amorphous Carbon	US	12/750,596	30-Mar-10	2010-0184259	22-Jul-10	7,994,068	9-Aug-11

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1045	Method for Fabricating a 3-D Integrated Circuit using a Hard Mask of Silicon-Oxynitride on Amorphous Carbon	US	11/769,027	27-Jun-07	2009-0004786	1-Jan-09	7,718,546	18-May-10
1046	Dual-Damascene with Amorphous Carbon for 3D Deep VIA/Trench Application	US	11/864,759	28-Sep-07	2009-0087979	2-Apr-09	8,298,931	30-Oct-12
1047	METHOD FOR REDUCING PILLAR STRUCTURE DIMENSIONS OF A SEMICONDUCTOR DEVICE	TW	097137350	26-Sep-08				
1048	METHOD FOR REDUCING PILLAR STRUCTURE DIMENSIONS OF A SEMICONDUCTOR DEVICE	US	11/864,205	28-Sep-07	2009-0087963	2-Apr-09	7,682,942	23-Mar-10
1049	METHOD FOR REDUCING PILLAR STRUCTURE DIMENSIONS OF A SEMICONDUCTOR DEVICE	WO	US08/011215	26-Sep-08	WO2009/045347	9-Apr-09		
1050	Liner for Tungsten/Silicon Dioxide Interface In Memory	CN	200880117519.0	26-Sep-08			ZL200880117519.0	31-Oct-12
1051	Liner for Tungsten/Silicon Dioxide Interface In Memory	DE	088361456	26-Sep-08	2191508	2-Jun-10	2191508	29-Jun-11
1052	Liner for Tungsten/Silicon Dioxide Interface In Memory	EP	08836145.6	26-Sep-08	2191508	2-Jun-10	2191508	29-Jun-11
1053	Liner for Tungsten/Silicon Dioxide Interface In Memory	FR	088361456	26-Sep-08	2191508	2-Jun-10	2191508	29-Jun-11
1054	Liner for Tungsten/Silicon Dioxide Interface In Memory	GB	088361456	26-Sep-08	2191508	2-Jun-10	2191508	29-Jun-11
1055	Liner for Tungsten/Silicon Dioxide Interface In Memory	JP	2010-526964	26-Sep-08	P2010-541004A	24-Dec-10	4995968	18-May-12
1056	Liner for Tungsten/Silicon Dioxide Interface In Memory	KR	2010-7007262	26-Sep-08			10-1472754	9-Dec-14
1057	Liner for Tungsten/Silicon Dioxide Interface In Memory	NL	088361456	26-Sep-08	2191508	2-Jun-10	2191508	29-Jun-11
1058	Liner for Tungsten/Silicon Dioxide Interface In Memory	TW	097137351	26-Sep-08	200931641	16-Jul-09		
1059	Liner for Tungsten/Silicon Dioxide Interface In Memory	US	11/863,734	28-Sep-07	2009-0085087	2-Apr-09	8,071,475	6-Dec-11
1060	Liner for Tungsten/Silicon Dioxide Interface In Memory	WO	US08/011216	26-Sep-08	WO09/045348	9-Apr-09		
1061	Diode Array and Method of Making Thereof	US	12/949,056	18-Nov-10	2011-0065243	17-Mar-11	8,268,678	18-Sep-12
1062	Diode Array and Method of Making Thereof	US	11/864,532	28-Sep-07	2009-0085153	2-Apr-09	7,846,782	7-Dec-10
1063	VERTICAL DIODE BASED MEMORY CELLS HAVING A LOWERED PROGRAMMING VOLTAGE AND METHODS OF FORMING THE SAME	CN	200880118435.9	26-Sep-08	CN101878531A	3-Nov-10		
1064	VERTICAL DIODE BASED MEMORY CELLS HAVING A LOWERED PROGRAMMING VOLTAGE AND METHODS OF FORMING THE SAME	EP	08836291.8	26-Sep-08	2193545	9-Jun-10		

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1065	VERTICAL DIODE BASED MEMORY CELLS HAVING A LOWERED PROGRAMMING VOLTAGE AND METHODS OF FORMING THE SAME	JP	2010-527205	26-Sep-08	P2010-541253A	24-Dec-10		
1066	VERTICAL DIODE BASED MEMORY CELLS HAVING A LOWERED PROGRAMMING VOLTAGE AND METHODS OF FORMING THE SAME	KR	2010-7006803	26-Sep-08				
1067	VERTICAL DIODE BASED MEMORY CELLS HAVING A LOWERED PROGRAMMING VOLTAGE AND METHODS OF FORMING THE SAME	TW	097137501	26-Sep-08	200939397	16-Sep-09		
1068	VERTICAL DIODE BASED MEMORY CELLS HAVING A LOWERED PROGRAMMING VOLTAGE AND METHODS OF FORMING THE SAME	US	11/864,848	28-Sep-07	2009-0085154	2-Apr-09	8,349,663	8-Jan-13
1069	VERTICAL DIODE BASED MEMORY CELLS HAVING A LOWERED PROGRAMMING VOLTAGE AND METHODS OF FORMING THE SAME	WO	US08/077960	26-Sep-08	WO2009/045920			
1070	METHODS AND APPARATUS FOR COST-EFFECTIVELY INCREASING FEATURE DENSITY USING A MASK SHRINKING PROCESS WITH DOUBLE PATTERNING	US	11/864,901	28-Sep-07	2009-0087993	2-Apr-09		
1071	MULTIPLE ANTIFUSE MEMORY CELLS AND METHODS TO FORM, PROGRAM, AND SENSE THE SAME	CN	200880118438.2	26-Sep-08	CN101878508A	3-Nov-10		
1072	MULTIPLE ANTIFUSE MEMORY CELLS AND METHODS TO FORM, PROGRAM, AND SENSE THE SAME	EP	08833455.2	26-Sep-08	2203919	7-Jul-10		
1073	MULTIPLE ANTIFUSE MEMORY CELLS AND METHODS TO FORM, PROGRAM, AND SENSE THE SAME	JP	2010-527201	26-Sep-08	P2010-541252A	24-Dec-10		
1074	MULTIPLE ANTIFUSE MEMORY CELLS AND METHODS TO FORM, PROGRAM, AND SENSE THE SAME	KR	2010-7006799	26-Sep-08				
1075	MULTIPLE ANTIFUSE MEMORY CELLS AND METHODS TO FORM, PROGRAM, AND SENSE THE SAME	TW	097137471	26-Sep-08	200935428	16-Aug-09		
1076	MULTIPLE ANTIFUSE MEMORY CELLS AND METHODS TO FORM, PROGRAM, AND SENSE THE SAME	US	11/864,870	28-Sep-07	2009-0086521	2-Apr-09		

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1077	MULTIPLE ANTIFUSE MEMORY CELLS AND METHODS TO FORM, PROGRAM, AND SENSE THE SAME	WO	US08/077943	26-Sep-08	WO2009/042913	2-Apr-09		
1078	Digital Content Kiosk and Methods for Use Therewith	TW	097136366	22-Sep-08				
1079	Digital Content Kiosk and Methods for Use Therewith	WO	US08/010732	15-Sep-08	WO09/058177	7-May-09		
1080	Method for Fabricating Pitch-Doubling Pillar Structures	TW	097145367	24-Nov-08				
1081	Method for Fabricating Pitch-Doubling Pillar Structures	US	12/000,758	17-Dec-07	2009-0155962	18-Jun-09	7,759,201	20-Jul-10
1082	Method for Fabricating Pitch-Doubling Pillar Structures	WO	US08/012476	5-Nov-08	WO09/078896	25-Jun-09		
1083	Three Dimensional Hexagonal Matrix Memory Array	US	14/291,415	30-May-14				
1084	Three Dimensional Hexagonal Matrix Memory Array	US	12/801,504	11-Jun-10	2010-0290262	18-Nov-10	8,107,270	31-Jan-12
1085	Three Dimensional Hexagonal Matrix Memory Array and Method of Manufacturing the Same	CN	200880127585.6	5-Nov-08	CN101971336A	9-Feb-11	ZL200880127585.6	30-Jul-14
1086	Three Dimensional Hexagonal Matrix Memory Array	EP	08867796.8	5-Nov-08				
1087	Three Dimensional Hexagonal Matrix Memory Array	JP	2010-540629	5-Nov-08	P2011-508973A	17-Mar-11		
1088	Three Dimensional Hexagonal Matrix Memory Array	KR	2010-7015864	5-Nov-08				
1089	Three Dimensional Hexagonal Matrix Memory Array	TW	097145364	6-Nov-08				
1090	Three Dimensional Hexagonal Matrix Memory Array	US	12/005,346	27-Dec-07	2009-0168480	2-Jul-09	7,746,680	29-Jun-10
1091	Three Dimensional Hexagonal Matrix Memory Array	WO	US08/012481	5-Nov-08	WO09/085078	9-Jul-09		
1092	Method of Making a Pillar Pattern Using Triple or Quadruple Exposure	EP	08867215.9	5-Nov-08	2279453	2-Feb-11		
1093	Method of Making a Pillar Pattern Using Triple or Quadruple Exposure	TW	097145365	6-Nov-08	200931497	16-Jul-09		
1094	Method of Making a Pillar Pattern Using Triple or Quadruple Exposure	US	12/005,276	27-Dec-07	2009-0170030	2-Jul-09	7,887,999	15-Feb-11
1095	Method of Making a Pillar Pattern Using Triple or Quadruple Exposure	WO	US08/012480	5-Nov-08	WO09/085077	9-Jul-09		
1096	Large Capacity One-Time Programmable Memory Cell using Metal Oxides	CN	200880122646.X	5-Nov-08	CN101911206A	8-Dec-10	ZL200880122646.X	2-Apr-14
1097	Large Capacity One-Time Programmable Memory Cell using Metal Oxides	DE	08867812.3	5-Nov-08	2232499	29-Sep-10	2232499	16-Jul-14

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1098	Large Capacity One-Time Programmable Memory Cell using Metal Oxides	EP	08867812.3	5-Nov-08	2232499	29-Sep-10	2232499	16-Jul-14
1099	Large Capacity One-Time Programmable Memory Cell using Metal Oxides	GB	08867812.3	5-Nov-08	2232499	29-Sep-10	2232499	16-Jul-14
1100	Large Capacity One-Time Programmable Memory Cell using Metal Oxides	JP	2010-540628	5-Nov-08	P2011-508360A	10-Mar-11	5190520	1-Feb-13
1101	Large Capacity One-Time Programmable Memory Cell using Metal Oxides	KR	2010-7015687	5-Nov-08				
1102	Large Capacity One-Time Programmable Memory Cell using Metal Oxides	TW	097145368	24-Nov-08				
1103	Large Capacity One-Time Programmable Memory Cell using Metal Oxides	US	12/005,277	27-Dec-07		2-Jul-09	7,706,169	27-Apr-10
1104	Large Capacity One-Time Programmable Memory Cell using Metal Oxides	WO	US08/012478	5-Nov-08	WO09/085076	9-Jul-09		
1105	Method of Programming Cross-Point Diode Memory Array	TW	097145487	6-Nov-08				
1106	Method of Programming Cross-Point Diode Memory Array	US	12/003,571	28-Dec-07	2009-0168507	2-Jul-09	7,706,177	27-Apr-10
1107	Method of Programming Cross-Point Diode Memory Array	WO	US08/012482	5-Nov-08	WO09/085079	9-Jul-09		
1108	Two Terminal Non-Volatile Memory Using Gate Controlled Diode Element	TW	097145479	25-Nov-08				
1109	Two Terminal Non-Volatile Memory Using Gate Controlled Diode Elements	US	12/003,570	28-Dec-07	2009-0168492	2-Jul-09	7,764,534	27-Jul-10
1110	Two Terminal Non-Volatile Memory Using Gate Controlled Diode Element	WO	US08/012477	5-Nov-08	WO09/085075	9-Jul-09		
1111	METHODS AND APPARATUS FOR FORMING MEMORY LINES AND VIAS IN THREE DIMENSIONAL MEMORY ARRAYS USING DUAL DAMASCENE PROCESS AND IMPRINT LITHOGRAPHY	CN	200880123672.4	31-Dec-08	CN101919046A	15-Dec-10	ZL200880123672.4	6-Nov-13
1112	METHODS AND APPARATUS FOR FORMING MEMORY LINES AND VIAS IN THREE DIMENSIONAL MEMORY ARRAYS USING DUAL DAMASCENE PROCESS AND IMPRINT LITHOGRAPHY	EP	08870141.2	31-Dec-08	2227823	5-Apr-12		
1113	APPARATUS FOR FORMING MEMORY LINES AND VIAS IN THREE DIMENSIONAL MEMORY ARRAYS USING DUAL DAMASCENE PROCESS AND IMPRINT LITHOGRAPHY	US	13/911,294	6-Jun-13	2013-0264675	10-Oct-13		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1114	METHODS AND APPARATUS FOR FORMING MEMORY LINES AND VIAS IN THREE DIMENSIONAL MEMORY ARRAYS USING DUAL DAMASCENE PROCESS AND IMPRINT LITHOGRAPHY	JP	2010-540951	31-Dec-08	P2011-508459A	10-Mar-11		
1115	METHODS AND APPARATUS FOR FORMING MEMORY LINES AND VIAS IN THREE DIMENSIONAL MEMORY ARRAYS USING DUAL DAMASCENE PROCESS AND IMPRINT LITHOGRAPHY	KR	2010-7013806	31-Dec-08				
1116	METHODS AND APPARATUS FOR FORMING MEMORY LINES AND VIAS IN THREE DIMENSIONAL MEMORY ARRAYS USING DUAL DAMASCENE PROCESS AND IMPRINT LITHOGRAPHY	TW	097151904	31-Dec-08	200943491	16-Oct-09		
1117	METHODS AND APPARATUS FOR FORMING MEMORY LINES AND VIAS IN THREE DIMENSIONAL MEMORY ARRAYS USING DUAL DAMASCENE PROCESS AND IMPRINT LITHOGRAPHY	US	11/967,638	31-Dec-07	2009-0166682	2-Jul-09	8,466,068	18-Jun-13
1118	METHODS AND APPARATUS FOR FORMING MEMORY LINES AND VIAS IN THREE DIMENSIONAL MEMORY ARRAYS USING DUAL DAMASCENE PROCESS AND IMPRINT LITHOGRAPHY	WO	US08/088628	31-Dec-08	WO2009/088922	24-Sep-09		
1119	Storage Sub-System for a Computer Comprising Write-Once Memory Devices and Write-Many Memory Devices and Related Method	US	13/616,986	14-Sep-12	2013-0013847	10-Jan-13	9,152,562	6-Oct-15
1120	Storage Sub-System for a Computer Comprising Write-Once Memory Devices and Write-Many Memory Devices and Related Method	CN	200880123684.7	31-Dec-08			ZL200880123684.7	28-May-14
1121	Storage Sub-System for a Computer Comprising Write-Once Memory Devices and Write-Many Memory Devices and Related Method	EP	08869429.4	31-Dec-08	2227746	15-Sep-10		
1122	Storage Sub-System for a Computer Comprising Write-Once Memory Devices and Write-Many Memory Devices and Related Method	JP	2010-540949	31-Dec-08	P2011-514568A	6-May-11		

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1123	Storage Sub-System for a Computer Comprising Write-Once Memory Devices and Write-Many Memory Devices and Related Method	KR	2010-7013891	31-Dec-08				
1124	Storage Sub-System for a Computer Comprising Write-Once Memory Devices and Write-Many Memory Devices and Related Method	TW	097151672	31-Dec-08	200937191	1-Sep-09		
1125	Storage Sub-System for a Computer Comprising Write-Once Memory Devices and Write-Many Memory Devices and Related Method	US	11/967,987	31-Dec-07	2009-0172321	2-Jul-09	8,275,927	25-Sep-12
1126	Storage Sub-System for a Computer Comprising Write-Once Memory Devices and Write-Many Memory Devices and Related Method	WO	US08/088616	31-Dec-08	WO2009/088914			
1127	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	US	13/235,409	18-Sep-11	2012-0001150	5-Jan-12	8,878,235	4-Nov-14
1128	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	WO	US12/54571	11-Sep-12	WO2013/066496	10-May-13		
1129	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	CN	200880123685.1	30-Dec-08	CN101919047A	15-Dec-10	ZL200880123685.1	10-Jul-13
1130	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	DE	08869555.6	30-Dec-08	2227824	15-Sep-10	2227824	16-Apr-14
1131	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	EP	08869555.6	30-Dec-08	2227824	15-Sep-10	2227824	16-Apr-14
1132	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	GB	08869555.6	30-Dec-08	2227824	15-Sep-10	2227824	16-Apr-14
1133	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	JP	2010-540945	30-Dec-08	P2011-508458A	10-Mar-11		

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1134	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	KR	2010-7013893	30-Dec-08			10-1494746	12-Feb-15
1135	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	TW	097151907	31-Dec-08	200943489	16-Oct-09		
1136	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	US	11/968,154	31-Dec-07	2009-0168491	2-Jul-09	8,236,623	7-Aug-12
1137	Memory Cell that employs a selectively fabricated Carbon Nano-Tube Reversible Resistance-Switching Element and Methods of Forming the Same	WO	US08/088584	30-Dec-08	WO2009/088888	17-Sep-09		
1138	MEMORY CELL THAT EMPLOYS A SELECTIVELY FABRICATED CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT FORMED OVER A BOTTOM CONDUCTOR AND METHODS OF FORMING THE SAME	CN	200880123671.X	30-Dec-08	CN101919056A	15-Dec-10	ZL200880123671.X	18-Jul-12
1139	MEMORY CELL THAT EMPLOYS A SELECTIVELY FABRICATED CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT FORMED OVER A BOTTOM CONDUCTOR AND METHODS OF FORMING THE SAME	EP	08869246.2	30-Dec-08	2227827	15-Sep-10		
1140	MEMORY CELL THAT EMPLOYS A SELECTIVELY FABRICATED CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT FORMED OVER A BOTTOM CONDUCTOR AND METHODS OF FORMING THE SAME	JP	2010-540946	30-Dec-08	P2011-508979A	17-Mar-11		
1141	MEMORY CELL THAT EMPLOYS A SELECTIVELY FABRICATED CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT FORMED OVER A BOTTOM CONDUCTOR AND METHODS OF FORMING THE SAME	KR	2010-7014266	30-Dec-08				
1142	MEMORY CELL THAT EMPLOYS A SELECTIVELY FABRICATED CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT FORMED OVER A BOTTOM CONDUCTOR AND METHODS OF FORMING THE SAME	TW	097151905	31-Dec-08	200943488	16-Oct-09		

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1143	MEMORY CELL THAT EMPLOYS A SELECTIVELY FABRICATED CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT FORMED OVER A BOTTOM CONDUCTOR AND METHODS OF FORMING THE SAME	US	11/968,156	31-Dec-07	2009-0166609	2-Jul-09	8,558,220	15-Oct-13
1144	MEMORY CELL THAT EMPLOYS A SELECTIVELY FABRICATED CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT FORMED OVER A BOTTOM CONDUCTOR AND METHODS OF FORMING THE SAME	WO	US08/088585	30-Dec-08				
1145	MEMORY CELL WITH PLANARIZED CARBON NANOTUBE LAYER AND METHODS OF FORMING THE SAME	CN	200880123686.6	30-Dec-08	CN101919048A	15-Dec-10		
1146	MEMORY CELL WITH PLANARIZED CARBON NANOTUBE LAYER AND METHODS OF FORMING THE SAME	EP	08870041.4	30-Dec-08	2227825	15-Sep-10		
1147	MEMORY CELL WITH PLANARIZED CARBON NANOTUBE LAYER AND METHODS OF FORMING THE SAME	JP	2010-540947	30-Dec-08	P2011-508980A	17-Mar-11		
1148	MEMORY CELL WITH PLANARIZED CARBON NANOTUBE LAYER AND METHODS OF FORMING THE SAME	KR	2010-7014557	30-Dec-08				
1149	MEMORY CELL WITH PLANARIZED CARBON NANOTUBE LAYER AND METHODS OF FORMING THE SAME	TW	097151866	31-Dec-08	200943487	16-Oct-09		
1150	MEMORY CELL WITH PLANARIZED CARBON NANOTUBE LAYER AND METHODS OF FORMING THE SAME	US	11/968,159	31-Dec-07	2009-0166610	2-Jul-09		
1151	MEMORY CELL WITH PLANARIZED CARBON NANOTUBE LAYER AND METHODS OF FORMING THE SAME	WO	US08/088586	30-Dec-08	WO2009/088890	17-Sep-09		
1152	Method of Fabricating a Self Aligning Damascene Memory Structure	US	12/611,087	2-Nov-09	2010-0044756	25-Feb-10	8,389,399	5-Mar-13
1153	Method of Fabricating a Self Aligning Damascene Memory Structure	US	13/781,983	1-Mar-13	2013-0175675	11-Jul-13	8,633,105	21-Jan-14
1154	Method of Fabricating a Self Aligning Damascene Memory Structure	CN	200880019869.3	10-Apr-08			ZL200880019869.3	21-Mar-12
1155	Method of Fabricating a Self Aligning Damascene Memory Structure	US	14/140,468	24-Dec-13	2014-0117514	1-May-14	9,082,786	14-Jul-15
1156	Method of Fabricating a Self Aligning Damascene Memory Structure	EP	08727325.6	10-Apr-08	2135283	23-Dec-09		
1157	Method of Fabricating a Self Aligning Damascene Memory Structure	JP	2010-503065	10-Apr-08	P2010-524258A	15-Jul-10		

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1158	Method of Fabricating a Self Aligning Damascene Memory Structure	KR	2009-7021152	10-Apr-08				
1159	Method of Fabricating a Self Aligning Damascene Memory Structure	TW	097113343	11-Apr-08	200901393	1-Jan-09		
1160	Method of Fabricating a Self Aligning Damascene Memory Structure	US	11/786,620	12-Apr-07	2008-0254576	16-Oct-08	7,629,247	8-Dec-09
1161	Method of Fabricating a Self Aligning Damascene Memory Structure	WO	US08/004665	10-Apr-08	WO2008/127628	23-Oct-08		
1162	Pillar Devices and Methods of Making Thereof	US	13/026,381	14-Feb-11	2011-0136326	9-Jun-11	8,987,119	24-Mar-15
1163	Pillar Devices and Methods of Making Thereof	CN	200980108243.4	14-Jan-09	CN101978497A	16-Feb-11		
1164	Pillar Devices and Methods of Making Thereof	KR	2010-7017757	14-Jan-09				
1165	Pillar Devices and Methods of Making Thereof	TW	098101267	14-Jan-09			I449131	11-Aug-14
1166	Pillar Devices and Methods of Making Thereof	US	12/007,781	15-Jan-08	2009-0179310	16-Jul-09	7,906,392	15-Mar-11
1167	Pillar Devices and Methods of Making Thereof	WO	US09/030937	14-Jan-09	WO09/091786	23-Jul-09		
1168	Selective Germanium Deposition for Pillar Devices	US	12/007,780	15-Jan-08	2009-0181515	16-Jul-09	7,745,312	29-Jun-10
1169	Damascene Integration Methods for Graphitic Films in Three-Dimensional Memories and Memories formed Therefrom	US	61/044,352	11-Apr-08				
1170	Damascene Integration Methods for Graphitic Films in Three-Dimensional Memories and Memories formed Therefrom	TW	098112099	10-Apr-09	201001695	1-Jan-10		
1171	Damascene Integration Methods for Graphitic Films in Three-Dimensional Memories and Memories formed Therefrom	US	12/421,405	9-Apr-09	2009-0257270	15-Oct-09	8,467,224	18-Jun-13
1172	Damascene Integration Methods for Graphitic Films in Three-Dimensional Memories and Memories formed Therefrom	WO	US09/040128	9-Apr-09	WO09/126846	15-Oct-09		
1173	Carbon Based Switching Element for Three Dimensional Memory	US	61/044,187	11-Apr-08				
1174	Multilevel Nonvolatile Memory Device Containing a Carbon Storage Material and Methods of Making and Using Same	US	61/071,092	11-Apr-08				
1175	Multilevel Nonvolatile Memory Device Containing a Carbon Storage Material and Methods of Making and usng Same	TW	098112109	10-Apr-09				

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1176	Multilevel Nonvolatile Memory Device Containing a Carbon Storage Material and Methods of Making and usng Same	US	12/153,872	27-May-08	2009-0257265	15-Oct-09	7,830,698	9-Nov-10
1177	Multilevel Nonvolatile Memory Device Containing a Carbon Storage Material and Methods of Making and usng Same	WO	US09/039120	1-Apr-09				
1178	Double patterning method	US	13/155,754	8-Jun-11	2011-0236833	29-Sep-11	8,178,286	15-May-12
1179	Double patterning method	US	61/071,091	11-Apr-08				
1180	Double patterning method	TW	098112101	10-Apr-09				
1181	Double patterning method	US	12/222,293	6-Aug-08			7,981,592	19-Jul-11
1182	Double patterning method	WO	US09/039124	1-Apr-09				
1183	Multilevel Nonvolatile Memory Device Containing a Carbon Storage Material and Methods of Making and Using Same	US	61/071,090	11-Apr-08				
1184	Multilevel Nonvolatile Memory Device containing Carbon Storage Material and Methods of Making and Using the Same	US	12/153,873	27-May-08			7,859,887	28-Dec-10
1185	Method of Making Nonvolatile Memory Cell Containing Graphene as a Storage Element by Low Temperature Processing	US	61/071,088	11-Apr-08				
1186	Method of Making Nonvolatile Memory Cell Containing Graphene as a Storage Element by Low Temperature Processing	TW	098112070	10-Apr-09				
1187	Method of Making Nonvolatile Memory Cell Containing Carbon Resistivity Switching as a Storage Element by Low Temperature Processing	US	12/222,341	7-Aug-08	2009-0258135	15-Oct-09	8,048,474	1-Nov-11
1188	Method of Making Nonvolatile Memory Cell Containing Graphene as a Storage Element by Low Temperature Processing	WO	US09/39127	1-Apr-09				
1189	Multilevel Nonvolatile Memory Device Containing a Carbon Storage Material and Methods of Making and Using Same	US	61/071,093	11-Apr-08				
1190	Multilevel Nonvolatile Memory Device Containing a Carbon Storage Material and Methods of Making and Using Same	US	12/153,874	27-May-08	2009-0258489	15-Oct-09	7,723,180	25-May-10
1191	One-Time Programmable (OTP) Memory Device and Methods for Use Therewith	US	61/044,410	11-Apr-08				
1192	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	CN	200980120069.5	10-Apr-09			ZL200980120069.5	12-Jun-13

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1193	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	DE	09730256.6	10-Apr-09	2263257	22-Dec-10	2263257	8-Aug-12
1194	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	EP	09730256.6	10-Apr-09	2263257	22-Dec-10	2263257	8-Aug-12
1195	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	FR	09730256.6	10-Apr-09	2263257	22-Dec-10	2263257	8-Aug-12
1196	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	GB	09730256.6	10-Apr-09	2263257	22-Dec-10	2263257	8-Aug-12
1197	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	JP	2011-504201	10-Apr-09	P2011-517857A	16-Jun-11		
1198	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	KR	2010-7022338	10-Apr-09				
1199	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	NL	09730256.6	10-Apr-09	2263257	22-Dec-10	2263257	8-Aug-12
1200	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	US	61/044,406	11-Apr-08				
1201	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	TW	098112119	10-Apr-09	201001770	1-Jan-10		
1202	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	US	12/410,771	25-Mar-09	2009-0256130	15-Oct-09	8,304,284	6-Nov-12
1203	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element and Methods for Forming the Same	WO	US09/040189	10-Apr-09	WO2009/126876	15-Oct-09		

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1204	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	US	13/351,468	17-Jan-12	2012-0119178	17-May-12	8,536,015	17-Sep-13
1205	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	CN	200980122112.1	10-Apr-09	CN102067312A	18-May-11	ZL200980122112.1	30-Apr-14
1206	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	DE	09729975.4	10-Apr-09	2263256	22-Dec-10	2263256	21-Aug-13
1207	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	EP	09729975.4	10-Apr-09	2263256	22-Dec-10	2263256	21-Aug-13
1208	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	GB	09729975.4	10-Apr-09	2263256	22-Dec-10	2263256	21-Aug-13
1209	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	JP	2011-504199	10-Apr-09	P2011-517856A	16-Jun-11	5564035	20-Jun-14
1210	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	KR	2010-7022345	10-Apr-09				
1211	Thin deposited carbon switchable resistor and diode matrix cell for 3D arrays	US	61/044,399	11-Apr-08				
1212	A MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	TW	098112117	10-Apr-09				
1213	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	US	12/418,855	6-Apr-09	2009-0256132	15-Oct-09	8,110,476	7-Feb-12
1214	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	WO	US09/040183	10-Apr-09	WO2009/126871	15-Oct-09		
1215	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	CN	200980117208.9	10-Apr-09	CN102027610A	20-Apr-11	CN200980117208.9	5-Dec-12
1216	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	DE	097432090	10-Apr-09	2263273	22-Dec-10	2263273	16-May-12
1217	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	EP	09743209.0	10-Apr-09	2263273	22-Dec-10	2263273	16-May-12

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1218	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	FR	097432090	10-Apr-09	2263273	22-Dec-10	2263273	16-May-12
1219	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	GB	097432090	10-Apr-09	2263273	22-Dec-10	2263273	16-May-12
1220	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	JP	2011-504206	10-Apr-09	P2011-517123A	26-May-11	5469159	7-Feb-14
1221	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	KR	2010-7022549	10-Apr-09			10-1537518	13-Jul-15
1222	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	NL	097432090	10-Apr-09	2263273	22-Dec-10	2263273	16-May-12
1223	Damascene Integration Methods for Carbon Nano-Tube Films in in Non-Volatile Memories and Memories formed Therefrom	US	61/044,328	11-Apr-08				
1224	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	TW	098112118	10-Apr-09	201001629	1-Jan-10		
1225	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	US	12/421,823	10-Apr-09	2010-0072445	25-Mar-10	7,977,667	12-Jul-11
1226	MEMORY CELL THAT INCLUDES A CARBON NANO-TUBE REVERSIBLE RESISTANCE-SWITCHING ELEMENT AND METHODS OF FORMING THE SAME	WO	US09/040222	10-Apr-09	WO09/137222	12-Nov-09		
1227	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	CN	200980122308.0	10-Apr-09	CN102067292A	18-May-11	ZL200980122308.0	14-Aug-13
1228	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	DE	09730879.5	10-Apr-09	2263252	22-Dec-10	2263252	9-Oct-13
1229	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	EP	09730879.5	10-Apr-09	2263252	22-Dec-10	2263252	9-Oct-13
1230	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	GB	09730879.5	10-Apr-09	2263252	22-Dec-10	2263252	9-Oct-13

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1231	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	JP	2011-504204	10-Apr-09	2011-520249	14-Jul-11		
1232	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	KR	2010-7022552	10-Apr-09				
1233	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	US	61/044,314	11-Apr-08				
1234	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	TW	098112126	10-Apr-09	201007836	16-Feb-10		
1235	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	US	12/421,803	10-Apr-09	2009-0278112	12-Nov-09	8,445,385	21-May-13
1236	Methods for Etching Carbon Nano-Tube Films in Non-Volatile Memories	WO	US09/040215	10-Apr-09	WO2009/126891	15-Oct-09		
1237	NONVOLATILE MEMORY ARRAY COMPRISING SILICON-BASED DIODES FABRICATED AT LOW TEMPERATURE	TW	099115014	11-May-10	201112399	1-Apr-11		
1238	NONVOLATILE MEMORY ARRAY COMPRISING SILICON-BASED DIODES FABRICATED AT LOW TEMPERATURE	US	12/463,530	11-May-09	2010-0283053	11-Nov-10		
1239	NONVOLATILE MEMORY ARRAY COMPRISINGSILICON-BASED DIODES FABRICATED AT LOW TEMPERATURE	WO	US10/034210	10-May-10	WO2010/132346	18-Nov-10		
1240	Methods and Apparatus for Forming Line and Pillar Structures for Three Dimensional Memory Arrays using Double Subtractive Process and Imprint Lithography	TW	100128978	12-Aug-11	201234565	16-Aug-12		
1241	Methods and Apparatus for Forming Line and Pillar Structures for Three Dimensional Memory Arrays using Double Subtractive Process and Imprint Lithography	US	12/856,392	13-Aug-10				
1242	Methods and Apparatus for Forming Line and Pillar Structures for Three Dimensional Memory Arrays using Double Subtractive Process and Imprint Lithography	WO	US11/046904	8-Aug-11	WO2012/021433	16-Feb-12		
1243	Shared Masks for X-Lines and Shared Masks for Y-Lines for Fabrication of 3D Memory Arrays	CN	200980135327.7	3-Sep-09	CN102150267	10-Aug-11	ZL200980135327.7	12-Mar-14
1244	Shared Masks for X-Lines and Shared Masks for Y-Lines for Fabrication of 3D Memory Arrays	DE	09792218.1	3-Sep-09	2335284	22-Jun-11	2335284	2-Dec-15
1245	Shared Masks for X-Lines and Shared Masks for Y-Lines for Fabrication of 3D Memory Arrays	EP	09792218.1	3-Sep-09	2335284	22-Jun-11	2335284	2-Dec-15

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1246	Shared Masks for X-Lines and Shared Masks for Y-Lines for Fabrication of 3D Memory Arrays	JP	2011-526189	3-Sep-09	2012-502480	26-Jan-12	5129391	9-Nov-12
1247	Shared Masks for X-Lines and Shared Masks for Y-Lines for Fabrication of 3D Memory Arrays	KR	2011-7006681	3-Sep-09			10-1501105	4-Mar-15
1248	THREE DIMENSIONAL SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	TW	098130243	8-Sep-09			I382417	11-Jan-13
1249	Shared Masks for X-Lines and Shared Masks for Y-Lines for Fabrication of 3D Memory Arrays	US	12/231,000	9-Sep-08	2010-0059796	11-Mar-10	7,943,515	17-May-11
1250	Shared Masks for X-Lines and Shared Masks for Y-Lines for Fabrication of 3D Memory Arrays	WO	US09/055850	3-Sep-09	WO2010/030555	18-Mar-10		
1251	Apparatus and Methods of Forming Memory Lines and Structures using Double Sidewall Patterning for Four Times Half Pitch Relief Patterning	CN	201080059446.1	26-Oct-10			ZL201080059446.1	12-Aug-15
1252	Apparatus and Methods of Forming Memory Lines and Structures using Double Sidewall Patterning for Four Times Half Pitch Relief Patterning	EP	10774374.2	26-Oct-10	2494586	5-Sep-12		
1253	Apparatus and Methods of Forming Memory Lines and Structures using Double Sidewall Patterning for Four Times Half Pitch Relief Patterning	JP	2012-535449	26-Oct-10	2013-508986	7-Mar-13		
1254	Apparatus and Methods of Forming Memory Lines and Structures using Double Sidewall Patterning for Four Times Half Pitch Relief Patterning	KR	2012-7011118	26-Oct-10				
1255	Double Sidewall Patterning for 4x Half Pitch Relief Patterning	US	61/255,080	26-Oct-09				
1256	Apparatus and Methods of Forming Memory Lines and Structures using Double Sidewall Patterning for Four Times Half Pitch Relief Patterning	TW	099136568	26-Oct-10	201126651	1-Aug-11		
1257	Apparatus and Methods of Forming Memory Lines and Structures using Double Sidewall Patterning for Four Times Half Pitch Relief Patterning	US	12/911,887	26-Oct-10	2011-0095434	28-Apr-11	8,679,967	25-Mar-14

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1258	Apparatus and Methods of Forming Memory Lines and Structures using Double Sidewall Patterning for Four Times Half Pitch Relief Patterning	WO	US10/054017	26-Oct-10	WO11/056529	12-May-11		
1259	Methods and Apparatus for Layout of Three Dimensional Matrix Array Memory for Reduced Cost Patterning	US	14/334,653	17-Jul-14	2014-0328105	6-Nov-14	8,969,923	3-Mar-15
1260	Layout of 3D Matrix Array Memory for Reduced Cost Patterning	US	61/255,085	26-Oct-09				
1261	Methods and Apparatus for Layout of Three Dimensional Matrix Array Memory for Reduced Cost Patterning	TW	099136574	26-Oct-10	201131744	16-Sep-11		
1262	Methods and Apparatus for Layout of Three Dimensional Matrix Array Memory for Reduced Cost Patterning	US	12/911,900	26-Oct-10	2011-0095438	28-Apr-11	8,809,128	19-Aug-14
1263	Methods and Apparatus for Layout of Three Dimensional Matrix Array Memory for Reduced Cost Patterning	WO	US10/054013	26-Oct-10	WO11/056527	12-May-11		
1264	Methods of Forming Pillars for Memory Cells Using Sequential Sidewall Patterning	TW	099136573	26-Oct-10	201126572	1-Aug-11		
1265	Methods of Forming Pillars for Memory Cells Using Sequential Sidewall Patterning	US	12/911,944	26-Oct-10	2011-0095338	28-Apr-11	8,741,696	3-Jun-14
1266	Methods of Forming Pillars for Memory Cells Using Sequential Sidewall Patterning	WO	US10/054027	26-Oct-10	WO2011/056534	12-May-11		
1267	A Memory Cell that Includes a Sidewall Collar for Pillar Isolation and Methods of Forming the Same	EP	11702105.5	21-Jan-11	2532028	12-Dec-12		
1268	Memory Cell that Includes a Sidewall Collar for Pillar Isolation and Methods of Forming the Same	US	14/182,264	17-Feb-14	2014-0158975	12-Jun-14	8,981,347	17-Mar-15
1269	Memory Cell that Includes a Sidewall Collar for Pillar Isolation and Methods of Forming the Same	US	13/868,667	23-Apr-13	2013-0234104	12-Sep-13	8,679,901	25-Mar-14
1270	A Memory Cell that Includes a Sidewall Collar for Pillar Isolation and Methods of Forming the Same	KR	2012-7020174	21-Jan-11				
1271	A Memory Cell that Includes a Sidewall Collar for Pillar Isolation and Methods of Forming the Same	TW	100103761	31-Jan-11	201203639	16-Jan-12		
1272	Memory Cell that Includes a Sidewall Collar for Pillar Isolation and Methods of Forming the Same	US	12/698,761	2-Feb-10	2011-0186797	4-Aug-11	8,431,492	30-Apr-13

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1273	A Memory Cell that Includes a Sidewall Collar for Pillar Isolation and Methods of Forming the Same	WO	US11/022091	21-Jan-11	WO11/097077	11-Aug-11		
1274	Creating Short Program Pulses in Asymmetric Memory Arrays	TW	099128933	27-Aug-10	201140589	16-Nov-11		
1275	Creating Short Program Pulses in Asymmetric Memory Arrays	US	12/551,546	31-Aug-09	2011-0051504	3-Mar-11	8,040,721	18-Oct-11
1276	Creating Short Program Pulses in Asymmetric Memory Arrays	WO	US10/045684	17-Aug-10	WO2011/025686	3-Mar-11		
1277	Three Dimesional Memory Using Electric Field Switchable Resistor Material and a Tunnel Oxide Isolation Device	US	61/142,214	1-Jan-09				
1278	Reducing Programming Time of a Memory Cell	US	13/403,454	23-Feb-12	2012-0155163	21-Jun-12	8,441,849	14-May-13
1279	Methods And Apparatus For Reducing Programming Time Of A Memory Cell	US	13/890,622	9-May-13	2013-0242681	19-Sep-13	8,773,898	8-Jul-14
1280	Methods And Apparatus For Reducing Programming Time Of A Memory Cell	US	14/290,888	29-May-14	2014-0269129	18-Sep-14	9,202,539	1-Dec-15
1281	Reducing Programming Time of a Memory Cell	US	12/551,548	31-Aug-09	2010-0051505	3-Mar-11	8,125,822	28-Feb-12
1282	Methods Of Programming Two Terminal Memory Cells	US	13/765,394	12-Feb-13	2013-0148421	13-Jun-13	8,565,015	22-Oct-13
1283	Flexible Multi-Pulse Set Operation for Phase-Change Memories	US	12/551,553	31-Aug-09	2010-0051506	3-Mar-11	8,379,437	19-Feb-13
1284	Dielectric-Based Memory Cells Having Multi-Level One-Time Programmable and Bi-Level Rewriteable Operating Modes and Methods of Forming the Same	US	14/804,126	20-Jul-15	2015-0325310	12-Nov-15		
1285	Dielectric-Based Memory Cells Having Multi-Level One-Time Programmable and Bi-Level Rewriteable Operating Modes and Methods of Forming the Same	US	13/780,089	28-Feb-13	2014-0241031	28-Aug-14		
1286	Dielectric-Based Memory Cells Having Multi-Level One-Time Programmable and Bi-Level Rewriteable Operating Modes and Methods of Forming the Same	WO	US14/018123	25-Feb-14	WO14/133979	4-Sep-14		
1287	Memory Cell Formed Using a Recess and Methods for Forming the Same	EP	11702106.3	21-Jan-11				
1288	Memory Cell Formed Using a Recess and Methods for Forming the Same	KR	2012-7020870	21-Jan-11				
1289	Memory Cell Formed Using a Recess and Methods for Forming the Same	TW	100104467	10-Feb-11	201140805	16-Nov-11		
1290	Memory Cell Formed Using a Recess and Methods for Forming the Same	US	12/703,907	11-Feb-10	2011-0193042	11-Aug-11	8,389,375	5-Mar-13

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1291	Memory Cell Formed Using a Recess and Methods for Forming the Same	WO	US11/022096	21-Jan-11	WO11/100100	18-Aug-11		
1292	Modified DARC Stack for Resist Patterning	US	61/071,089	11-Apr-08				
1293	Modified DARC Stack for Resist Patterning	TW	098112100	10-Apr-09				
1294	Modified DARC Stack for Resist Patterning	US	12/213,273	17-Jun-08	2009-0258495	15-Oct-09	8,084,366	27-Dec-11
1295	Modified DARC Stack for Resist Patterning	WO	US09/039119	1-Apr-09	WO09/126488	15-Oct-09		
1296	Double Patterning Method	US	61/071,094	11-Apr-08				
1297	Double Patterning Method	TW	098112102	10-Apr-09				
1298	Double Patterning Method	US	12/216,107	30-Jun-08			7,713,818	11-May-10
1299	Double Patterning Method	WO	US09/039121	1-Apr-09				
1300	MIIM Diodes Having Stacked Structure	DE	09792784.2	21-Sep-09	2342768	13-Jul-11	2342768	17-Dec-14
1301	MIIM Diodes Having Stacked Structure	EP	09792784.2	21-Sep-09	2342768	13-Jul-11	2342768	17-Dec-14
1302	MIIM Diodes Having Stacked Structure	GB	09792784.2	21-Sep-09	2342768	13-Jul-11	2342768	17-Dec-14
1303	MIIM Diodes Having Stacked Structure	TW	098132737	28-Sep-09			I473261	11-Feb-15
1304	MIIM Diodes Having Stacked Structure	US	12/240,785	29-Sep-08	2010-0078759	1-Apr-10	7,969,011	28-Jun-11
1305	MIIM Diodes Having Stacked Structure	WO	US09/057696	21-Sep-09	WO10/036616	1-Apr-10		
1306	MIIM Diodes	EP	09792788.3	21-Sep-09				
1307	MIIM Diodes Having Lanthanum Oxide	US	13/787,505	6-Mar-13	2013-0181181	18-Jul-13		
1308	MIIM Diodes	TW	098132743	28-Sep-09	201025619	1-Jul-10		
1309	MIIM Diodes	US	12/240,766	29-Sep-08	2010-0078758	1-Apr-10		
1310	MIIM Diodes	WO	US09/057701	21-Sep-09	WO10/036618	1-Apr-10		
1311	Antifuse-Based Memory Cells having Multiple Memory States and Methods of Forming the Same	US	13/314,580	8-Dec-11	2013-0148404	13-Jun-13		
1312	Antifuse-Based Memory Cells having Multiple Memory States and Methods of Forming the Same	WO	US12/067316	30-Nov-12	WO2013/085815	13-Jun-13		
1313	Reverse Leakage Reduction and Vertical Height Shrinking of Diode with Halo Doping	TW	098114087	28-Apr-09				
1314	Reverse Leakage Reduction and Vertical Height Shrinking of Diode with Halo Doping	US	12/149,217	29-Apr-08	2009-0268508	29-Oct-09	8,450,835	28-May-13
1315	Reverse Leakage Reduction and Vertical Height Shrinking of Diode with Halo Doping	WO	US09/002402	17-Apr-09	WO09/134324	5-Nov-09		
1316	Method for Fabricating Self Aligned Complimentary Pillar Structures and Wiring	TW	098113921	27-Apr-09				
1317	Method for Fabricating Self Aligned Complimentary Pillar Structures and Wiring	US	12/149,151	28-Apr-08	2009-0269932	29-Oct-09	7,786,015	31-Aug-10
1318	Method for Fabricating Self Aligned Complimentary Pillar Structures and Wiring	WO	US09/002400	17-Apr-09	WO09/134323	5-Nov-09		
1319	Carbon Nano-Film Reversible Resistance-Switchable Elements and Methods of Forming the Same	CN	200980117734.5	15-May-09	CN102027598A	20-Apr-11	ZL200980117734.5	26-Dec-12

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1320	Carbon Nano-Film Reversible Resistance-Switchable Elements and Methods of Forming the Same	EP	09747677.4	15-May-09	2277200	26-Jan-11		
1321	Carbon Nano-Film Reversible Resistance-Switchable Elements and Methods of Forming the Same	US	13/416,135	9-Mar-12	2012-0168707	5-Jul-12	8,680,503	25-Mar-14
1322	Carbon Nano-Film Reversible Resistance-Switchable Elements and Methods of Forming the Same	JP	2011-509737	15-May-09	2011-521455	21-Jul-11		
1323	Carbon Nano-Film Reversible Resistance-Switchable Elements and Methods of Forming the Same	KR	2010-7025607	15-May-09				
1324	Memroy Cell that Employs a Graphene or Carbon Nano-film Reversible Resistance Switching Element and Methods for Forming the Same	US	61/054,111	16-May-08				
1325	Carbon Nano-Film Reversible Resistance-Switchable Elements and Methods of Forming the Same	TW	098116310	15-May-09	201005930	1-Feb-10		
1326	Carbon Nano-Film Reversible Resistance-Switchable Elements and Methods of Forming the Same	US	12/466,197	14-May-09	2009-0283735	19-Nov-09	8,133,793	13-Mar-12
1327	Carbon Nano-Film Reversible Resistance-Switchable Elements and Methods of Forming the Same	WO	US09/044145	15-May-09	WO2009/140596	19-Nov-09		
1328	Integration Methods for Carbon Films in Two- and Three-Dimensional Memories and Memories formed therefrom	TW	098127311	13-Aug-09	201011865	16-Mar-10		
1329	Integration Methods for Carbon Films in Two- and Three-Dimensional Memories and Memories formed therefrom	US	12/541,075	13-Aug-09	2010-0038620	18-Feb-10	8,093,123	10-Jan-12
1330	Integration Methods for Carbon Films in Two- and Three-Dimensional Memories and Memories formed therefrom	WO	US09/053745	13-Aug-09	WO10/019794	18-Feb-10		
1331	Methods and Appratus for Increasing Memory Density Using Diode Layer Sharing	US	13/674,513	12-Nov-12	2013-0313503	28-Nov-13	8,633,528	21-Jan-14
1332	Methods and Appratus for Increasing Memory Density Using Diode Layer Sharing	TW	098127308	13-Aug-09	201017944	1-May-10		
1333	Methods and Appratus for Increasing Memory Density Using Diode Layer Sharing	US	12/541,078	13-Aug-09	2010-0038623	18-Feb-10	8,309,415	13-Nov-12
1334	Methods and Appratus for Increasing Memory Density Using Diode Layer Sharing	WO	US09/053737	13-Aug-09	WO10/019789	18-Feb-10		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1335	Integration Methods for Carbon Films in Two- and Three-Dimensional Memories and Memories formed therefrom	US	61/088,668	13-Aug-08				
1336	Methods and Appratus for Increasing Memory Density Using Diode Layer Sharing	US	61/088,665	13-Aug-08				
1337	Carbon-Based Interface Layer for a Memory Device and Methods of Forming the Same	US	61/078,911	8-Jul-08				
1338	Carbon-Based Interface Layer for a Memory Device and Methods of Forming the Same	TW	098123088	8-Jul-09	201007942	16-Feb-10		
1339	Carbon-Based Interface Layer for a Memory Device and Methods of Forming the Same	US	12/465,315	13-May-09	2010-0006811	14-Jan-10	8,569,730	29-Oct-13
1340	Carbon-Based Interface Layer for a Memory Device and Methods of Forming the Same	WO	US09/049463	1-Jul-09	WO10/005854	14-Jan-10		
1341	Carbon Based Resistivity-Switching Materials and Methods for Forming the Same	CN	200980134334.5	7-Jul-09	CN102144309	3-Aug-11		
1342	Carbon Based Resistivity-Switching Materials and Methods for Forming the Same	JP	2011-517528	7-Jul-09	2011-527834	4-Nov-11		
1343	Carbon Based Resistivity-Switching Materials and Methods for Forming the Same	KR	2011-7000195	7-Jul-09				
1344	Modulation of Resistivity in Carbon-Based Read-Writeable Materials	US	61/142,192	31-Dec-08				
1345	Carbon Based Resistivity-Switching Materials and Methods for Forming the Same	US	61/078,924	8-Jul-08				
1346	Carbon Based Resistivity-Switching Materials and Methods for Forming the Same	TW	098123128	8-Jul-09	201007837	16-Feb-10		
1347	Carbon Based Resistivity-Switching Materials and Methods for Forming the Same	US	12/499,467	8-Jul-09	2010-0006812	14-Jan-10		
1348	Carbon Based Resistivity-Switching Materials and Methods for Forming the Same	WO	US09/049854	7-Jul-09	WO10/006000	14-Jan-10		
1349	Dual Insulating Layer Diode with Asymmetric Interface State and Method of Fabrication	TW	098142769	14-Dec-09				
1350	Dual Insulating Layer Diode with Asymmetric Interface State and Method of Fabrication	US	12/336,410	16-Dec-08	2010-0148324	17-Jun-10	7,897,453	1-Mar-11

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1351	Dual Insulating Layer Diode with Asymmetric Interface State and Method of Fabrication	WO	US09/058858	29-Sep-09	WO2010/074785	1-Jul-10		
1352	Self-Assembly Process for Memory Array	TW	098133001	29-Sep-09				
1353	Self-Assembly Process for Memory Array	US	12/285,220	30-Sep-08	2010-0078618	1-Apr-10	8,008,213	30-Aug-11
1354	Self-Assembly Process for Memory Array	WO	US09/058151	24-Sep-09	WO2010/039568	8-Apr-10		
1355	Method of Programming a Nonvolatile Memory Device Containing a Carbon Storage Material	TW	098143439	17-Dec-09	201030752	16-Aug-10		
1356	Method of Programming a Nonvolatile Memory Device Containing a Carbon Storage Material	US	12/314,903	18-Dec-08	2010-0157651	24-Jun-10	7,978,496	12-Jul-11
1357	Method of Programming a Nonvolatile Memory Device Containing a Carbon Storage Material	WO	US09/067602	11-Dec-09	WO2010/080332	15-Jul-10		
1358	Non-Volatile Memory Arrays Comprising Rail Stacks with a Shared Diode Component Portion for Diodes of Electrically Isolated Pillars	CN	200980122197.3	2-Jun-09	CN102067315A	18-May-11	ZL200980122197.3	24-Apr-13
1359	Non-Volatile Memory Arrays Comprising Rail Stacks with a Shared Diode Component Portion for Diodes of Electrically Isolated Pillars	EP	09763292.1	2-Jun-09	2286453	23-Feb-11		
1360	Non-Volatile Memory Arrays Comprising Rail Stacks with a Shared Diode Component Portion for Diodes of Electrically Isolated Pillars	US	13/441,805	6-Apr-12	2012-0187361	26-Jul-12	8,748,859	10-Jun-14
1361	Non-Volatile Memory Arrays Comprising Rail Stacks with a Shared Diode Component Portion for Diodes of Electrically Isolated Pillars	JP	2011-513573	2-Jun-09	2011-524091	25-Aug-11		
1362	Non-Volatile Memory Arrays Comprising Rail Stacks with a Shared Diode Component Portion for Diodes of Electrically Isolated Pillars	KR	2011-7000959	2-Jun-09				
1363	Non-Volatile Memory Arrays Comprising Rail Stacks with a Shared Diode Component Portion for Diodes of Electrically Isolated Pillars	TW	098119833	12-Jun-09	201007887	16-Feb-10		
1364	Non-Volatile Memory Arrays Comprising Rail Stacks with a Shared Diode Component Portion for Diodes of Electrically Isolated Pillars	US	12/139,435	13-Jun-08	2009-0309089	17-Dec-09	8,154,005	10-Apr-12

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1365	Non-Volatile Memory Arrays Comprising Rail Stacks with a Shared Diode Component Portion for Diodes of Electrically Isolated Pillars	WO	US09/046001	2-Jun-09	WO09/152001	17-Dec-09		
1366	Semiconductor Memory With Improved Memory Block Switching	US	13/233,602	15-Sep-11	2012-0002476	5-Jan-12	8,320,196	27-Nov-12
1367	Semiconductor Memory With Improved Memory Block Switching	CN	201080035781.8	6-Aug-10	CN102483948A	30-May-12	ZL201080035781.8	10-Dec-14
1368	Semiconductor Memory With Improved Memory Block Switching	DE	10744637.9	6-Aug-10	2465116	20-Jun-12	2465116	26-Mar-14
1369	Semiconductor Memory With Improved Memory Block Switching	EP	10744637.9	6-Aug-10	2465116	20-Jun-12	2465116	26-Mar-14
1370	Semiconductor Memory With Improved Memory Block Switching	GB	10744637.9	6-Aug-10	2465116	20-Jun-12	2465116	26-Mar-14
1371	Semiconductor Memory With Improved Memory Block Switching	JP	2012-524764	6-Aug-10			5575243	11-Jul-14
1372	Semiconductor Memory With Improved Memory Block Switching	KR	2012-7006342	6-Aug-10				
1373	Semiconductor Memory With Improved Memory Block Switching	TW	099126388	6-Aug-10				
1374	Semiconductor Memory With Improved Memory Block Switching	US	12/538,492	10-Aug-09	2011-0032774	10-Feb-11	8,050,109	1-Nov-11
1375	Semiconductor Memory With Improved Memory Block Switching	WO	US10/044815	6-Aug-10				
1376	Three-Dimensional Memory Structures Having Shared Pillar Memory Cells	US	13/365,991	3-Feb-12	2012-0135580	31-May-12	9,076,518	7-Jul-15
1377	Three-Dimensional Memory Structures Having Shared Pillar Memory Cells	TW	098142966	15-Dec-09	201041121	16-Nov-10		
1378	Three-Dimensional Memory Structures Having Shared Pillar Memory Cells	US	12/344,022	24-Dec-08	2010-0155784	24-Jun-10	8,120,068	21-Feb-12
1379	Three-Dimensional Memory Structures Having Shared Pillar Memory Cells	WO	US09/058855	29-Sep-09	WO2010/074784	1-Jul-10		
1380	Method of Making Pillars Using Photoresist Spacer Mask	TW	098136215	26-Oct-09	201027620	16-Jul-10		
1381	Method of Making Pillars Using Photoresist Spacer Mask	US	12/289,396	27-Oct-08	2010-0105210	29-Apr-10	8,080,443	13-Dec-11
1382	Method of Making Pillars Using Photoresist Spacer Mask	WO	US09/061643	22-Oct-09	WO2010/062515	3-Jun-10		
1383	Method of Making Sub-Resolution Pillar Structures using Undercutting Technique	TW	098133740	5-Oct-09			I365509	1-Jun-12
1384	Method of Making Sub-Resolution Pillar Structures using Undercutting Technique	US	12/285,466	6-Oct-08	2010-0086875	8-Apr-10	8,076,056	13-Dec-11
1385	Method of Making Sub-Resolution Pillar Structures using Undercutting Technique	WO	US09/059188	1-Oct-09	WO2010/042380	15-Apr-10		

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1386	Quad Memory Cell and Method of Making Same	TW	098143764	18-Dec-09				
1387	Quad Memory Cell and Method of Making Same	WO	US09/068234	16-Dec-09	WO2010/080437			
1388	Quad Memory Cell and Method of Making Same	US	12/318,022	19-Dec-08	2010-0157653	24-Jun-10	7,910,407	22-Mar-11
1389	Quad Memory Cell and Method of Making Same	US	12/318,001	19-Dec-08	2010-0155689	24-Jun-10	7,923,812	12-Apr-11
1390	Reverse Set with Current Limit for Non-Volatile Storage	US	12/963,540	8-Dec-10	2011-0075468	31-Mar-11	8,098,511	17-Jan-12
1391	Reverse Set with Current Limit for Non-Volatile Storage	CN	200980124526.8	26-Jun-09	CN102077292A	25-May-11	ZL200980124526.8	14-Jan-15
1392	Reverse Set with Current Limit for Non-Volatile Storage	EP	09771201.2	26-Jun-09				
1393	Reverse Set with Current Limit for Non-Volatile Storage	JP	2011-516735	26-Jun-09	2011-526400	6-Oct-11	5285772	7-Jun-13
1394	Reverse Set with Current Limit for Non-Volatile Storage	KR	2011-7001341	26-Jun-09			10-1573506	25-Nov-15
1395	Set Scheme for Memory System	US	61/103,180	6-Oct-08				
1396	Memory System With Reversible Resistance-Switching Element	US	61/076,553	27-Jun-08				
1397	Reverse Set with Current Limit for Non-Volatile Storage	TW	098121706	26-Jun-09	201013673	1-Apr-10	I412038	11-Oct-13
1398	Reverse Set with Current Limit for Non-Volatile Storage	US	12/339,313	19-Dec-08	2009-0323391	31-Dec-09	7,869,258	11-Jan-11
1399	Reverse Set with Current Limit for Non-Volatile Storage	WO	US2009/048945	26-Jun-09	WO2009/158670	30-Dec-09		
1400	Smart Detection Circuit for Writing to Non-Volatile Storage	CN	200980124527.2	26-Jun-09	CN102077293	25-May-11	ZL200980124527.2	15-Oct-14
1401	Smart Detection Circuit for Writing to Non-Volatile Storage	EP	09771204.6	26-Jun-09				
1402	SMART DETECTION CIRCUIT FOR WRITING TO NON-VOLATILE STORAGE	JP	2011-516736	26-Jun-09			5297525	21-Jun-13
1403	Smart Detection Circuit for Writing to Non-Volatile Storage	KR	2011-7001342	26-Jun-09			10-1568327	5-Nov-15
1404	Smart Detection Circuit for Writing to Non-Volatile Storage	TW	098121699	26-Jun-09	201015550	16-Apr-10		
1405	Smart Detection Circuit for Writing to Non-Volatile Storage	US	12/339,327	19-Dec-08	2009-0323392	31-Dec-09	8,111,539	7-Feb-12
1406	Smart Detection Circuit for Writing to Non-Volatile Storage	WO	US09/048951	26-Jun-09	WO09/158673	30-Dec-09		
1407	Capacitive Discharge Method for Writing to a Non-Volatile Memory	US	13/237,773	20-Sep-11	2012-0008373	12-Jan-12	8,310,892	13-Nov-12

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1408	A NON-VOLATILE STORAGE SYSTEM AND A METHOD	CN	200980124528.7	26-Jun-09	CN102077294A	25-May-11	ZL200980124528.7	6-Nov-13
1409	Capacitive Discharge Method for Writing to a Non-Volatile Memory	DE	09771207.9	26-Jun-09	2304732	6-Apr-11	2304732	20-Aug-14
1410	Capacitive Discharge Method for Writing to a Non-Volatile Memory	EP	09771207.9	26-Jun-09	2304732	6-Apr-11	2304732	20-Aug-14
1411	Capacitive Discharge Method for Writing to a Non-Volatile Memory	GB	09771207.9	26-Jun-09	2304732	6-Apr-11	2304732	20-Aug-14
1412	Capacitive Discharge Method for Writing to a Non-Volatile Memory	JP	2011-516738	26-Jun-09			5377633	4-Oct-13
1413	Capacitive Discharge Method for Writing to a Non-Volatile Memory	KR	2011-7001690	26-Jun-09			10-1568328	5-Nov-15
1414	Capacitive Discharge Method for Writing to a Non-Volatile Memory	TW	098121700	26-Jun-09				
1415	Capacitive Discharge Method for Writing to a Non-Volatile Memory	US	12/339,338	19-Dec-08	2009-0323393	31-Dec-09	8,059,447	15-Nov-11
1416	Capacitive Discharge Method for Writing to a Non-Volatile Memory	WO	US09/048955	26-Jun-09	WO09/158676	30-Dec-09		
1417	Pulse Reset for Non-Volatile Storage	US	13/154,795	7-Jun-11	2011-0235404	29-Sep-11	8,270,210	18-Sep-12
1418	Short Reset Pulse for Non-Volatile Storage	CN	200980124529.1	26-Jun-09	CN102077295A	25-May-11	ZL200980124529.1	6-Nov-13
1419	Pulse Reset for Non-Volatile Storage	DE	09771208.7	26-Jun-09	2301032	30-Mar-11	2301032	25-Feb-15
1420	Pulse Reset for Non-Volatile Storage	EP	09771208.7	26-Jun-09	2301032	30-Mar-11	2301032	25-Feb-15
1421	Pulse Reset for Non-Volatile Storage	GB	09771208.7	26-Jun-09	2301032	30-Mar-11	2301032	25-Feb-15
1422	Pulse Reset for Non-Volatile Storage	JP	2011-516739	26-Jun-09			5301662	28-Jun-13
1423	Pulse Reset for Non-Volatile Storage	KR	2011-7002072	26-Jun-09			10-1573507	25-Nov-15
1424	Pulse Reset for Non-Volatile Storage	TW	098121698	26-Jun-09	201013672	1-Apr-10		
1425	Pulse Reset for Non-Volatile Storage	US	12/339,363	19-Dec-08	2009-0323394	31-Dec-09	7,978,507	12-Jul-11
1426	Pulse Reset for Non-Volatile Storage	WO	US09/048956	26-Jun-09	WO2009/158677	30-Dec-09		
1427	Methods for Etching Carbon Nano-Tube Films	US	61/225,487	14-Jul-09				
1428	Methods of Etching Carbon Nano-Tube Films	US	61/081,029	15-Jul-08				
1429	Electronic Devices Including Carbon-Based Films having Sidewall Liners, and Methods of Formng such Devices	TW	098123969	15-Jul-09	201013852	1-Apr-10		
1430	Electronic Devices Including Carbon-Based Films having Sidewall Liners, and Methods of Formng such Devices	US	12/415,964	31-Mar-09	2010-0012912	21-Jan-10	8,309,407	13-Nov-12
1431	Electronic Devices Including Carbon-Based Films having Sidewall Liners, and Methods of Formng such Devices	WO	US09/049462	7-Jul-09	WO10/008938	21-Jan-10		
1432	Triangle Two Dimensional Complementary Patterning of Pillars	CN	200980125461.9	25-Jun-09				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1433	Triangle Two Dimensional Complementary Patterning of Pillars	EP	09774133.4	25-Jun-09	2297775	23-Mar-11		
1434	Triangle Two Dimensional Complementary Patterning of Pillars	JP	2011-516639	25-Jun-09	P2011-527114A	20-Oct-11		
1435	Triangle Two Dimensional Complementary Patterning of Pillars	KR	2011-7002172	25-Jun-09				
1436	Triangle Two Dimensional Complementary Patterning of Pillars	TW	098121904	29-Jun-09				
1437	Triangle Two Dimensional Complementary Patterning of Pillars	US	12/216,109	30-Jun-08	2009-0321789	31-Dec-09	7,781,269	24-Aug-10
1438	Triangle Two Dimensional Complementary Patterning of Pillars	WO	US09/048581	25-Jun-09	WO2010/002682	7-Jan-10		
1439	Methods for Fabricating High Density Pillar Structures by Double Patterning Using Positive Photoresist	US	12/777,046	10-May-10	2010-0219510	2-Sep-10	7,935,553	3-May-11
1440	Methods for Fabricating High Density Pillar Structures by Double Patterning Using Positive Photoresist	US	13/070,825	24-Mar-11	2011-0171809	14-Jul-11	8,138,010	20-Mar-12
1441	Methods for Fabricating High Density Pillar Structures by Double Patterning Using Positive Photoresist	CN	200980125068.X	25-Jun-09	CN102077346A	25-May-11	ZL200980125068.X	1-May-13
1442	Methods for Fabricating High Density Pillar Structures by Double Patterning Using Positive Photoresist	EP	09774134.2	25-Jun-09	2294615	16-Mar-11		
1443	Methods for Fabricating High Density Pillar Structures by Double Patterning Using Positive Photoresist	JP	2011-516640	25-Jun-09	P2011-527155A	20-Oct-11	5336589	9-Aug-13
1444	Methods for Fabricating High Density Pillar Structures by Double Patterning Using Positive Photoresist	KR	2011-7002164	25-Jun-09			10-1487288	22-Jan-15
1445	Methods for Fabricating High Density Pillar Structures by Double Patterning Using Positive Photoresist	TW	098121903	29-Jun-09			I500070	11-Sep-15
1446	Methods for Fabricating High Density Pillar Structures by Double Patterning Using Positive Photoresist	US	12/216,108	30-Jun-08	2009-0323385	31-Dec-09	7,732,235	8-Jun-10
1447	Methods for Fabricating High Density Pillar Structures by Double Patterning Using Positive Photoresist	WO	US09/048584	25-Jun-09	WO2010/002683	7-Jan-10		
1448	Sidewall Structured Switchable Resistor Cell	CN	200980112695.X	1-Apr-09	CN101999170A	30-Mar-11	ZL200980112695.X	16-Jan-13
1449	Sidewall Structured Switchable Resistor Cell	EP	09731080.9	1-Apr-09	2277201	26-Jan-11		
1450	Sidewall Structured Switchable Resistor Cell	CN	2012105722908	1-Apr-09	CN102983273A	20-Mar-13		
1451	Sidewall Structured Switchable Resistor Cell	JP	2012-130412	1-Apr-09	P2012-212902A	1-Nov-12	5395213	25-Oct-13

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1452	Sidewall Structured Switchable Resistor Cell	JP	2011-504064	1-Apr-09	P2011-517855A	16-Jun-11	5044042	20-Jul-12
1453	Sidewall Structured Switchable Resistor Cell	KR	2010-7024382	1-Apr-09			10-1532293	23-Jun-15
1454	Sidewall Structured Switchable Resistor Cell	TW	098112104	10-Apr-09			I380437	21-Dec-12
1455	Sidewall Structured Switchable Resistor Cell	US	12/216,110	30-Jun-08	2009-0256129	15-Oct-09	7,812,335	12-Oct-10
1456	Sidewall Structured Switchable Resistor Cell	WO	US09/039126	1-Apr-09				
1457	Adjustable Read Latency for Memory Device in Page-Mode Access	TW	098122082	30-Jun-09	201015571	16-Apr-10		
1458	Adjustable Read Latency for Memory Device in Page-Mode Access	US	12/164,601	30-Jun-08				
1459	Adjustable Read Latency for Memory Device in Page-Mode Access	WO	US09/048991	29-Jun-09	WO2010/002753	7-Jan-10		
1460	Write Method of a Cross Point Non-Volatile Memory Cell with Diode	CN	201080024397.8	30-Mar-10			ZL201080024397.8	17-Sep-14
1461	Cross Point Non-Volatile Memory Cell	EP	10725309.8	30-Mar-10	2415053	8-Feb-12	2415053	
1462	Cross Point Non-Volatile Memory Cell	US	13/591,097	21-Aug-12	2013-0021837	24-Jan-13	8,605,486	10-Dec-13
1463	Write Method of a Cross Point Non-Volatile Memory Cell with Diode	JP	2012-503603	30-Mar-10	2012-523061	27-Sep-12	5558553	13-Jun-14
1464	Cross Point Non-Volatile Memory Cell	KR	2011-7026285	30-Mar-10				
1465	Cross Point Non-Volatile Memory Cell	TW	099109231	26-Mar-10	201104685	1-Feb-11		
1466	Cross Point Non-Volatile Memory Cell	US	12/418,191	3-Apr-09	2010-0254175	7-Oct-10	8,270,199	18-Sep-12
1467	Cross Point Non-Volatile Memory Cell	WO	US10/029186	30-Mar-10	WO2010/123657	28-Oct-10		
1468	Multibit Resistance-Switching Memory Cell Including Resistance Switching Elements	CN	201080021499.4	30-Mar-10	CN102439665A	2-May-12	ZL201080021499.4	14-Jan-15
1469	Writing a multibit resistance-switching memory cell including a dummy resistance, resistance switching elements and diodes	EP	10726350.1	30-Mar-10	2415052	8-Feb-12		
1470	Multi -Bit Resistance-Switching Memory Cell	US	13/396,501	14-Feb-12	2012-0140547	7-Jun-12	8,482,960	9-Jul-13
1471	Multi -Bit Resistance-Switching Memory Cell	US	13/396,489	14-Feb-12	2012-0140546	7-Jun-12	8,649,206	11-Feb-14
1472	Writing a Multi-Bit Resistance-Switching Memory Cell Including a Dummy Resistance, Resistance Switching Elements and Diodes	JP	2012-503605	30-Mar-10	2012-523062	27-Sep-12	5557899	13-Jun-14
1473	Multi -Bit Resistance-Switching Memory Cell	KR	2011-7026286	30-Mar-10				
1474	Multi -Bit Resistance-Switching Memory Cell	TW	099109233	26-Mar-10				
1475	Multi -Bit Resistance-Switching Memory Cell	US	12/418,212	3-Apr-09	2010-0254176	7-Oct-10	8,139,391	20-Mar-12
1476	Multi -Bit Resistance-Switching Memory Cell	WO	US10/029189	30-Mar-10	WO2010/114831	7-Oct-10		
1477	Programming Non-Volatile Strorage Element Using Current From Other Element	US	13/154,832	7-Jun-11	2011-0235405	29-Sep-11	8,270,202	18-Sep-12
1478	Programming Non-Volatile Strorage Element Using Current From Other Element	CN	201080019803.1	30-Mar-10			ZL201080019803.1	12-Nov-14
1479	Programming Non-Volatile Strorage Element Using Current From Other Element	EP	10726351.9	30-Mar-10	2415054	8-Feb-12		
1480	Programming Non-Volatile Strorage Element Using Current From Other Element	JP	2012-503607	30-Mar-10			5352004	30-Aug-13

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1481	Programming Non-Volatile Storage Element Using Current From Other Element	KR	2011-7026287	30-Mar-10				
1482	Programming Non-Volatile Storage Element Using Current From Other Element	TW	099109244	26-Mar-10	201104686	1-Feb-11		
1483	Programming Non-Volatile Storage Element Using Current From Other Element	US	12/418,233	3-Apr-09	2010-0254177	7-Oct-10	7,978,498	12-Jul-11
1484	Programming Non-Volatile Storage Element Using Current From Other Element	WO	US10/029192	30-Mar-10	WO2010/114832	7-Oct-10		
1485	Self-Aligned Stacked Memory Arrays and Methods of Forming	US	61/115,913	18-Nov-08				
1486	Self-Aligned Three-Dimensional Non-Volatile Memory Fabrication	TW	098139153	18-Nov-09	201027713	16-Jul-10		
1487	Self-Aligned Three-Dimensional Non-Volatile Memory Fabrication	US	12/468,717	19-May-09	2010-0124813	20-May-10	8,105,867	31-Jan-12
1488	Self-Aligned Three-Dimensional Non-Volatile Memory Fabrication	WO	US09/059052	30-Sep-09	WO10/059296	27-May-10		
1489	CARBON-BASED RESISTIVITY-SWITCHING MATERIALS AND METHODS OF FORMING THE SAME	US	61/082,180	18-Jul-08				
1490	CARBON-BASED RESISTIVITY-SWITCHING MATERIALS AND METHODS OF FORMING THE SAME	TW	098124291	17-Jul-09	201021161	1-Jun-10		
1491	CARBON-BASED RESISTIVITY-SWITCHING MATERIALS AND METHODS OF FORMING THE SAME	US	12/505,122	17-Jul-09				
1492	CARBON-BASED RESISTIVITY-SWITCHING MATERIALS AND METHODS OF FORMING THE SAME	WO	US09/050930	17-Jul-09	WO10/009364	21-Jan-10		
1493	Damascene Process for Carbon Memory Element with MIM Diode	US	12/566,486	24-Sep-09	2010-0081268	1-Apr-10	7,935,594	3-May-11
1494	Damascene Process for Carbon Memory Element with MIM Diode	DE	09792789.1	21-Sep-09	2342752	13-Jul-11	2342752	7-Jan-15
1495	Damascene Process for Carbon Memory Element with MIM Diode	EP	09792789.1	21-Sep-09	2342752	13-Jul-11	2342752	7-Jan-15
1496	Damascene Process for Carbon Memory Element with MIM Diode	GB	09792789.1	21-Sep-09	2342752	13-Jul-11	2342752	7-Jan-15
1497	METHOD FOR FORMING MEMORY ELEMENT IN SERIES WITH MIIM DIODE	TW	098132742	28-Sep-09			I472026	1-Feb-15
1498	Damascene Process for Carbon Memory Element with MIM Diode	US	12/240,758	29-Sep-08			7,615,439	10-Nov-09
1499	Damascene Process for Carbon Memory Element with MIM Diode	WO	US09/057704	21-Sep-09	WO10/036619	1-Apr-10		
1500	Method of Making a Non-Volatile Memory Device	CN	200980127111.6	2-Jul-09	CN102089880A	8-Jun-11	ZL200980127111.6	7-Aug-13

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1501	Method of Making a Non-Volatile Memory Device	EP	09790046.8	2-Jul-09	2308089	13-Apr-11		
1502	Method of Making a Non-Volatile Memory Device	JP	2011-517490	2-Jul-09	P2011-527832A	4-Nov-11	5227455	22-Mar-13
1503	Method of Making a Non-Volatile Memory Device	KR	2011-7003238	2-Jul-09				
1504	Method of Making a Non-Volatile Memory Device	TW	098123475	10-Jul-09			I381490	1-Jan-13
1505	Method of Making a Non-Volatile Memory Device	US	12/216,924	11-Jul-08			7,579,232	25-Aug-09
1506	Method of Making a Non-Volatile Memory Device	WO	US09/049518	2-Jul-09	WO10/005866	14-Jan-10		
1507	Multiple Series Passive Element Matrix Cell for Three-Dimensional Arrays	TW	098123112	8-Jul-09				
1508	Multiple Series Passive Element Matrix Cell for Three-Dimensional Arrays	US	12/216,677	9-Jul-08	2010-0008123	14-Jan-10	8,014,185	6-Sep-11
1509	Multiple Series Passive Element Matrix Cell for Three-Dimensional Arrays	WO	US09/049513	2-Jul-09	WO2010/005864	14-Jan-10		
1510	Cross Point Memory Cell with Distributed Diodes and Method of Making Same	TW	098123089	8-Jul-09				
1511	Cross Point Memory Cell with Distributed Diodes and Method of Making Same	US	12/216,678	9-Jul-08	2010-0008124	14-Jan-10	7,733,685	8-Jun-10
1512	Cross Point Memory Cell with Distributed Diodes and Method of Making Same	WO	US09/049502	2-Jul-09	WO2010/005862	14-Jan-10		
1513	Voltage Regulator with Reduced Sensitivity of Output Voltage to Change in Load Current	US	12/236,382	23-Sep-08	2010-0074034	25-Mar-10	7,796,437	14-Sep-10
1514	Memory System with Sectional Data Lines	US	13/079,613	4-Apr-11	2011-0182105	28-Jul-11	8,358,528	22-Jan-13
1515	Memory System with Sectional Data Lines	CN	200980133212.4	17-Jul-09	CN102132352	20-Jul-11	ZL200980133212.4	1-Jul-15
1516	Memory System with Sectional Data Lines	DE	097905731	17-Jul-09	2321826	18-May-11	2321826	8-Feb-12
1517	Memory System with Sectional Data Lines	EP	09790573.1	17-Jul-09	2321826	18-May-11	2321826	8-Feb-12
1518	Memory System with Sectional Data Lines	FR	097905731	17-Jul-09	2321826	18-May-11	2321826	8-Feb-12
1519	Memory System with Sectional Data Lines	GB	097905731	17-Jul-09	2321826	18-May-11	2321826	8-Feb-12
1520	Memory System with Sectional Data Lines	US	13/362,320	31-Jan-12	2012-0170347	5-Jul-12	8,982,597	17-Mar-15
1521	Memory System with Sectional Data Lines	US	13/362,311	31-Jan-12	2012-0170346	5-Jul-12	8,913,413	16-Dec-14
1522	Memory System with Sectional Data Lines	JP	2011-525038	17-Jul-09	2012-501038	12-Jan-12	5318211	19-Jul-13
1523	Memory System with Sectional Data Lines	KR	2011-7007003	17-Jul-09			10-1573509	25-Nov-15
1524	Memory System with Sectional Data Lines	NL	097905731	17-Jul-09	2321826	18-May-11	2321826	8-Feb-12
1525	Memory System with Sectional Data Line	US	61/091,720	25-Aug-08				
1526	Memory System with Sectional Data Lines	TW	098126194	4-Aug-09	20107683	1-May-10	I427642	21-Feb-14
1527	Memory System with Sectional Data Lines	US	12/410,648	25-Mar-09	2010-0046267	25-Feb-10	8,130,528	6-Mar-12
1528	Memory System with Sectional Data Lines	WO	US09/050970	17-Jul-09	WO10/024982	4-Mar-10		
1529	Producing C based read writable materials with post treatment	US	61/087,164	7-Aug-08				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1530	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	TW	098126804	10-Aug-09	201017825	1-May-10		
1531	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	US	12/536,459	5-Aug-09	2010-0032639	11-Feb-10		
1532	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	WO	US09/053060	6-Aug-09	WO2010/017428	11-Feb-10		
1533	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	TW	098126825	10-Aug-09	201017826	1-May-10		
1534	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	US	12/536,463	5-Aug-09	2010-0032643	11-Feb-10	8,557,685	15-Oct-13
1535	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	WO	US09/053059	6-Aug-09	WO2010/017427	11-Feb-10		
1536	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	TW	098126824	10-Aug-09	201017759	1-May-10		
1537	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	US	12/536,469	5-Aug-09	2010-0032640	11-Feb-10		
1538	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	WO	US09/053058	6-Aug-09	WO10/017426	11-Feb-10		
1539	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	TW	098126803	10-Aug-09	201017824	1-May-10		
1540	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	US	12/536,457	5-Aug-09	2010-0032638	11-Feb-10	8,466,044	18-Jun-13
1541	MEMORY CELL THAT INCLUDES A CARBON-BASED MEMORY ELEMENT AND METHODS OF FORMING THE SAME	WO	US09/053057	6-Aug-09	WO10/017425	11-Feb-10		
1542	Carbon Based Memory Elements Exhibiting Reduced Delamination and Methods for Forming the Same	CN	200980152209.7	22-Oct-09	102265400A	30-Nov-11		
1543	Carbon Based Memory Elements Exhibiting Reduced Delamination and Methods for Forming the Same	EP	09744276.8	22-Oct-09	2340562	6-Jul-11		

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1544	Carbon Based Memory Elements Exhibiting Reduced Delamination and Methods for Forming the Same	JP	2011-533336	22-Oct-09	2012-507150	22-Mar-12		
1545	Carbon Based Memory Elements Exhibiting Reduced Delamination and Methods for Forming the Same	KR	2011-7011190	22-Oct-09				
1546	Methods and Apparatus Exhibiting Reduced Delamination of Carbon-Based Resistivity Switching Materials	US	61/108,017	23-Oct-08				
1547	Carbon Based Memory Elements Exhibiting Reduced Delamination and Methods for Forming the Same	TW	098136061	23-Oct-09	201027744	16-Jul-10		
1548	Carbon Based Memory Elements Exhibiting Reduced Delamination and Methods for Forming the Same	US	12/604,178	22-Oct-09	2010-0102291	29-Apr-10		
1549	Carbon Based Memory Elements Exhibiting Reduced Delamination and Methods for Forming the Same	WO	US09/061687	22-Oct-09	WO10/048408	29-Apr-10		
1550	Methods for Increasing Carbon Nano-Tube (CNT) Yield in Memory Devices	US	61/090,222	19-Aug-08				
1551	Methods for Increasing Carbon Nano-Tube (CNT) Yield in Memory Devices	TW	098127938	19-Aug-09	201017946	1-May-10		
1552	Methods for Increasing Carbon Nano-Tube (CNT) Yield in Memory Devices	US	12/543,465	18-Aug-09	2010-0044671	25-Feb-10	8,431,417	30-Apr-13
1553	Methods for Increasing Carbon Nano-Tube (CNT) Yield in Memory Devices	WO	US09/054219	18-Aug-09	WO2010/022097	25-Feb-10		
1554	Modulations of Resistivity in Carbon-Based Read-Writeable Materials	US	61/108,013	23-Oct-08				
1555	Nanoimprint Enhanced Resist Spacer Patterning Method	US	12/318,590	31-Dec-08	2010-0167502	1-Jul-10	7,846,756	7-Dec-10
1556	Methods for Increased Array Feature Density	US	13/366,916	6-Feb-12	2012-0135603	31-May-12	8,372,740	12-Feb-13
1557	Methods for Increased Array Feature Density	US	13/760,877	6-Feb-13	2013-0183829	18-Jul-13	8,658,526	25-Feb-14
1558	Method for Increased Array Feature Density	US	12/754,602	5-Apr-10	2010-0193916	5-Aug-10	8,114,765	14-Feb-12
1559	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	US	13/331,267	20-Dec-11	2012-0094478	19-Apr-12	8,357,606	22-Jan-13
1560	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	US	13/744,971	18-Jan-13	2013-0130467	23-May-13	8,637,389	28-Jan-14
1561	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	CN	200980153246.X	29-Dec-09	CN102272888A	7-Dec-11	ZL200980153246.X	28-May-14

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1562	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	DE	09799471.9	29-Dec-09	2380189	26-Oct-11	2380189	9-Apr-14
1563	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	EP	09799471.9	29-Dec-09	2380189	26-Oct-11	2380189	9-Apr-14
1564	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	GB	09799471.9	29-Dec-09	2380189	26-Oct-11	2380189	9-Apr-14
1565	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	JP	2011-543713	29-Dec-09	2012-514339A	21-Jun-12	5695575	13-Feb-15
1566	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	KR	2011-7015138	29-Dec-09				
1567	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	TW	098146517	31-Dec-09	201034051	16-Sep-10		
1568	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	US	12/318,609	31-Dec-08	2010-0167520	1-Jul-10	8,084,347	27-Dec-11
1569	Resist Feature and Removable Spacer Pitch Doubling Patterning Method for Pillar Structures	WO	US09/069711	29-Dec-09	WO10/078343	8-Jul-10		
1570	Programming A Memory Cell with a Diode in Series by Applying Reverse Bias	TW	098143753	18-Dec-09	201030753	16-Aug-10		
1571	Programming A Memory Cell with a Diode in Series by Applying Reverse Bias	US	12/318,021	19-Dec-08	2010-0157652A1	24-Jun-10	7,944,728	17-May-11
1572	Programming A Memory Cell with a Diode in Series by Applying Reverse Bias	WO	US09/067604	11-Dec-09	WO2010/080334	15-Jul-10		
1573	Set and Reset Detection Circuits for Reversible Resistance Switching Memory Material	CN	200980139728.X	23-Sep-09	CN 102203872A	28-Sep-11	ZL200980139728.X	15-Oct-14
1574	Set and Reset Detection Circuits for Reversible Resistance Switching Material	DE	09792881.6	23-Sep-09	2342717	13-Jul-11	2342717	25-Feb-15
1575	Set and Reset Detection Circuits for Reversible Resistance Switching Material	EP	09792881.6	23-Sep-09	2342717	13-Jul-11	2342717	25-Feb-15
1576	Set and Reset Detection Circuits for Reversible Resistance Switching Material	GB	09792881.6	23-Sep-09	2342717	13-Jul-11	2342717	25-Feb-15
1577	Set and Reset Detection Circuits for Reversible Resistance Switching Memory Material	CN	201410534704.7	23-Sep-09				
1578	Set and Reset Detection Circuits for Reversible Resistance Switching Material	EP	15150340.6	23-Sep-09				

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1579	Set and Reset Detection Circuits for Reversible Resistance Switching Memory Material	CN	201410535382.8	23-Sep-09	CN104681083A	3-Jun-15		
1580	Set and Reset Detection Circuits for Reversible Resistance Switching Material	JP	2011-530114	23-Sep-09	2012-504839	23-Feb-12	5390620	18-Oct-13
1581	Set and Reset Detection Circuits for Reversible Resistance Switching Material	KR	2011-7010204	23-Sep-09				
1582	Memory System with Circuit to Provide Ramping Pulse with Detection for Re-Writeable Material	US	61/103,225	6-Oct-08				
1583	Set and Reset Detection Circuits for Reversible Resistance Switching Material	TW	098133890	6-Oct-09	201027547	16-Jul-10	I486960	1-Jun-15
1584	Set and Reset Detection Circuits for Reversible Resistance Switching Material	US	12/395,859	2-Mar-09	2010-0085794	8-Apr-10	7,920,407	5-Apr-11
1585	Set and Reset Detection Circuits for Reversible Resistance Switching Material	WO	US09/057979	23-Sep-09	WO10/042316	15-Apr-10		
1586	Optimized Re-Writable Materials, Devices, and Methods for Forming the Same	US	61/113,850	12-Nov-08				
1587	Metal Oxide Materials and Electrodes for RE-RAM	TW	098138489	12-Nov-09				
1588	Metal Oxide Materials and Electrodes for RE-RAM	US	12/364,707	3-Feb-09	2010-0117053	13-May-10	8,304,754	6-Nov-12
1589	Metal Oxide Materials and Electrodes for RE-RAM	WO	US09/059237	1-Oct-09	WO10/056428	20-May-10		
1590	Non-Volatile Memory Cell Including Carbon Storage Element Formed on a Silicide Layer	TW	099100822	13-Jan-10	201030946	16-Aug-10		
1591	Non-Volatile Memory Cell Including Carbon Storage Element Formed on a Silicide Layer	US	12/320,008	14-Jan-09	2010-0176366	15-Jul-10	8,023,310	20-Sep-11
1592	Non-Volatile Memory Cell Including Carbon Storage Element Formed on a Silicide Layer	WO	US10/020084	5-Jan-10	WO2010/083067	22-Jul-10		
1593	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	CN	200980142194.6	23-Sep-09	CN 102203873A	28-Sep-11	ZL200980142194.6	9-Jul-14
1594	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	DE	09792884.0	23-Sep-09	2351040	3-Aug-11	2351040	14-Aug-13
1595	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	EP	09792884.0	23-Sep-09	2351040	3-Aug-11	2351040	14-Aug-13
1596	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	GB	09792884.0	23-Sep-09	2351040	3-Aug-11	2351040	14-Aug-13

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1597	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	JP	2011-533210	23-Sep-09	2012-507070	22-Mar-12	5547741	23-May-14
1598	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	KR	2011-7011939	23-Sep-09			10-1579555	16-Dec-15
1599	Page buffer program command and methods to reprogram pages without re-inputing data on the Smart Media Interface	US	61/108,507	25-Oct-08				
1600	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	US	14/285,829	23-May-14				
1601	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	TW	098136069	23-Oct-09	2010-27557	16-Jul-10		
1602	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	US	12/414,925	31-Mar-09	2010-0106893	29-Apr-10	8,397,024	12-Mar-13
1603	Page Buffer Program Command and Methods to Reprogram Pages without Re-inputing Data to a Memory Device	WO	US09/057992	23-Sep-09	WO10/047911	29-Apr-10		
1604	Column Redudancy Strategy and Bad Page Marking Strategy for Fast Readout	US	61/108,524	26-Oct-08				
1605	Bad Page Marking Strategy for Fast Readout in Memory	US	12/400,091	9-Mar-09	2010-0107022	29-Apr-10	7,996,736	9-Aug-11
1606	Method for Selectively Retrieving Column Redundancy Data in Memory Device	TW	098136062	23-Oct-09	201022929	16-Jun-10		
1607	Method for Selectively Retrieving Column Redundancy Data in Memory Device	US	12/414,935	31-Mar-09	2010-0107004	29-Apr-10	7,966,532	21-Jun-11
1608	Method for Selectively Retrieving Column Redundancy Data in Memory Device	WO	US09/057996	23-Sep-09	WO10/047912	29-Apr-10		
1609	ELECTRONIC DEVICES INCLUDING CARBON NANO-TUBE FILMS HAVING CARBON-BASED LINERS, AND METHODS OF FORMING THE SAME	TW	098137034	30-Oct-09	201027672	16-Jul-10		
1610	ELECTRONIC DEVICES INCLUDING CARBON NANO-TUBE FILMS HAVING CARBON-BASED LINERS, AND METHODS OF FORMING THE SAME	US	12/608,607	29-Oct-09	2010-0108982	6-May-10	8,421,050	16-Apr-13
1611	ELECTRONIC DEVICES INCLUDING CARBON NANO-TUBE FILMS HAVING CARBON-BASED LINERS, AND METHODS OF FORMING THE SAME	WO	US09/062532	29-Oct-09	WO10/059368	27-May-10		

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1612	ELECTRONIC DEVICES INCLUDING CARBON NANO-TUBE FILMS HAVING BORON NITRIDE-BASED LINERS, AND METHODS OF FORMING THE SAME	TW	098137028	30-Oct-09	201027671	16-Jul-10		
1613	ELECTRONIC DEVICES INCLUDING CARBON NANO-TUBE FILMS HAVING BORON NITRIDE-BASED LINERS, AND METHODS OF FORMING THE SAME	US	12/608,592	29-Oct-09	2010-0108981	6-May-10	8,835,892	16-Sep-14
1614	ELECTRONIC DEVICES INCLUDING CARBON NANO-TUBE FILMS HAVING BORON NITRIDE-BASED LINERS, AND METHODS OF FORMING THE SAME	WO	US090/62507	29-Oct-09	WO10/059362	27-May-10		
1615	Carbon-Based Liner For Protection of Carbon Nano-Tube Films Against Short-Circuiting and Damage	US	61/109,905	30-Oct-08				
1616	Electronic Device including Carbon-Based Films, and Methods of Forming Such Devices	TW	098137025	30-Oct-09	201027670	16-Jul-10		
1617	Electronic Device including Carbon-Based Films, and Methods of Forming Such Devices	US	12/408,419	20-Mar-09	2010-0108976	6-May-10		
1618	Electronic Device including Carbon-Based Films, and Methods of Forming Such Devices	WO	US09/062330	28-Oct-09	WO10/056521	20-May-10		
1619	Integration of Damascene Type Diodes and Conductive Wires for Memory Device	TW	098139539	20-Nov-09	201029115	1-Aug-10		
1620	Integration of Damascene Type Diodes and Conductive Wires for Memory Device	US	12/292,620	21-Nov-08			8,193,074	5-Jun-12
1621	Integration of Damascene Type Diodes and Conductive Wires for Memory Device	WO	US09/064915	18-Nov-09	WO2010/059672	27-May-10		
1622	Limited charge delivery for programming non-volatile storage elements	US	12/472,074	26-May-09	2010-0302835	2-Dec-10	7,885,091	8-Feb-11
1623	Memory Employing Diamond-Like Carbon Resistivity-Switchable Material and Methods of Forming the Same	TW	100116963	13-May-11	201208160	16-Feb-12		
1624	Memory Employing Diamond-Like Carbon Resistivity-Switchable Material and Methods of Forming the Same	US	12/780,564	14-May-10	2011-0278529	17-Nov-11		
1625	Memory Employing Diamond-Like Carbon Resistivity-Switchable Material and Methods of Forming the Same	WO	US11/036075	11-May-11	W011/143311	17-Nov-11		
1626	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES AND A DOUBLE-GLOBAL-BIT-LINE ARCHITECTURE	CN	201080023575.5	2-Apr-10	CN102449698A	9-May-12	ZL201080023575.5	29-Jul-15

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1627	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES AND A DOUBLE-GLOBAL-BIT-LINE ARCHITECTURE	EP	10719436.7	2-Apr-10	2417598	15-Feb-12		
1628	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES AND A DOUBLE-GLOBAL-BIT-LINE ARCHITECTURE	JP	2012-504733	2-Apr-10				
1629	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES AND A DOUBLE-GLOBAL-BIT-LINE ARCHITECTURE	KR	2011-7026209	2-Apr-10				
1630	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES AND A DOUBLE-GLOBAL-BIT-LINE ARCHITECTURE	TW	099110923	8-Apr-10				
1631	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES AND A DOUBLE-GLOBAL-BIT-LINE ARCHITECTURE	US	12/748,233	26-Mar-10	2010-0259961	14-Oct-10	8,199,576	12-Jun-12
1632	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES AND A DOUBLE-GLOBAL-BIT-LINE ARCHITECTURE	WO	US10/029855	2-Apr-10	WO2010/117912	14-Oct-10		
1633	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES AND A SINGLE-SIDED WORD LINE ARCHITECTURE	US	13/735,983	7-Jan-13	2013-0121078	16-May-13	8,780,605	15-Jul-14
1634	Three-Dimensional Array of Re-Programmable Non-Volatile Memory Elements Having Vertical Bit Lines and a Single-Sided Word Line Architecture	US	14/153,794	13-Jan-14	2014-0192595	10-Jul-14	9,190,134	17-Nov-15
1635	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINESAND A SINGLE-SIDED WORD LINE ARCHITECTURE	CN	201080023539.9	2-Apr-10	CN102449699A	9-May-12	ZL201080023539.9	2-Sep-15
1636	Three-Dimensional Array of Re-Programmable Non-Volatile Memory Elements Having Vertical Bit Lines	US	14/933,672	5-Nov-15				
1637	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINESAND A SINGLE-SIDED WORD LINE ARCHITECTURE	EP	10726352.7	2-Apr-10	2417599	15-Feb-12		

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1638	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINESAND A SINGLE-SIDED WORD LINE ARCHITECTURE	JP	2012-504735	2-Apr-10	2012-523649	4-Oct-12	5722874	3-Apr-15
1639	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINESAND A SINGLE-SIDED WORD LINE ARCHITECTURE	KR	2011-7026212	2-Apr-10				
1640	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINESAND A SINGLE-SIDED WORD LINE ARCHITECTURE	TW	099110912	8-Apr-10				
1641	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINESAND A SINGLE-SIDED WORD LINE ARCHITECTURE	US	12/748,260	26-Mar-10	2010-0259962	14-Oct-10	8,351,236	8-Jan-13
1642	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINESAND A SINGLE-SIDED WORD LINE ARCHITECTURE	WO	US10/029857	2-Apr-10	WO2010/117914	14-Oct-10		
1643	Method For Non-Volatile Memory Having 3D Array of Read/Write Elements with Efficient Decoding of Vertical Bit Lines and Word Lines	US	14/057,971	18-Oct-13	2014-0043911	13-Feb-14	9,245,629	26-Jan-16
1644	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS WITH VERTICAL BIT LINES AND LATERALLY ALIGNED ACTIVE ELEMENTS AND METHODS THEREOF	CN	201180028685.5	7-Jun-11	CN102971799A	13-Mar-13		
1645	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS WITH VERTICAL BIT LINES AND LATERALLY ALIGNED ACTIVE ELEMENTS AND METHODS THEREOF	EP	11725298.1	7-Jun-11	2580758	17-Apr-13		
1646	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS WITH VERTICAL BIT LINES AND LATERALLY ALIGNED ACTIVE ELEMENTS AND METHODS THEREOF	JP		7-Jun-11				
1647	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS WITH VERTICAL BIT LINES AND LATERALLY ALIGNED ACTIVE ELEMENTS AND METHODS THEREOF	KR	2013-7000288	7-Jun-11				
1648	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS WITH VERTICAL BIT LINES AND LATERALLY ALIGNED ACTIVE ELEMENTS AND METHODS THEREOF	US	61/352,714	8-Jun-10				

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1649	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS WITH VERTICAL BIT LINES AND LATERALLY ALIGNED ACTIVE ELEMENTS AND METHODS THEREOF	TW	100120027	8-Jun-11				
1650	Non-Volatile Memory Having 3d Array of Read/Write Elements with Vertical Bit Lines and Laterally Aligned Active Elements and Methods Thereof	US	13/151,217	1-Jun-11	2011-0297912	8-Dec-11		
1651	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS WITH VERTICAL BIT LINES AND LATERALLY ALIGNED ACTIVE ELEMENTS AND METHODS THEREOF	WO	US11/039416	7-Jun-11	WO11/156351	15-Dec-11		
1652	Non-Volatile Memory having 3D Array of Read/Write Elements with Vertical Bit Lines and Laterally Aligned Active Elements and Methods Thereof	US	61/423,007	14-Dec-10				
1653	Non-Volatile Memory Having 3d Array of Read/Write Elements with Efficient Decoding of Vertical Bit Lines and Word Lines	CN	201180028664.3	7-Jun-11	CN102971798A	13-Mar-13	ZL201180028664.3	25-Nov-15
1654	Non-Volatile Memory Having 3d Array of Read/Write Elements with Efficient Decoding of Vertical Bit Lines and Word Lines	DE	11725299.9	7-Jun-11	2580759	17-Apr-13	2580759	13-Jan-16
1655	Non-Volatile Memory Having 3d Array of Read/Write Elements with Efficient Decoding of Vertical Bit Lines and Word Lines	EP	11725299.9	7-Jun-11	2580759	17-Apr-13	2580759	13-Jan-16
1656	Non-Volatile Memory Having 3d Array of Read/Write Elements with Efficient Decoding of Vertical Bit Lines and Word Lines	JP	2013-514297	7-Jun-11				
1657	Non-Volatile Memory Having 3d Array of Read/Write Elements with Efficient Decoding of Vertical Bit Lines and Word Lines	KR	2013-7000292	7-Jun-11				
1658	Non-Volatile Memory Having 3d Array of Read/Write Elements with Efficient Decoding of Vertical Bit Lines and Word Lines	TW	100120004	8-Jun-11	201207855	16-Feb-12		
1659	Non-Volatile Memory Having 3d Array of Read/Write Elements with Efficient Decoding of Vertical Bit Lines and Word Lines	US	13/151,224	1-Jun-11	2011-0299314	8-Dec-11	8,547,720	1-Oct-13

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1660	Non-Volatile Memory Having 3d Array of Read/Write Elements with Efficient Decoding of Vertical Bit Lines and Word Lines	WO	US11/039423	7-Jun-11	WO11/156357	15-Dec-11		
1661	Non-Volatile Memory having 3D Array of Read/Write Elements with Low Current Structures and Methods Thereof	CN	201180060500.9	13-Dec-11			ZL201180060500.9	
1662	Non-Volatile Memory having 3D Array of Read/Write Elements with Low Current Structures and Methods Thereof	CN	201510415257.8	13-Dec-11				
1663	Non-Volatile Memory having 3D Array of Read/Write Elements with Low Current Structures and Methods Thereof	US	14/149,601	7-Jan-14	2014-0179068	26-Jun-14	8,817,514	26-Aug-14
1664	Non-Volatile Memory having 3D Array of Read/Write Elements with Low Current Structures and Methods Thereof	KR	2013-7014979	13-Dec-11				
1665	Non-Volatile Memory having 3D Array of Read/Write Elements with Low Current Structures and Methods Thereof	US	13/323,766	12-Dec-11	2012-0147649	14-Jun-12	8,625,322	7-Jan-14
1666	Non-Volatile Memory having 3D Array of Read/Write Elements with Low Current Structures and Methods Thereof	WO	US11/064695	13-Dec-11				
1667	Non-Volatile Memory Having 3D Array of Read/Write Elements with Vertical Bit Lines and Select Devices and Methods Thereof	CN	201180060453.8	13-Dec-11			ZL201180060453.8	
1668	Non-Volatile Memory Having 3D Array of Read/Write Elements with Vertical Bit Lines and Select Devices and Methods Thereof	US	14/339,895	24-Jul-14	2014-0335671	13-Nov-14	8,958,228	17-Feb-15
1669	Non-Volatile Memory Having 3D Array of Read/Write Elements with Vertical Bit Lines and Select Devices and Methods Thereof	KR	2013-7014984	13-Dec-11				
1670	Non-Volatile Memory Having 3D Array of Read/Write Elements with Vertical Bit Lines and Select Devices and Methods Thereof	US	13/323,780	12-Dec-11	2012-0147650	14-Jun-12	8,824,183	2-Sep-14
1671	Non-Volatile Memory Having 3D Array of Read/Write Elements with Vertical Bit Lines and Select Devices and Methods Thereof	WO	US11/064700	13-Dec-11				
1672	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES	CN	201080023571.7	2-Apr-10	CN102449701A	9-May-12	ZL201080023571.7	25-Mar-15
1673	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES	EP	10712669.0	2-Apr-10	2417600	15-Feb-12		

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1674	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES	JP	2012-504732	2-Apr-10	2012-523647	4-Oct-12	5469239	7-Feb-14
1675	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES	KR	2011-7026206	2-Apr-10				
1676	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES	TW	099110911	8-Apr-10				
1677	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES	US	12/420,334	8-Apr-09	2010-0259960	14-Oct-10	7,983,065	19-Jul-11
1678	THREE-DIMENSIONAL ARRAY OF RE-PROGRAMMABLE NON-VOLATILE MEMORY ELEMENTS HAVING VERTICAL BIT LINES	WO	US10/029852	2-Apr-10	WO2010/117911	14-Oct-10		
1679	NON-VOLATILE MULTI-LEVEL RE-WRITABLE MEMORY CELL INCORPORATING A DIODE IN SERIES WITH MULTIPLE RESISTORS AND METHOD FOR WRITING SAME	TW	098112124	10-Apr-09	201007733	16-Feb-10		
1680	NON-VOLATILE MULTI-LEVEL RE-WRITABLE MEMORY CELL INCORPORATING A DIODE IN SERIES WITH MULTIPLE RESISTORS AND METHOD FOR WRITING SAME	US	12/242,417	30-Sep-08	2009-0257267	15-Oct-09	7,961,494	14-Jun-11
1681	NON-VOLATILE MULTI-LEVEL RE-WRITABLE MEMORY CELL INCORPORATING A DIODE IN SERIES WITH MULTIPLE RESISTORS AND METHOD FOR WRITING SAME	WO	US09/040187	10-Apr-09	WO09/126874	15-Oct-09		
1682	Reduced Complexity Array Line Drivers for 3D Matrix arrays	TW	099112909	23-Apr-10	201106370	16-Feb-11		
1683	Reduced Complexity Array Line Drivers for 3D Matrix arrays	US	12/385,964	24-Apr-09	2010-0271885	28-Oct-10	7,940,554	10-May-11
1684	Reduced Complexity Array Line Drivers for 3D Matrix arrays	WO	US10/031876	21-Apr-10	WO10/123978	28-Oct-10		
1685	A Memory Cell that Includes a Carbon-Based Reversible Resistance Switching Element Compatible with a Steering Element, and Methods of Forming the Same	TW	099136209	22-Oct-10	201125078	16-Jul-11		
1686	Memory Cell that Includes a Carbon-Based Reversible Resistance Switching Element Compatible with a Steering Element, and Methods of Forming the Same	US	12/834,942	13-Jul-10	2011-0095257	28-Apr-11	8,551,855	8-Oct-13

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1687	Memory Cell that Includes a Carbon-Based Reversible Resistance Switching Element Compatible with a Steering Element, and Methods of Forming the Same	WO	US10/052855	15-Oct-10	WO2011/049829	28-Apr-11		
1688	Memory Cell that Includes a Carbon-Based Reversible Resistance Switching Element Compatitle with a Steering Element, and Methods of Forming the Same	TW	099136211	22-Oct-10	201138173	1-Nov-11		
1689	Memory Cell that Includes a Carbon-Based Reversible Resistance Switching Element Compatitle with a Steering Element, and Methods of Forming the Same	US	12/835,236	13-Jul-10	2011-0095258	28-Apr-11	8,481,396	9-Jul-13
1690	Memory Cell that Includes a Carbon-Based Reversible Resistance Switching Element Compatitle with a Steering Element, and Methods of Forming the Same	WO	US10/052859	15-Oct-10	WO2011/049830	28-Apr-11		
1691	A Memory Cell that Includes a Carbon-Based Reversible Resistance Switching Element Compatible with a Steering Element, and Methods of Forming the Same	US	61/254,627	23-Oct-09				
1692	A Memory Cell that Includes a Carbon-Based Reversible Resistance Switching Element Compatitle with a Steering Element, and Methods of Forming the Same	US	61/254,631	23-Oct-09				
1693	Optimized Electrodes for Re-Ram	US	13/553,411	19-Jul-12	2012-0280201	8-Nov-12	8,637,845	28-Jan-14
1694	Optimized Electrodes for Re-Ram	US	12/364,732	3-Feb-09	2010-0117069	13-May-10	8,263,420	11-Sep-12
1695	Non-Volatile Memory having 3D Array of Read/Write Elements with Low Current Structures and Methods Thereof	CN	201510415257.8	13-Dec-11				
1696	Carbon- Based Films, and Methods of Forming The Same, Having Dielectric Filler Material and Exhibiting Reduced Thermal Resistance	US	12/415,011	31-Mar-09	2010-0245029	30-Sep-10	8,183,121	22-May-12
1697	Carbon- Based Firms, and Methods of Forming The Same, Having Dielectric Filler Material and Exhibiting Reduced Thermal Resistance	WO	US10/028497	24-Mar-10	WO10/117640	14-Oct-10		
1698	Methods and Apparatus for Generating Voltage References Using Transistor Threshold Differences	US	12/395,198	27-Feb-09	2010-0219804	2-Sep-10	7,999,529	16-Aug-11
1699	Methods and Apparatus for Generating Voltage References Using Transistor Threshold Differences	WO	US10/024764	19-Feb-10	WO2010/099046	2-Sep-10		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1700	Programming Reversible Resistance Switching Elements	CN	201080027431.7	8-Jun-10	102804277	28-Dec-12	ZL201080027431.7	16-Sep-15
1701	Programming Reversible Resistance Switching Elements	EP	10726382.4	8-Jun-10	2443630	25-Apr-12		
1702	Programming Reversible Resistance Switching Elements	US	13/397,448	15-Feb-12	2012-0147657	14-Jun-12	8,498,146	30-Jul-13
1703	Programming Reversible Resistance Switching Elements	JP	2012-516130	8-Jun-10				
1704	Programming Reversible Resistance Switching Elements	KR	2011-7028600	8-Jun-10				
1705	Programming Reversible Resistance Switching Elements	TW	099113933	30-Apr-10				
1706	Programming Reversible Resistance Switching Elements	US	12/488,159	19-Jun-09	2010-0321977	23-Dec-10	8,154,904	10-Apr-12
1707	Programming Reversible Resistance Switching Elements	WO	US10/037841	8-Jun-10	WO10/147809	23-Dec-10		
1708	Cross Point Non-Volatile Memory Devices with a Plurality of Pillars having Rounded Corners and Method of Manufacturing	CN	201080029635.4	10-Jun-10	CN102484119A	30-May-12	ZL201080029635.4	10-Dec-14
1709	Cross Point Non-Volatile Memory Devices with a Plurality of Pillars having Rounded Corners and Method of Manufacturing	DE	10727304.7	10-Jun-10	2449591	9-May-12	2449591	2-Apr-14
1710	Cross Point Non-Volatile Memory Devices with a Plurality of Pillars having Rounded Corners and Method of Manufacturing	EP	10727304.7	10-Jun-10	2449591	9-May-12	2449591	2-Apr-14
1711	Cross Point Non-Volatile Memory Devices with a Plurality of Pillars having Rounded Corners and Method of Manufacturing	GB	10727304.7	10-Jun-10	2449591	9-May-12	2449591	2-Apr-14
1712	Electrode Diffusions in Two-Terminal Non-Volatile Memory Devices	US	13/100,657	4-May-11	2011-0204313	25-Aug-11	8,592,793	26-Nov-13
1713	Methods to Improve Electrode Diffusions in Two-terminal Non-volatile Memory Devices	JP	2012-517565	10-Jun-10	2012-532450	13-Dec-12	5620481	26-Sep-14
1714	Methods to Improve Electrode Diffusions in Two-terminal Non-volatile Memory Devices	KR	2011-7030716	10-Jun-10				
1715	NON-VOLATILE MEMORY DEVICES AND METHOD OF MAKING THE SAME	TW	099121100	28-Jun-10	201114018	16-Apr-11		
1716	Methods to Improve Electrode Diffusions in Two-terminal Non-volatile Memory Devices	US	12/458,091	30-Jun-09	2010-0327254	30-Dec-10	7,955,981	7-Jun-11
1717	Methods to Improve Electrode Diffusions in Two-terminal Non-volatile Memory Devices	WO	US10/038130	10-Jun-10	WO11/008385	20-Jan-11		
1718	A Memory Cell that includes a Carbon-Based Memory Element and Methods of Forming the Same	TW	100107401	4-Mar-11	201145459	16-Dec-11		

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1719	Memory Cell that includes a Carbon-Based Memory Element and Methods of Forming the Same	US	12/717,457	4-Mar-10	2011-0215320	8-Sep-11	8,481,394	9-Jul-13
1720	A Memory Cell that includes a Carbon-Based Memory Element and Methods of Forming the Same	WO	US11/026431	28-Feb-11	WO11/109271	9-Sep-11		
1721	Method of Making Damascene Diodes with Sacrificial Material	CN	201080040859.5	13-Jul-10	CN102612748A	25-Jul-12	ZL201080040859.5	10-Jun-15
1722	Method of Making Damascene Diodes with Sacrificial Material	EP	10734617.3	13-Jul-10	2454754	23-May-12		
1723	Method of Making Damascene Diodes with Sacrificial Material	JP	2012-520722	13-Jul-10	2012-533885	27-Dec-12		
1724	Method of Making Damascene Diodes with Sacrificial Material	KR	2012-7003724	13-Jul-10				
1725	Method of Making Damascene Diodes with Sacrificial Material	TW	099123333	15-Jul-10	201133635	1-Oct-11		
1726	Method of Making Damascene Diodes with Sacrificial Material	US	12/458,543	15-Jul-09	2011-0014779	20-Jan-11	7,927,977	19-Apr-11
1727	Method of Making Damascene Diodes with Sacrificial Material	WO	US10/041836	13-Jul-10	WO2011/008767	20-Jan-11		
1728	Methods of Using Single Spacer to Triple Line/Space Frequency	US	12/689,677	19-Jan-10			7,871,909	18-Jan-11
1729	PIN DIODE WITH SIGE LOW CONTACT RESISTANCE AND METHOD FOR FORMING THE SAME	CN	201080041550.8	7-Sep-10	CN 102640289	15-Aug-12		
1730	PIN DIODE WITH SIGE LOW CONTACT RESISTANCE AND METHOD FOR FORMING THE SAME	EP	10760496.9	7-Sep-10				
1731	3D Polysilicon Diode With Low Contact Resistance and Method for Forming Same	US	13/479,093	23-May-12	2012-0228579	13-Sep-12	8,410,582	2-Apr-13
1732	PIN DIODE WITH SIGE LOW CONTACT RESISTANCE AND METHOD FOR FORMING THE SAME	JP	2012-529797	7-Sep-10	2013-505581	14-Feb-13		
1733	PIN DIODE WITH SIGE LOW CONTACT RESISTANCE AND METHOD FOR FORMING THE SAME	KR	2012-7008199	7-Sep-10				
1734	3D Polysilicon Diode With Low Contact Resistance and Method for Forming Same	TW	099129758	2-Sep-10				
1735	3D Polysilicon Diode With Low Contact Resistance and Method for Forming Same	US	12/562,079	17-Sep-09	2011-0062557	17-Mar-11	8,207,064	26-Jun-12
1736	PIN DIODE WITH SIGE LOW CONTACT RESISTANCE AND METHOD FOR FORMING THE SAME	WO	US10/047957	7-Sep-10	WO11/034750	24-Mar-11		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1737	Page Register Outside Array and Sense Amplifier Interface	CN	201080056156.1	13-Dec-10	CN102754160A	24-Oct-12	ZL201080056156.1	16-Sep-15
1738	Page Register Outside Array and Sense Amplifier Interface	EP	10796542.8	13-Dec-10	2513903	24-Oct-12	2513903	
1739	Page Register Outside Array and Sense Amplifier Interface	JP	2012-544687	13-Dec-10	2013-513903	22-Apr-13		
1740	Page Register Outside Array and Sense Amplifier Interface	KR	2012-7018463	13-Dec-10				
1741	Page Register Outside Array and Sense Amplifier Interface	TW	099142854	8-Dec-10	201145300	16-Dec-11		
1742	Page Register Outside Array and Sense Amplifier Interface	US	12/638,719	15-Dec-09	2011-0141788	16-Jun-11	8,223,525	17-Jul-12
1743	Page Register Outside Array and Sense Amplifier Interface	WO	US10/060153	13-Dec-10	WO11/075452	23-Jun-11		
1744	Program Cycle Skip	US	13/488,609	5-Jun-12	2012-0243349	27-Sep-12	8,427,890	23-Apr-13
1745	Program Cycle Skip	US	13/488,600	5-Jun-12	2012-0236663	20-Sep-12	8,395,948	12-Mar-13
1746	Program Cycle Skip	US	14/231,591	31-Mar-14				
1747	Program Cycle Skip	TW	099142855	8-Dec-10	201135739	16-Oct-11		
1748	Program Cycle Skip	US	12/638,729	15-Dec-09	2011-0141832	16-Jun-11	8,213,243	3-Jul-12
1749	Program Cycle Skip	WO	US10/060155	13-Dec-10				
1750	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	CN	200980122196.9	9-Apr-09	CN102067313A	18-May-11	ZL200980122196.9	8-May-13
1751	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	DE	09739405.0	9-Apr-09	2263258	22-Dec-10	2263258	4-Dec-13
1752	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	EP	09739405.0	9-Apr-09	2263258	22-Dec-10	2263258	4-Dec-13
1753	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	GB	09739405.0	9-Apr-09	2263258	22-Dec-10	2263258	4-Dec-13

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1754	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	JP	2011-504187	9-Apr-09	P2011-517122A	26-May-11		
1755	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	KR	2010-7022557	9-Apr-09				
1756	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	US	61/044,414	11-Apr-08				
1757	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	TW	098112133	10-Apr-09	201003847	16-Jan-10		
1758	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	US	12/410,789	25-Mar-09	2009-0256131	15-Oct-09	8,530,318	10-Sep-13
1759	Memory Cell that Employs a Selectively Fabricated Carbon Nano-Tube Reversible Resistance Switching Element Formed Over a Bottom Conductor and Methods for Forming the Same	WO	US09/040131	9-Apr-09	WO2009/134603	5-Nov-09		
1760	Memory System with Data Line Switching Scheme	US	13/479,145	23-May-12	2012-0257433	11-Oct-12	8,638,586	28-Jan-14
1761	Memory System with Data Line Switching Scheme	CN	200980158609.9	29-Sep-09	CN102405499A	4-Apr-12	ZL200980158609.9	9-Sep-15
1762	Memory System with Data Line Switching Scheme	DE	09793151.3	29-Sep-09	2422345		2422345	12-Aug-15
1763	Memory System with Data Line Switching Scheme	EP	09793151.3	29-Sep-09	2422345		2422345	12-Aug-15
1764	Memory System with Data Line Switching Scheme	US	13/601,869	31-Aug-12	2013-0010523	10-Jan-13	8,711,596	29-Apr-14
1765	Memory System with Data Line Switching Scheme	JP	2012-505873	29-Sep-09			5270040	17-May-13
1766	Memory System with Data Line Switching Scheme	KR	2011-7027603	29-Sep-09				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1767	Data dependent Data-line Switching Scheme	US	61/171,022	20-Apr-09				
1768	Memory System with Data Line Switching Scheme	TW	099111300	12-Apr-10			I494947	1-Aug-15
1769	Memory System with Data Line Switching Scheme	US	12/563,139	20-Sep-09	2010-0265750	21-Oct-10	8,279,650	2-Oct-12
1770	Memory System with Data Line Switching Scheme	WO	US09/058889	29-Sep-09	WO2010/123517	28-Oct-10		
1771	CONTINUOUS PROGRAMMING FOR NON-VOLATILE MEMORY	US	14/290,934	29-May-14				
1772	CONTINUOUS PROGRAMMING FOR NON-VOLATILE MEMORY	US	13/217,235	24-Aug-11	2011-0305071	15-Dec-11	8,238,174	7-Aug-12
1773	CONTINUOUS PROGRAMMING OF NON-VOLATILE MEMORY	US	13/537,029	28-Jun-12	2012-0287734	15-Nov-12	8,780,651	15-Jul-14
1774	CONTINUOUS PROGRAMMING OF RESISTIVE MEMORY USING STAGGERED PRECHARGE	CN	200980139725.6	29-Sep-09			ZL200980139725.6	14-Jan-15
1775	Continuous programming of resistive memory using staggered precharge	EP	09737244.5	29-Sep-09				
1776	CONTINUOUS PROGRAMMING FOR NON-VOLATILE MEMORY	JP	2011-530151	29-Sep-09	2012-504840	23-Feb-12	5384653	11-Oct-13
1777	CONTINUOUS PROGRAMMING FOR NON-VOLATILE MEMORY	KR	2011-7010496	29-Sep-09				
1778	CONTINUOUS PROGRAMMING FOR NON-VOLATILE MEMORY	TW	098133883	6-Oct-09	201032234	1-Sep-10		
1779	CONTINUOUS PROGRAMMING FOR NON-VOLATILE MEMORY	US	12/563,140	20-Sep-09	2010-0085822	8-Apr-10	8,027,209	27-Sep-11
1780	CONTINUOUS PROGRAMMING FOR NON-VOLATILE MEMORY	WO	US09/058890	29-Sep-09	WO10/042354	15-Apr-10		
1781	Method of Forming Contact Hole Arrays using a Hybrid Spacer Technique	TW	099120901	25-Jun-10	201120996	16-Jun-11		
1782	Method of Forming Contact Hole Arrays using a Hybrid Spacer Technique	US	12/458,017	29-Jun-09	2010-0330806	30-Dec-10	8,026,172	27-Sep-11
1783	Method of Forming Contact Hole Arrays using a Hybrid Spacer Technique	WO	US10/038125	10-Jun-10	WO2011/002590	6-Jan-11		
1784	Process for Forming Resistive Switching Memory Cells Using Nano-Particles	US	13/755,577	31-Jan-13	2014-0213032	31-Jul-14	8,877,586	4-Nov-14
1785	Process for Forming Resistive Switching Memory Cells Using Nano-Particles	WO	US14/013696	29-Jan-14	WO2014/120843	7-Aug-14		
1786	PUNCH-THROUGH DIODE STEERING ELEMENT	US	13/571,100	9-Aug-12	2012-0302029	29-Nov-12	8,575,715	5-Nov-13
1787	PUNCH-THROUGH DIODE STEERING ELEMENT	TW	099134953	13-Oct-10	201138088	1-Nov-11		
1788	PUNCH-THROUGH DIODE STEERING ELEMENT	US	12/582,509	20-Oct-09	2011-0089391	21-Apr-11	8,274,130	25-Sep-12
1789	PUNCH-THROUGH DIODE STEERING ELEMENT	WO	US10/053128	19-Oct-10				
1790	METHODS OF FORMING A REVERSIBLE RESISTANCE-SWITCHING METAL-INSULATOR-METAL STRUCTURE	US	12/631,913	7-Dec-09	2011-0133151	9-Jun-11	8,551,850	8-Oct-13

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1791	METHOD OF MAKING DAMASCENE DIODES USING SELECTIVE ETCHING METHODS	US	61/213,785	15-Jul-09				
1792	METHOD OF MAKING DAMASCENE DIODES USING SELECTIVE ETCHING METHODS	TW	099123336	15-Jul-10	201133636	1-Oct-11		
1793	METHOD OF MAKING DAMASCENE DIODES USING SELECTIVE ETCHING METHODS	US	12/656,306	25-Jan-10	2011-0014771	20-Jan-11	8,148,230	3-Apr-12
1794	METHOD OF MAKING DAMASCENE DIODES USING SELECTIVE ETCHING METHODS	WO	US10/041830	13-Jul-10	WO2011/008761	20-Jan-11		
1795	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS AND READ/WRITE CIRCUITS AND METHOD THEREOF	EP	11731579.6	7-Jun-11				
1796	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS AND READ/WRITE CIRCUITS AND METHOD THEREOF	US	13/973,218	22-Aug-13			8,824,191	2-Sep-14
1797	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS AND READ/WRITE CIRCUITS AND METHOD THEREOF	US	61/352,740	8-Jun-10				
1798	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS AND READ/WRITE CIRCUITS AND METHOD THEREOF	TW	100120032	8-Jun-11	201230041	16-Jul-12		
1799	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS AND READ/WRITE CIRCUITS AND METHOD THEREOF	US	13/151,204	1-Jun-11	2011-0299340	8-Dec-11	8,526,237	3-Sep-13
1800	NON-VOLATILE MEMORY HAVING 3D ARRAY OF READ/WRITE ELEMENTS AND READ/WRITE CIRCUITS AND METHOD THEREOF	WO	US11/039405	7-Jun-11	WO11/156343	15-Dec-11		
1801	Damascene Method of Making a Non-Volatile Memory Device	US	13/309,857	2-Dec-11	2012-0077318	29-Mar-12	8,222,091	17-Jul-12
1802	Damascene Method of Making a Non-Volatile Memory Device	TW	100101505	14-Jan-11	201135872	16-Oct-11		
1803	Damascene Method of Making a Non-Volatile Memory Device	US	12/693,322	25-Jan-10	2011-0183475	28-Jul-11	8,097,498	17-Jan-12
1804	Damascene Method of Making a Non-Volatile Memory Device	WO	US11/022400	25-Jan-11	WO11/091416	28-Jul-11		
1805	Memory Cell with Silicon-Containing Carbon Switching Layer and Methods for Forming the Same	EP	11703361.3	9-Feb-11	2539936	2-Jan-13	2539936	
1806	Memory Cell with Silicon-Containing Carbon Switching Layer and Methods for Forming the Same	KR	2012-7022208	9-Feb-11				
1807	Memory Cell with Silicon-Containing Carbon Switching Layer and Methods for Forming the Same	TW	100105854	22-Feb-11	201145632	16-Dec-11		

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1808	Memory Cell with Silicon-Containing Carbon Switching Layer and Methods for Forming the Same	US	12/711,810	24-Feb-10	2011-0204474	25-Aug-11	8,237,146	7-Aug-12
1809	Memory Cell with Silicon-Containing Carbon Switching Layer and Methods for Forming the Same	WO	US11/024162	9-Feb-11	WO11/106155	1-Sep-11		
1810	CARBON/TUNNELING-BARRIER/CARBON DIODE	CN	201080063987.1	8-Dec-10	CN102870246A	9-Jan-13	ZL201080063987.1	2-Dec-15
1811	CARBON/TUNNELING-BARRIER/CARBON DIODE	EP	10796527.9	8-Dec-10				
1812	CARBON/TUNNELING-BARRIER/CARBON DIODE	JP	2012-544632	8-Dec-10	2013-514667	25-Apr-13		
1813	CARBON/TUNNELING-BARRIER/CARBON DIODE	KR	2012-7018628	8-Dec-10				
1814	CARBON/TUNNELING-BARRIER/CARBON DIODE	TW	099143834	14-Dec-10				
1815	CARBON/TUNNELING-BARRIER/CARBON DIODE	US	12/639,840	16-Dec-09	2011-0140064	16-Jun-11	8,624,293	7-Jan-14
1816	CARBON/TUNNELING-BARRIER/CARBON DIODE	WO	US10/059555	8-Dec-10	WO11/084334	14-Jul-11		
1817	Soft Forming Reversible Resistivity-Switching Element for Bipolar Switching	US	61/249,946	8-Oct-09				
1818	Soft Forming Reversible Resistivity-Switching Element for Bipolar Switching	TW	099134257	7-Oct-10				
1819	Soft Forming Reversible Resistivity-Switching Element for Bipolar Switching	US	12/642,191	18-Dec-09			8,289,749	16-Oct-12
1820	Soft Forming Reversible Resistivity-Switching Element for Bipolar Switching	WO	US10/051666	6-Oct-10				
1821	Patterning Methods for High Density Pillar Structures	US	12/686,201	12-Jan-10			7,923,305	12-Apr-11
1822	Patterning Method for High Density Pillar Structures	US	13/463,260	3-May-12	2012-0276744	1-Nov-12	8,329,512	11-Dec-12
1823	Patterning Method for High Density Pillar Structures	US	13/216,688	24-Aug-11	2011-0306174	15-Dec-11	8,241,969	14-Aug-12
1824	Patterning Method for High Density Pillar Structures	TW	099147403	31-Dec-10	201135806	16-Oct-11		
1825	Patterning Method for High Density Pillar Structures	US	12/686,217	12-Jan-10	2011-0171815	14-Jul-11	8,026,178	27-Sep-11
1826	Patterning Method for High Density Pillar Structures	WO	US11/020848	11-Jan-11	WO2011/088050	21-Jul-11		
1827	Memory Cell with Carbon Switching Material Having a Reduced Cross-Sectional Area and Methods for Forming the Same	CN	201180029359.6	12-Apr-11	CN102939655A	20-Feb-13	ZL201180029359.6	25-Nov-15

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1828	Memory Cell with Carbon Switching Material Having a Reduced Cross-Sectional Area and Methods for Forming the Same	DE	11717383.1	12-Apr-11	2559068	20-Feb-13	2559068	20-May-15
1829	Memory Cell with Carbon Switching Material Having a Reduced Cross-Sectional Area and Methods for Forming the Same	EP	11717383.1	12-Apr-11	2559068	20-Feb-13	2559068	20-May-15
1830	Memory Cell with Carbon Switching Material Having a Reduced Cross-Sectional Area and Methods for Forming the Same	JP	2013-505037	12-Apr-11	P2013/524551A	17-Jun-13		
1831	Memory Cell with Carbon Switching Material Having a Reduced Cross-Sectional Area and Methods for Forming the Same	KR	2012-7026777	12-Apr-11				
1832	Memory Cell with Carbon Switching Material Having a Reduced Cross-Sectional Area and Methods for Forming the Same	TW	100113044	14-Apr-11	201203640	16-Jan-12		
1833	Memory Cell with Carbon Switching Material Having a Reduced Cross-Sectional Area and Methods for Forming the Same	US	12/760,156	14-Apr-10	2011-0254126	20-Oct-11	8,471,360	25-Jun-13
1834	Memory Cell with Carbon Switching Material Having a Reduced Cross-Sectional Area and Methods for Forming the Same	WO	US11/032039	12-Apr-11	WO11/130212	20-Oct-11		
1835	Non-Volatile Memory Array Architecture Incorporating 1T-1R NEAR 4F2 Memory Cell	CN	201080059504.0	22-Oct-10	CN102714057	3-Oct-12	ZL201080059504.0	25-Mar-15
1836	Non-Volatile Memory Array Architecture Incorporating 1T-1R NEAR 4F2 Memory Cell	EP	10779595.7	22-Oct-10	2494555	5-Sep-12		
1837	Non-Volatile Memory Array Architecture Incorporating 1T-1R NEAR 4F2 Memory Cell	KR	2012-7012391	22-Oct-10				
1838	Non-Volatile Memory Array Architecture Incorporating 1T-1R NEAR 4F2 Memory Cell	TW	099135981	21-Oct-10	201129985	1-Sep-11		
1839	Non-Volatile Memory Array Architecture Incorporating 1T-1R NEAR 4F2 Memory Cell	US	12/606,111	26-Oct-09	2011-0096588	28-Apr-11	8,233,309	31-Jul-12
1840	Non-Volatile Memory Array Architecture Incorporating 1T-1R NEAR 4F2 Memory Cell	WO	US10/053766	22-Oct-10	WO2011/056474	12-May-11		
1841	Rewritable Memory Device with Multi-Level, Write-Once Memory Cells	CN	201080056716.3	5-Nov-10	CN102656640A	5-Sep-12		
1842	Rewritable Memory Device with Multi-Level, Write-Once Memory Cells	EP	10782466.6	5-Nov-10	2517209	31-Oct-12		
1843	Rewritable Memory Device with Multi-Level, Write-Once Memory Cells	JP	2012-544515	5-Nov-10	2013-515330	2-May-13	5320511	19-Jul-13
1844	Rewritable Memory Device with Multi-Level, Write-Once Memory Cells	KR	2012-7015984	5-Nov-10			10-1213982	13-Dec-12
1845	Rewritable Memory Device with Multi-Level, Write-Once Memory Cells	TW	099142643	7-Dec-10	201135730	16-Oct-11		

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1846	Rewritable Memory Device with Multi-Level, Write-Once Memory Cells	US	12/643,561	21-Dec-09	2011-0149631	23-Jun-11	8,149,607	3-Apr-12
1847	Rewritable Memory Device with Multi-Level, Write-Once Memory Cells	WO	US10/055547	5-Nov-10	WO11/078917	30-Jun-11		
1848	Method of Programming a Non-Volatile Memory Cell by Reverse Biasing a Diode Steering Element to Set a Storage Element	US	12/703,289	10-Feb-10			8,547,725	1-Oct-13
1849	Memory Cell that Includes a Carbon-Based Memory Element and Methods of Forming the Same	TW	100106048	23-Feb-11	201135873	16-Oct-11		
1850	Memory Cell that Includes a Carbon-Based Memory Element and Methods of Forming the Same	US	12/714,359	26-Feb-10	2011-0210306	1-Sep-11		
1851	Memory Cell that Includes a Carbon-Based Memory Element and Methods of Forming the Same	WO	US11/024188	9-Feb-11	WO11/106156	10-Nov-11		
1852	In-Situ Passivation Methods to Improve Performance of PolySilicon Diode	TW	09914643	28-Dec-10	201131848	16-Sep-11		
1853	In-Situ Passivation Methods to Improve Performance of PolySilicon Diode	US	12/654,927	8-Jan-10	2011-0169126	14-Jul-11	8,450,181	28-May-13
1854	In-Situ Passivation Methods to Improve Performance of PolySilicon Diode	WO	US11/020293	6-Jan-11	WO11/085054	14-Jul-11		
1855	Memory Cell that Includes a Carbon-Based Memory Element and Methods of Forming the Same	TW	100114148	22-Apr-11	201203641	16-Jan-12		
1856	Memory Cell that Includes a Carbon-Based Memory Element and Methods of Forming the Same	US	12/765,955	23-Apr-10	2011-0260290	27-Oct-11	8,436,447	7-May-13
1857	Memory Cell that Includes a Carbon-Based Memory Element and Methods of Forming the Same	WO	US11/032850	18-Apr-11	WO11/133449	27-Oct-11		
1858	Methods and Apparatus to Increase Pattern Density by 2X Using Gap Fill of PECVD C	US	61/260,813	12-Nov-09				
1859	Three Dimensional Horizontal Diode Non-Volatile Memory Array and Method of Making Thereof	TW	100137164	13-Oct-11				
1860	Three Dimensional Horizontal Diode Non-Volatile Memory Array and Method of Making Thereof	US	12/905,445	15-Oct-10	2012-0091413	19-Apr-12	8,187,932	29-May-12
1861	Three Dimensional Horizontal Diode Non-Volatile Memory Array and Method of Making Thereof	WO	US11/055721	11-Oct-11	WO12/051159	19-Apr-12		
1862	Fabricating Voids Using Slurry Protect Coat Before Chemical-Mechanical Polishing	TW	100111393	31-Mar-11				

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1863	Fabricating Voids Using Slurry Protect Coat Before Chemical-Mechanical Polishing	WO	US11/030320	29-Mar-11				
1864	Modulation of Resistivity in Carbon-Based Read-Writeable Materials	TW	098146537	31-Dec-09	201034125	16-Sep-10		
1865	Modulation of Resistivity in Carbon-Based Read-Writeable Materials	US	12/650,417	30-Dec-09	2010-0163824	1-Jul-10	8,470,646	25-Jun-13
1866	Modulation of Resistivity in Carbon-Based Read-Writeable Materials	WO	US09/069875	30-Dec-09	WO2010/078467	8-Jul-10		
1867	Non-Volatile Memory Cell Containing Nanodots and Method of Making Thereof	US	61/282,408	4-Feb-10				
1868	Non-Volatile Memory Cell Containing Nanodots and Method of Making Thereof	TW	100104158	8-Feb-11	201140813	16-Nov-11		
1869	Non-Volatile Memory Cell Containing Nanodots and Method of Making Thereof	US	13/020,054	3-Feb-11	2011-0186799	4-Aug-11		
1870	Non-Volatile Memory Cell Containing Nanodots and Method of Making Thereof	WO	US11/023617	3-Feb-11	WO11/097389	11-Aug-11		
1871	Structure and Fabrication Method for Resistance-Change Memory Cell in 3-D Memory	US	61/307,398	23-Feb-10				
1872	Structure and Fabrication Method for Resistance-Change Memory Cell in 3-D Memory	TW	100106072	23-Feb-11	201203249	16-Jan-12		
1873	Structure and Fabrication Method for Resistance-Change Memory Cell in 3-D Memory	US	13/029,361	17-Feb-11	2011-0204316	25-Aug-11	8,686,419	1-Apr-14
1874	Structure and Fabrication Method for Resistance-Change Memory Cell in 3-D Memory	WO	US11/025768	22-Feb-11	WO2011/106329	1-Sep-11		
1875	Step Soft Program for Reversible Resistivity-Switching Elements	CN	201180019680.6	18-Feb-11	CN102893338A	23-Jan-13		
1876	Step Soft Program for Reversible Resistivity-Switching Elements	JP	2012-554047	18-Feb-11	2013-520761	6-Jun-13		
1877	Step Soft Program for Reversible Resistivity-Switching Elements	KR	2012-7024277	18-Feb-11				
1878	Step Initialization for Forming Reversible Resistivity-Switching Elements	US	61/305,868	18-Feb-10				
1879	Step Initialization For Forming Reversible Resistivity-Switching Elements	US	61/307,245	23-Feb-10				
1880	Step Soft Program for Reversible Resistivity-Switching Elements	TW	100105508	18-Feb-11	201135731	16-Oct-11		
1881	Step Soft Program for Reversible Resistivity-Switching Elements	US	12/949,146	18-Nov-10	2011-2055782	25-Aug-11	8,848,430	30-Sep-14
1882	Step Soft Program for Reversible Resistivity-Switching Elements	WO	US11/025367	18-Feb-11	WO2011/103379	25-Aug-11		

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1883	Non-Volatile Storage with Metal Oxide Switching Element	US	61/314,564	16-Mar-10				
1884	Non-Volatile Storage with Metal Oxide Switching Element and Methods for Fabricating the Same	US	13/848,603	21-Mar-13	2013-0234099	12-Sep-13	9,034,689	19-May-15
1885	TRAP PASSIVATION IN MEMORY CELL WITH METAL OXIDE SWITCHING ELEMENT	US	13/837,917	15-Mar-13	2013-0221311	29-Aug-13	8,987,046	24-Mar-15
1886	Non-Volatile Storage with Metal Oxide Switching Element	US	12/942,575	9-Nov-10	2011-0227026	22-Sep-11	8,435,831	7-May-13
1887	Resistance-Switching Memory Cell with Heavily Doped Metal Oxide Layer	US	12/842,798	23-Jul-10	2011-0227024	22-Sep-11	8,487,292	16-Jul-13
1888	Forming and Training Processes for Resistance Change Memory Cell	US	12/842,810	23-Jul-10	2011-0229990	22-Sep-11	8,216,862	10-Jul-12
1889	Bottom Electrodes for Use with Metal Oxide Resistivity Switching Materials	EP	11713107.8	16-Mar-11	2548239	23-Jan-13		
1890	Electrodes for USe with Resistivity Switching Materials	JP	2013-500131	16-Mar-11	P20013-522911A	13-Jun-13		
1891	Bottom Electrodes for Use with Metal Oxide Resistivity Switching Materials	KR	2012-7024030	16-Mar-11				
1892	Electrodes for USe with Resistivity Switching Materials	US	61/314,577	16-Mar-10				
1893	Electrodes for USe with Resistivity Switching Materials	TW	100108969	16-Mar-11	201145634	16-Dec-11		
1894	Bottom Electrodes for Use with Metal Oxide Resistivity Switching Layers	US	13/047,020	14-Mar-11	2011-0227020	22-Sep-11	8,772,749	8-Jul-14
1895	Bottom Electrodes for Use with Metal Oxide Resistivity Switching Materials	WO	US11/028394	16-Mar-11	WO11/115924	22-Sep-11		
1896	Alternating Bipolar Formnig Voltage for Resistivity-Switching Elements	US	61/333,533	11-May-10				
1897	Alternating Bipolar Formnig Voltage for Resistivity-Switching Elements	TW	100115639	4-May-11	201203252	16-Jan-12		
1898	Alternating Bipolar Formnig Voltage for Resistivity-Switching Elements	US	12/949,590	18-Nov-10	2011-0280059	17-Nov-11	8,385,102	26-Feb-13
1899	Alternating Bipolar Formnig Voltage for Resistivity-Switching Elements	WO	US11/035802	9-May-11	WO2011/143139	17-Nov-11		
1900	Counter Doping Compensation Methods to Improve Polysilicon Diode Performance	TW	100135103	28-Sep-11	201216540	16-Apr-12		
1901	Counter Doping Compensation Methods to Improve Polysilicon Diode Performance	US	12/892,633	28-Sep-10	2012-0074367	29-Mar-12	8,883,589	11-Nov-14
1902	Counter Doping Compensation Methods to Improve Polysilicon Diode Performance	WO	US11/051988	16-Sep-11	WO12/044473	5-Apr-12		
1903	Memory System with Reversible Resistivity Switching Using Pulses of Alternatrie Polarity	TW	100140954	9-Nov-11				

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1904	Memory System with Reversible Resistivity Switching Using Pulses of Alternatrie Polarity	US	12/948,375	17-Nov-10	2012-0120710	17-May-12	8,462,580	11-Jun-13
1905	Memory System with Reversible Resistivity Switching Using Pulses of Alternatrie Polarity	WO	US11/056126	13-Oct-11				
1906	Bipolar Storage Elements for Use in Memory Cells and Methods of Forming the Same	US	12/904,770	14-Oct-10	2012-0091418	19-Apr-12		
1907	Multi-Level Memory Arrays with Memory Cells that Employ Bipolar Storage Elements and Methods of Forming the Same	CN	201180060113.5	6-Oct-11	CN103314442A	18-Sep-13		
1908	Multi-Level Memory Arrays with Memory Cells that Employ Bipolar Storage Elements and Methods of Forming the Same	EP	11770030.2	6-Oct-11	2628181	21-Aug-13		
1909	Multi-Level Memory Arrays with Memory Cells that Employ Bipolar Storage Elements and Methods of Forming the Same	US	14/456,158	11-Aug-14	2014-0346433	27-Nov-14	9,105,576	11-Aug-15
1910	Multi-Level Memory Arrays with Memory Cells that Employ Bipolar Storage Elements and Methods of Forming the Same	KR	2013-7012138	6-Oct-11				
1911	Multi-Level Memory Arrays with Memory Cells that Employ Bipolar Storage Elements and Methods of Forming the Same	TW	100137392	14-Oct-11	201232544	1-Aug-12		
1912	Multi-Level Memory Arrays with Memory Cells that Employ Bipolar Storage Elements and Methods of Forming the Same	US	12/904,802	14-Oct-10	2012-0091427	19-Apr-12	8,841,648	23-Sep-14
1913	Multi-Level Memory Arrays with Memory Cells that Employ Bipolar Storage Elements and Methods of Forming the Same	WO	US11/055076	6-Oct-11	WO12/051041	19-Apr-12		
1914	Transistor Driven 3D Memory	CN	201180065151.X	15-Nov-11	CN103314410A	18-Sep-13	ZL201180065151.X	
1915	Transistor Driven 3D Memory	EP	11785883.7	15-Nov-11	2641248	25-Sep-13		
1916	Transistor Driven 3D Memory	KR	2013-7014221	15-Nov-11				
1917	Transistor Driven 3D Memory	TW	100140175	3-Nov-11	201230253	16-Jul-12		
1918	Transistor Driven 3D Memory	US	12/947,553	16-Nov-10	2012-0120709	17-May-12	8,351,243	8-Jan-13
1919	Transistor Driven 3D Memory	WO	US11/060812	15-Nov-11	WO12/068127	24-May-12		
1920	Memory Cell With Resistance-Switching Layers	TW	100121287	17-Jun-11	201212317	16-Mar-12		
1921	Memory Cell With Resistance-Switching Layers	US	13/157,191	9-Jun-11	2011-0310653	22-Dec-11	8,737,111	27-May-14
1922	Memory Cell With Resistance-Switching Layers	WO	US11/040103	10-Jun-11	WO2011/159581	19-Apr-12		
1923	Memory Cell With Resistance-Switching Layers And Lateral Arrangement	CN	201180029537.5	10-Jun-11	CN102986048A	20-Mar-13	ZL201180029537.5	1-Apr-15

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1924	Memory Cell With Resistance-Switching Layers And Lateral Arrangement	EP	11725853.3	10-Jun-11	2583322	24-Apr-13		
1925	Memory Cell With Resistance-Switching Layers And Lateral Arrangement	JP	2013-515404	10-Jun-11	2013-534722	5-Sep-13		
1926	Memory Cell With Resistance-Switching Layers And Lateral Arrangement	KR	2013-7001295	10-Jun-11				
1927	Memory Cell With Resistance-Switching Layers And Lateral Arrangement	TW	100121289	17-Jun-11	201212318	16-Mar-12		
1928	Memory Cell With Resistance-Switching Layers And Lateral Arrangement	US	13/157,200	9-Jun-11	2011-0310654	22-Dec-11	8,395,926	12-Mar-13
1929	Memory Cell With Resistance-Switching Layers And Lateral Arrangement	WO	US11/040104	10-Jun-11	WO2011/159582	22-Dec-11		
1930	Composition Of Memory Cell With Resistance-Switching Layers	CN	201180029544.5	10-Jun-11	CN103168372A	19-Jun-13	ZL201180029544.5	25-Nov-15
1931	Composition Of Memory Cell With Resistance-Switching Layers	EP	11729217.7	10-Jun-11	2583323	24-Apr-13		
1932	Composition Of Memory Cell With Resistance-Switching Layers	JP	2013-515405	10-Jun-11	2013-534723	5-Sep-13		
1933	Composition Of Memory Cell With Resistance-Switching Layers	KR	2013-7001491	10-Jun-11				
1934	Composition Of Memory Cell With Resistance-Switching Layers	TW	100121291	17-Jun-11	201212319	16-Mar-12		
1935	Composition Of Memory Cell With Resistance-Switching Layers	US	13/157,204	9-Jun-11	2011-0310655	22-Dec-11	8,520,424	27-Aug-13
1936	Composition Of Memory Cell With Resistance-Switching Layers	WO	US11/040105	10-Jun-11	WO2011/159583	22-Dec-11		
1937	Memory Cell With Resistance-Switching Layer And Breakdown Layer	CN	201180029615.1	10-Jun-11	CN103003971A	27-Mar-13	ZL201180029615.1	3-Jun-15
1938	Memory Cell With Resistance-Switching Layer And Breakdown Layer	EP	11729218.5	10-Jun-11	2583324	24-Apr-13		
1939	Memory Cell With Resistance-Switching Layer And Breakdown Layer	JP	2013-515406	10-Jun-11	2013-534724	5-Sep-13		
1940	Memory Cell With Resistance-Switching Layer And Breakdown Layer	KR	2013-7001492	10-Jun-11				
1941	Memory Cell With Resistance-Switching Layer And Breakdown Layer	TW	100121288	17-Jun-11	201209824	1-Mar-12		
1942	Memory Cell With Resistance-Switching Layer And Breakdown Layer	US	13/157,208	9-Jun-11	2011-0310656	22-Dec-11	8,395,927	12-Mar-13
1943	Memory Cell With Resistance-Switching Layer And Breakdown Layer	WO	US11/040107	10-Jun-11	WO2011/159584	22-Dec-11		
1944	RESISTANCE-CHANGE MEMORY CELL	US	61/356,327	18-Jun-10				
1945	Memory Cell With Resistance-Switching Layers	US	61/467,936	25-Mar-11				

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1946	Single Device Driver Circuit to Control Three-Dimensional Memory Element Array	CN	201180040413.7	15-Aug-11	CN103069496A	24-Apr-13		
1947	Single Device Driver Circuit to Control Three-Dimensional Memory Element Array	EP	11745908.1	15-Aug-11	2606488	26-Jun-13		
1948	Single Device Driver Circuit to Control Three-Dimensional Memory Element Array	US	13/608,098	10-Sep-12	2013-0003440	3-Jan-13	8,659,932	25-Feb-14
1949	Single Device Driver Circuit to Control Three-Dimensional Memory Element Array	JP	2013-524916	15-Aug-11	P2013-534349A	2-Sep-13		
1950	Single Device Driver Circuit to Control Three-Dimensional Memory Element Array	KR	2013-7005511	15-Aug-11				
1951	Single Device Driver Circuit to Control Three-Dimensional Memory Element Array	US	61/375,514	20-Aug-10				
1952	Single Device Driver Circuit to Control Three-Dimensional Memory Element Array	TW	100129274	16-Aug-11	201214441	1-Apr-12		
1953	Single Device Driver Circuit to Control Three-Dimensional Memory Element Array	US	12/938,028	2-Nov-10	2012-0044733	23-Feb-12	8,284,589	9-Oct-12
1954	Single Device Driver Circuit to Control Three-Dimensional Memory Element Array	WO	US11/47788	15-Aug-11	WO2012/024237	23-Feb-12		
1955	Punch-Through Diode	US	12/966,735	13-Dec-10	2012-0145984	14-Jun-12	8,557,654	15-Oct-13
1956	Memory Cells Having Storage Elements that Share Material Layers with Steering Elements and Methods of Forming the Same	US	13/783,585	4-Mar-13	2013-0175492	11-Jul-13	8,981,331	17-Mar-15
1957	Memory Cells Having Storage Elements that Share Material Layers with Steering Elements and Methods of Forming the Same	US	14/299,240	6-Jun-14	2014-0284538	25-Sep-14	8,969,845	3-Mar-15
1958	Memory Cells Having Storage Elements that Share Material Layers with Steering Elements and Methods of Forming the Same	US	12/905,047	14-Oct-10	2012-0091419	19-Apr-12	8,389,971	5-Mar-13
1959	Charge-Pump System that Dynamically Selects Number of Active Stages	CN	201180061403.1	30-Nov-11	CN103329414A	25-Sep-13		
1960	Charge-Pump System that Dynamically Selects Number of Active Stages	KR	2013-7016955	30-Nov-11				
1961	Charge-Pump System with Dynamically Selects Number of Active Stages	US	14/291,481	30-May-14				
1962	Charge-Pump System with Dynamically Selects Number of Active Stages	US	12/973,493	20-Dec-10	2012-0154022	21-Jun-12	8,339,185	25-Dec-12
1963	Charge-Pump System that Dynamically Selects Number of Active Stages	WO	US11/062662	30-Nov-11	WO12/087518	28-Jun-12		
1964	Three Dimensional Memory System with Page of Data Across Word Lines	US	13/039,581	3-Mar-11			8,553,476	8-Oct-13
1965	Diodes With Native Oxide Regions for use in Memory Arrays and Methods of Forming the Same	US	13/020,007	2-Feb-11	2012-0193756	2-Aug-12	8,866,124	21-Oct-14

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1966	Memory System with Reversible Switching using Pules of Alternatrie Polarity	TW	100140961	9-Nov-11				
1967	Memory System with Reversible Resistivity-Switching Using Pulses of Alternate Polarity	US	12/948,388	17-Nov-10	2012-0120711	17-May-12	8,355,271	15-Jan-13
1968	Memory System with Reversible Switching using Pules of Alternatrie Polarity	WO	US11/056130	13-Oct-11				
1969	Conditional Programming of Multibit Memory Cells	CN	201280024163.2	16-Mar-12	CN103548085A	29-Jan-14		
1970	Conditional Programming of Multibit Memory Cells	KR	2013-7026294	16-Mar-12				
1971	Balanced Method for Programming Multi-Layer Cell Memories	US	13/051,885	18-Mar-11	2012-0236624	20-Sep-12	8,934,292	13-Jan-15
1972	Conditional Programming of Multibit Memory Cells	WO	US12/029416	16-Mar-12	WO2012/129083	27-Sep-12		
1973	Three Dimensional Memory System with Column Pipeline	CN	201280011544.7	15-Feb-12	CN103703514A	2-Apr-14		
1974	Three Dimensional Memory System with Column Pipeline	EP	12709997.6	15-Feb-12	2681738	8-Jan-14		
1975	Three Dimensional Memory System with Column Pipeline	TW	101105886	22-Feb-12				
1976	Three Dimensional Memory System with Column Pipeline	US	13/039,574	3-Mar-11	2012-0224408	6-Sep-12	8,374,051	12-Feb-13
1977	Three Dimensional Memory System with Column Pipeline	WO	US12/025171	15-Feb-12	WO12/118618	7-Sep-12		
1978	Three Dimensional Memory System with Intelligent Select Circuit	US	13/039,593	3-Mar-11	2012-0224410	6-Sep-12	9,053,766	9-Jun-15
1979	Methods for Increasing Bottom Electrode Performance in Carbon-Based Memory Devices	US	61/448,477	2-Mar-11				
1980	Methods for Increasing Bottom Electrode Performance in Carbon-Based Memory Devices	US	13/204,772	8-Aug-11	2012-0223414	6-Sep-12		
1981	Methods for Increasing Bottom Electrode Performance in Carbon-Based Memory Devices	WO	US12/26914	28-Feb-12	WO12/118791	7-Sep-12		
1982	Non-Volatile Storage System Using Opposite Polarity Programming Signals for MIM Memory Cell	US	14/216,251	17-Mar-14	2014-0198558	17-Jul-14	9,047,949	2-Jun-15
1983	Non-Volatile Storage System Using Opposite Polarity Programming Signals for MIM Memory Cell	US	61/448,603	2-Mar-11				
1984	Non-Volatile Storage System Using Opposite Polarity Programming Signals for MIM Memory Cell	US	13/410,848	2-Mar-12	2012-0224413	6-Sep-12	8,699,259	15-Apr-14

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
1985	Bottom Electrodes for Use with Metal Oxide Resistivity Switching Layers	US	13/740,766	14-Jan-13	2013-0126821	23-May-13		
1986	Bottom Electrodes for Use with Resistivity Switching Layers	DE	11712085.7	14-Mar-11	2548238	23-Jan-13	2548238	22-Apr-15
1987	Bottom Electrodes for Use with Resistivity Switching Layers	EP	11712085.7	14-Mar-11	2548238	23-Jan-13	2548238	22-Apr-15
1988	Bottom Electrodes for Use with Resistivity Switching Layers	GB	11712085.7	14-Mar-11	2548238	23-Jan-13	2548238	22-Apr-15
1989	Bottom Electrodes for Use with Resistivity Switching Layers	JP	2013-500132	14-Mar-11	P2013-522912A	13-Jun-13		
1990	Bottom Electrodes for Use with Metal Oxide Resistivity Switching Layers	KR	2012-7024032	14-Mar-11				
1991	Bottom Electrodes for Use with Resistivity Switching Layers	TW	100108967	16-Mar-11	201145633	16-Dec-11		
1992	Bottom Electrodes for Use with Resistivity Switching Layers	US	13/047,098	14-Mar-11	2011-0227028	22-Sep-11	8,354,660	15-Jan-13
1993	Bottom Electrodes for Use with Resistivity Switching Layers	WO	US11/028396	14-Mar-11	WO2011/115926	22-Sep-11		
1994	Non-Volatile Storage System with Dual Block Programming	CN	201280020447.4	23-Apr-12	CN103765520A	30-Apr-14		
1995	Non-Volatile Storage System with Dual Block Programming	DE	12717569.3	23-Apr-12	2702591	5-Mar-14	2702591	18-Mar-15
1996	Non-Volatile Storage System with Dual Block Programming	EP	12717569.3	23-Apr-12	2702591	5-Mar-14	2702591	18-Mar-15
1997	Non-Volatile Storage System with Dual Block Programming	GB	12717569.3	23-Apr-12	2702591	5-Mar-14	2702591	18-Mar-15
1998	Non-Volatile Storage System with Dual Block Programming	US	14/201,899	9-Mar-14	2014-0185351	3-Jul-14		
1999	Non-Volatile Storage System with Dual Block Programming	KR	2013-7029448	23-Apr-12				
2000	Non-Volatile Storage System with Dual Block Programming	TW	101112839	11-Apr-12				
2001	Non-Volatile Storage System with Dual Block Programming	US	13/095,779	27-Apr-11	2012-0275210	1-Nov-12	8,699,293	15-Apr-14
2002	Non-Volatile Storage System with Dual Block Programming	WO	US12/034674	23-Apr-12	WO12/148852	1-Nov-12		
2003	Non-Volatile Memory Cell Containing A Nano-Rail Electrode	CN	201380014814.4	10-Jan-13				
2004	Non-Volatile Memory Cell Containing A Nano-Rail Electrode	KR	2014-7021481	10-Jan-13				
2005	Non-Volatile Memory Cell Containing A Nano-Rail Electrode	US	13/356,047	23-Jan-12	2013-0187114	25-Jul-13	8,710,481	29-Apr-14
2006	Non-Volatile Memory Cell Containing A Nano-Rail Electrode	WO	US13/020948	10-Jan-13	WO13/112291	1-Aug-13		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2007	Methods and Apparatus for Including an Air Gap in Carbon-Based Memory Devices	US	13/241,098	22-Sep-11	2013-0075685	28-Mar-13		
2008	Methods and Apparatus for Including an Air Gap in Carbon-Based Memory Devices	WO	US12/54602	11-Sep-12	WO2013/043410	28-Mar-13		
2009	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	CN	201180060491.3	12-Dec-11	CN104040633A	10-Sep-14		
2010	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	EP	11804618.4	12-Dec-11	2652740	23-Oct-13		
2011	Continuous Mesh Three Dimensional Non-Volatile Storage with Vertical Select Devices	US	14/089,718	25-Nov-13	2014-0080272	20-Mar-14	8,853,569	11-Nov-14
2012	Continuous Mesh Three Dimensional Non-Volatile Storage with Vertical Select Devices	US	14/089,715	25-Nov-13	2014-0078851	20-Mar-14	8,885,389	11-Nov-14
2013	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	KR	2013-7018358	12-Dec-11				
2014	Continuous Mesh Three Dimensional Non-Volatile Storage with Vertical Select Devices	US	13/323,680	12-Dec-11	2012-0147644	14-Jun-12	8,618,614	31-Dec-13
2015	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	CN	201410021018.X	12-Dec-11				
2016	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	EP	14152895.0	12-Dec-11	2731107	14-May-14		
2017	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	KR	2013-7018598	12-Dec-11				
2018	Three Dimensional Non-Volatile Storage with Dual Gated Vertical Select Devices	US	13/323,687	12-Dec-11	2012-0147645	14-Jun-12	8,885,381	11-Nov-14
2019	Three Dimensional Non-Volatile Storage with Connected Word Lines	US	14/746,003	22-Jun-15	2015-0325292	12-Nov-15		
2020	Three Dimensional Non-Volatile Storage with Connected Word Lines	US	13/323,695	12-Dec-11	2012-0147646	14-Jun-12	9,065,044	23-Jun-15
2021	Three Dimensional Non-Volatile Storage with Multi-Block Row Selection	US	13/323,573	12-Dec-11	2012-0147689	14-Jun-12	8,848,415	30-Sep-14
2022	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	CN	201410020325.6	12-Dec-11				
2023	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	EP	14152902.4	12-Dec-11	2731108	14-May-14		
2024	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	KR	2013-7018601	12-Dec-11				
2025	Three Dimensional Non-Volatile Storage with Three Device Driver for Row Select	US	13/323,703	12-Dec-11	2012-0147647	14-Jun-12	9,059,401	16-Jun-15
2026	Three Dimensional Non-Volatile Storage with Dual Gate Selection of Vertical Bit Lines	US	13/323,710	12-Dec-11	2012-0147648	14-Jun-12	8,619,453	31-Dec-13
2027	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	CN	201410021190.5	12-Dec-11	CN103915113A	9-Jul-14		
2028	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	EP	14152904.0	12-Dec-11	2731109	14-May-14		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2029	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	KR	2013-7018602	12-Dec-11				
2030	Three Dimensional Non-Volatile Storage with Dual Layers of Select Devices	US	13/323,583	12-Dec-11	2012-0147651	14-Jun-12	9,030,859	12-May-15
2031	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	CN	201410020388.1	12-Dec-11	CN103811516A	21-May-14		
2032	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	EP	14152910.7	12-Dec-11				
2033	Three Dimensional Non-Volatile Storage with Asymmetrical Vertical Select Devices	US	14/269,107	3-May-14	2014-0242764	28-Aug-14	9,048,422	2-Jun-15
2034	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	KR	2013-7018603	12-Dec-11				
2035	Three Dimensional Non-Volatile Storage with Asymmetrical Vertical Select Devices	US	13/323,717	12-Dec-11	2012-0147652	14-Jun-12	8,755,223	17-Jun-14
2036	Optimized Architecture for Three Dimensional Non-Volatile Storage Device with Vertical Bit Lines	US	61/526,764	24-Aug-11				
2037	Architecture for Three Dimensional Non-Volatile Storage with Vertical Bit Lines	WO	US11/064493	12-Dec-11	WO12/082654	21-Jun-12		
2038	Re-Writable Resistance-Switching Memory with Balanced Series Stack	US	13/363,252	31-Jan-12	2012-0127779	24-May-12	8,693,233	8-Apr-14
2039	NON-VOLATILE MEMORY CELL COMPRISING METAL OXIDE RESISTIVE MEMORY ELEMENT AND AN ANTIFUSE LAYER	CN	201280061039.3	26-Jul-12	CN103988264	13-Aug-14	ZL201280061039.3	26-Aug-15
2040	Non-Volatile Memorty Cell Containing an In-Cell Resistor	KR	2014-7012439	26-Jul-12				
2041	Non-Volatile Memorty Cell Containing an In-Cell Resistor	US	61/547,819	17-Oct-11				
2042	Non-Volatile Memory Cell Containing an In-Cell Resistor	US	13/552,355	18-Jul-12	2013-00094278	18-Apr-13	8,879,299	4-Nov-14
2043	Non-Volatile Memorty Cell Containing an In-Cell Resistor	WO	US12/048232	26-Jul-12	WO2013/058853	25-Apr-13		
2044	Resistive Random Access Memory with Low Current Operation	US	13/424,131	19-Mar-12	2012-0176831	12-Jul-12	8,520,425	27-Aug-13
2045	Resistive Random Access Memory with Low Current Operation	WO	US12/066912	28-Nov-12	WO2013/141904	26-Sep-13		
2046	Temperature Compensation of Conductive Bridge Memory Arrays	US	14/044,416	2-Oct-13	2014-0029356	30-Jan-14	8,750,066	10-Jun-14
2047	Temperature Compensation of Conductive Bridge Memory Arrays	US	14/256,925	19-Apr-14	2014-0226393	14-Aug-14	9,047,983	2-Jun-15
2048	Temperature Compensation of Conductive Bridge Memory Arrays	US	13/354,796	20-Jan-12	2013-0188431	25-Jul-13	8,576,651	5-Nov-13
2049	Composition Of Memory Cell With Resistance-Switching Layers	CN	201280065802.X	6-Sep-12	CN104040746A	10-Sep-14		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2050	Composition Of Memory Cell With Resistance-Switching Layers	KR	2014-7015277	6-Sep-12				
2051	Composition Of Memory Cell With Resistance-Switching Layers	US	13/408,394	29-Feb-12	2012-0153249	21-Jun-12	8,724,369	13-May-14
2052	Composition Of Memory Cell With Resistance-Switching Layers	WO	US12/053860	6-Sep-12				
2053	Composition of Memory Cell with Resistance Switching Layers	US	61/556,486	7-Nov-11				
2054	Low Forming Voltage Non-Volatile Storage Device	US	14/996,144	14-Jan-16				
2055	Low Forming Voltage Non-Volatile Storage Device	US	61/582,017	30-Dec-11				
2056	Low Forming Voltage Non-Volatile Storage Device	US	13/709,349	10-Dec-12	2013-0170283	4-Jul-13	9,269,425	23-Feb-16
2057	Low Forming Voltage Non-Volatile Storage Device	WO	US12/069676	14-Dec-12	WO2013/101499	4-Jul-13		
2058	Resistance-Switching Memory Cells Having Reduced Metal Migration and Low Current Operation and Methods of Forming the Same	US	13/465,263	7-May-12	2013-00292634	7-Nov-13		
2059	Resistance-Switching Memory Cells Having Reduced Metal Migration and Low Current Operation and Methods of Forming the Same	WO	US13/039208	2-May-13	WO13/169551	14-Nov-13		
2060	Three Dimensional Non-Volatile Storage with Interleaved Vertical Select Devices above and below Vertical Bit Lines	EP	13727681.2	8-May-13	2852977	1-Apr-15		
2061	Three Dimensional Non-Volatile Storage with Interleaved Vertical Select Devices above and below Vertical Bit Lines	KR	2014-7035219	8-May-13				
2062	Three Dimensional Non-Volatile Storage with Interleaved Vertical Select Devices above and below Vertical Bit Lines	US	61/647,488	15-May-12				
2063	Three Dimensional Non-Volatile Storage with Interleaved Vertical Select Devices above and below Vertical Bit Lines	US	13/886,874	3-May-13	2013-0308363	21-Nov-13	9,171,584	27-Oct-15
2064	Three Dimensional Non-Volatile Storage with Interleaved Vertical Select Devices above and below Vertical Bit Lines	WO	US13/040147	8-May-13	WO13/173140	21-Nov-13		
2065	Non-Volatile Memory Having 3D Array Architecture with Vertical Bit Line Voltage Control & Merthods Thereof	CN		31-May-13				
2066	Non-Volatile Memory Having 3D Array Architecture with Vertical Bit Line Voltage Control & Merthods Thereof	KR	2014-7036718	31-May-13				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2067	Non-Volatile Memory Having 3D Array Architecture with Vertical Bit Lines and Staircase Word Lines and Methods Thereof	US	61/660,490	15-Jun-12				
2068	Non-Volatile Memory Having 3D Array Architecture with Vertical Bit Line Voltage Control & Merthods Thereof	US	13/794,344	11-Mar-13	2013-0336036	19-Dec-13	9,281,029	8-Mar-16
2069	Non-Volatile Memory Having 3D Array Architecture with Vertical Bit Line Voltage Control & Merthods Thereof	WO	US13/043779	31-May-13				
2070	Method of Forming Crack Free Gap-Fill	US	61/738,878	18-Dec-12				
2071	Method of Forming Crack Free Gap-Fill	US	13/742,239	15-Jan-13	2014-0170847	19-Jun-14	8,937,011	20-Jan-15
2072	Memories with Cylindrical Read/Write Stacks	US	61/662,824	21-Jun-12				
2073	Memories with Cylindrical Read/Write Stacks	US	13/789,375	7-Mar-13	2013-0229846	5-Sep-13	9,227,456	5-Jan-16
2074	Memories with Cylindrical Read/Write Stacks	WO	US13/046379	18-Jun-13				
2075	METHOD FOR FORMING RESISTANCE-SWITCHING MEMORY CELL WITH MULTIPLE ELECTRODES USING NANO-PARTICLE HARD MASK	US	13/767,649	14-Feb-13	2014-0227853	14-Aug-14		
2076	RESISTANCE-SWITCHING MEMORY CELL WITH MULTIPLE RAISED STRUCTURES IN A BOTTOM ELECTRODES	US	13/767,663	14-Feb-13	2014-0225057	14-Aug-14	9,123,890	1-Sep-15
2077	RESISTANCE-SWITCHING MEMORY CELL WITH MULTIPLE RAISED STRUCTURES IN A BOTTOM ELECTRODE	US	14/807,370	23-Jul-15	2015-0333105	19-Nov-15		
2078	Support Lines to Prevent Line Collapse in Arrays	US	13/644,119	3-Oct-12	2014-0091381	3-Apr-14	8,741,714	3-Jun-14
2079	Support Lines to Prevent Line Collapse in Arrays	WO	US13/062774	30-Sep-13	WO2014/055460	15-Jan-15		
2080	Non-Volatile Memory Having 3D Array Architecture with Vertical Bit Lines and Staircase Word Lines And Methods Thereof	US	61/705,766	26-Sep-12				
2081	Program Cycle Skip Evaluation Before Write Operations in Non-Volatile Memory	US	13/839,366	15-Mar-13	2014-0269106	18-Sep-14	8,947,944	3-Feb-15
2082	Program Cycle Skip Evaluation Before Write Operations in Non-Volatile Memory	WO	US14/019740	1-Mar-14	WO2014/149585	25-Sep-14		
2083	Dynamic Address Grouping for Parallel Programming in Non-Volatile Memory	US	13/839,300	15-Mar-13	2014-0281135	18-Sep-14	8,947,972	3-Feb-15
2084	Dynamic Address Grouping for Parallel Programming in Non-Volatile Memory	WO	US14/019741	1-Mar-14	WO2014/149586	25-Sep-14		
2085	ReRAM FORMING WITH RESET AND ILOAD COMPENSATION	US	13/781,503	28-Feb-13	2014-0241035	28-Aug-14	9,007,810	14-Apr-15

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2086	ReRAM FORMING WITH RESET AND ILOAD COMPENSATION	WO	US14/017840	21-Feb-14	WO14/133912	4-Sep-14		
2087	Load and Short Current Measurement by Current Summation Technique	US	14/254,880	16-Apr-14	2014-0226417	14-Aug-14	8,885,401	11-Nov-14
2088	Load and Short Current Measurement by Current Summation Technique	US	13/754,801	30-Jan-13	2014-0211553	31-Jul-14	8,842,468	23-Sep-14
2089	Smart READ Scheme for Memory Array Sensing	US	13/773,963	22-Feb-13	2014-0241090	28-Aug-14	8,885,428	11-Nov-14
2090	Smart READ Scheme for Memory Array Sensing	WO	US14/017252	20-Feb-14	WO2014/130604	28-Aug-14		
2091	Compensation Scheme for Non-Volatile Memory	US	14/506,607	4-Oct-14	2015-0023113	22-Jan-15	8,988,936	24-Mar-15
2092	Compensation Scheme for Non-Volatile Memory	US	14/254,883	16-Apr-14	2014-0233327	21-Aug-14	8,897,064	25-Nov-14
2093	Compensation Scheme for Non-Volatile Memory	US	14/506,610	4-Oct-14	2015-0023115	22-Jan-15	8,934,295	13-Jan-15
2094	Compensation Scheme for Non-Volatile Memory	US	13/773,078	21-Feb-13	2014-0233329	21-Aug-14	8,885,400	11-Nov-14
2095	Compensation Scheme for Non-Volatile Memory	WO	US14/017217	19-Feb-14	WO2014/130586	28-Aug-14		
2096	Integrated Circuit Manufacturing	US	61/720,705	31-Oct-12				
2097	SEMICONDUCTOR DEVICE MANUFACTURING LINE	US	14/032,041	19-Sep-13	2014-0119858	1-May-14		
2098	SEMICONDUCTOR DEVICE MANUFACTURING LINE	WO	US13/065686	18-Oct-13				
2099	Methods and Apparatus for High Capacity Anodes for Lithium Batteries	CN	201480015289.2	13-Mar-14	CN105190949A	23-Dec-15		
2100	Methods and Apparatus for High Capacity Anodes for Lithium Batteries	EP	14714909.0	13-Mar-14				
2101	Methods and Apparatus for High Capacity Anodes for Lithium Batteries	US	13/827,980	14-Mar-13	2014-0272576	18-Sep-14		
2102	Methods and Apparatus for High Capacity Anodes for Lithium Batteries	WO	US14/026849	13-Mar-14	WO2014/152036	25-Sep-14		
2103	Methods and Apparatus for High Capacity Anodes for Lithium Batteries	US	13/828,301	14-Mar-13	2014-0272577	18-Sep-14		
2104	Methods and Apparatus for High Capacity Anodes for Lithium Batteries	WO	US14/026868	13-Mar-14	WO14/152044	25-Sep-14		
2105	SET/RESET ALGORITHM WHICH DETECTS AND REPAIRS WEAK CELLS IN RESISTIVE-SWITCHING MEMORY DEVICE	US	13/772,729	21-Feb-13	2014-0233299	21-Aug-14	8,861,258	14-Oct-14
2106	Methods and Apparatus for Metal Oxide Reversible Resistance-Switching Memory Devices	US	13/792,100	10-Mar-13	2014-0252298	11-Sep-14		

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2107	Methods and Apparatus for Metal Oxide Reversible Resistance-Switching Memory Devices	WO	US14/019731	1-Mar-14	WO2014/163994	9-Oct-14		
2108	Non-Volatile Memory Having 3D Array Architecture with Vertical Bit Lines and Staircase Word Lines and Methods Thereof	CN	201380041348.9	12-Jun-13				
2109	Non-Volatile Memory Having 3D Array Architecture with Vertical Bit Lines and Staircase Word Lines and Methods Thereof	KR	2014-7036709	12-Jun-13				
2110	Non-Volatile Memory Having 3D Array Architecture with Staircase Word Lines And Vertical Bit Lines and Methods Thereof	US	13/840,759	15-Mar-13	2013-0336038	19-Dec-13	9,147,439	29-Sep-15
2111	Non-Volatile Memory Having 3D Array Architecture with Vertical Bit Lines and Staircase Word Lines and Methods Thereof	WO	US13/045466	12-Jun-13				
2112	Method for Forming Staircase Word Lines in a 3D Non-Volatile Memory Having Vertical Bit Lines	CN	201380041328.1	12-Jun-13				
2113	Method for Forming Staircase Word Lines in a 3D Non-Volatile Memory Having Vertical Bit Lines	KR	2014-7036716	12-Jun-13				
2114	Method for Forming Staircase Word Lines in a 3D Non-Volatile Memory Having Vertical Bit Lines	US	13/840,201	15-Mar-13			8,895,437	25-Nov-14
2115	Method for Forming Staircase Word Lines in a 3D Non-Volatile Memory Having Vertical Bit Lines	WO	US13/045481	12-Jun-13				
2116	3D Memory Having Vertical Switches with Surround Gates and Method Thereof	CN	201380041340.2	13-Jun-13				
2117	3D Memory Having Vertical Switches with Surround Gates and Method Thereof	KR	2014-7036713	13-Jun-13				
2118	3D Memory Having Vertical Switches with Surround Gates and Method Thereof	US	13/838,782	15-Mar-13	2013-0336037	19-Dec-13		
2119	3D Memory Having Vertical Switches with Surround Gates and Method Thereof	WO	US13/045636	13-Jun-13				
2120	3D Memory with Vertical Bit Lines and Staircase Word Lines and Vertical Switches and Methods Thereof	CN	201380041322.4	4-Jun-13				
2121	3D Memory with Vertical Bit Lines and Staircase Word Lines and Vertical Switches and Methods Thereof	KR	2014-7036711	4-Jun-13				
2122	3D Memory with Vertical Bit Lines and Staircase Word Lines and Vertical Switches and Methods Thereof	US	13/835,032	15-Mar-13	2013-0339571	19-Dec-13	8,923,050	30-Dec-14

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2123	3D Memory with Vertical Bit Lines and Staircase Word Lines and Vertical Switches and Methods Thereof	WO	US13/044079	4-Jun-13				
2124	Method for Forming a Surround Gate of Vertical Switch in a 3D Memory	US	61/747,837	31-Dec-12				
2125	Non-Volatile Storage System Biasing Conditions for Standby and First Read	US	14/700,134	29-Apr-15	2015-0248933	3-Sep-15	9,208,873	8-Dec-15
2126	Non-Volatile Storage System Biasing Conditions for Standby and First Read	US	61/772,793	5-Mar-13				
2127	Non-Volatile Storage System Biasing Conditions for Standby and First Read	US	14/197,136	4-Mar-14	2014-0254242	11-Sep-14	9,047,943	2-Jun-15
2128	Method to Improve SET yield with low temperature initialization for 3D memory array	US	61/772,131	4-Mar-13				
2129	Vertical Bit Line TFT Decoder for High Voltage Operation	US	13/788,990	7-Mar-13	2014-0252454		9,165,933	20-Oct-15
2130	Vertical Bit Line TFT Decoder for High Voltage Operation	WO	US14/018125	25-Feb-14	WO2014/137652	12-Sep-14		
2131	Logic Scheme to Decouple Slow Outbound DDR2 Read Data	US	61/772,241	4-Mar-13				
2132	ASYNCHRONOUS FIFO BUFFER FOR MEMORY ACCESS	US	14/193,917	28-Feb-14				
2133	ASYNCHRONOUS FIFO BUFFER FOR MEMORY ACCESS	WO	US14/019736	1-Mar-14	WO2014/137847	12-Sep-14		
2134	Charge pump with a power-controlled clock buffer to reduce power consumption and output voltage ripple	US	14/258,934	22-Apr-14			8,860,501	14-Oct-14
2135	Charge pump with a power-controlled clock buffer to reduce power consumption and output voltage ripple	US	61/763,432	11-Feb-13				
2136	Charge pump with a power-controlled clock buffer to reduce power consumption and output voltage ripple	US	14/101,164	9-Dec-13	2014-0225652	14-Aug-14	8,836,412	16-Sep-14
2137	3D Non-Volatile Memory Having Low-Current Cells and Methods	CN	201480025600.1	5-Mar-14				
2138	3D Non-Volatile Memory Having Low-Current Cells and Methods	EP	14710775.9	5-Mar-14				
2139	3D Non-Volatile Memory Having Low-Current Cells and Methods	US	61/773,043	5-Mar-13				
2140	3D Non-Volatile Memory Having Low-Current Cells and Methods	US	14/196,956	4-Mar-14	2014-0254231	11-Sep-14	9,064,547	23-Jun-15
2141	3D Non-Volatile Memory Having Low-Current Cells and Methods	WO	US14/020611	5-Mar-14	WO2014/138182			

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2142	Vertical Bit Line Non-Volatile Memory Systems and Methods of Fabrication	US	14/938,637	11-Nov-15	2016-0064222	3-Mar-16		
2143	Process Flow to Realize a Vertical Bit Line Rerem Memory	US	61/772,256	4-Mar-13				
2144	Vertical Bit Line Non-Volatile Memory Systems and Methods of Fabrication	US	14/196,904	4-Mar-14	2014-0248763	4-Sep-14	9,202,694	1-Dec-15
2145	Vertical Bit Line Non-Volatile Memory Systems and Methods of Fabrication	WO	US14/020416	4-Mar-14	WO2014/138124	12-Sep-14		
2146	High Capacity Select Switches for Three Dimensional Structures	US	13/925,662	24-Jun-13	2014-0374688	25-Dec-14	8,933,516	13-Jan-15
2147	VERTICAL BIT LINE WIDE BAND GAP TFT DECODER	US	14/793,167	7-Jul-15	2015-0311256	29-Oct-15		
2148	VERTICAL BIT LINE WIDE BAND GAP TFT DECODER	US	14/020,647	6-Sep-13	2015-0069320	12-Mar-15	9,105,468	11-Aug-15
2149	VERTICAL BIT LINE WIDE BAND GAP TFT DECODER	WO	US14/054080	4-Sep-14	WO2015/035038	12-Mar-15		
2150	FET LOW CURRENT 3D ReRAM NON-VOLATILE STORAGE	US	14/025,420	12-Sep-13	2015-0070965	12-Mar-15		
2151	FET LOW CURRENT 3D ReRAM NON-VOLATILE STORAGE	WO	US14/054864	9-Sep-14	WO2015/038557	19-Mar-15		
2152	METHOD OF OPERATING FET LOW CURRENT 3D Re-RAM	US	14/591,546	7-Jan-15	2015-0170742	18-Jun-15		
2153	METHOD OF OPERATING FET LOW CURRENT 3D Re-RAM	US	14/025,442	12-Sep-13	2015-0070966	12-Mar-15	8,995,169	31-Mar-15
2154	Vertical Cross Point ReRAM Forming Method	US	14/732,766	7-Jun-15	2015-0269998	24-Sep-15		
2155	Vertical Cross Point ReRAM Forming Method	US	14/246,052	5-Apr-14	2014-0301130	9-Oct-14	9,202,566	1-Dec-15
2156	MULTIPLE LAYER FORMING SCHEME FOR VERTICAL CROSS POINT RERAM	US	14/887,532	20-Oct-15	2016-0042789	11-Feb-16		
2157	MULTIPLE LAYER FORMING SCHEME FOR VERTICAL CROSS POINT RERAM	US	14/246,053	5-Apr-14	2014-0301131	9-Oct-14	9,196,362	24-Nov-15
2158	Vertical Cross Point ReRAM Forming Method	US	61/809,206	5-Apr-13				
2159	Method of Inhibiting Wire Collapse	US	13/862,222	12-Apr-13			8,802,561	12-Aug-14
2160	Read Operation Noise Compensation Techniques	US	61/816,893	29-Apr-13				
2161	Vertical Cross Point RERAM SA Local Feedbak to Control Bit Line Voltage	CN	201480021568.X	21-May-14				
2162	Vertical Cross Point RERAM SA Local Feedbak to Control Bit Line Voltage	DE	US2014/038954	21-May-14				
2163	Vertical Cross Point RERAM SA Local Feedbak to Control Bit Line Voltage	US	61/825,878	21-May-13				
2164	Sense Amplifier Local Feedbak to Control Bit Line Voltage	US	14/283,034	20-May-14	2014-0347912	27-Nov-14		
2165	Vertical Cross Point RERAM SA Local Feedbak to Control Bit Line Voltage	WO	US14/038954	21-May-14	WO2014*190046	27-Nov-14		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2166	Differential Current Sense Amplifier and Method for Non-Volatile Memory	CN	201480021580.0	4-Jun-14				
2167	Differential Current Sense Amplifier and Method for Non-Volatile Memory	DE	112014001489.3	4-Jun-14				
2168	Differential Current Sense Amplifier and Method for Non-Volatile Memory	US	13/918,833	14-Jun-13	2014-0369132	18-Dec-14	9,123,430	1-Sep-15
2169	Differential Current Sense Amplifier and Method for Non-Volatile Memory	WO	US14/040925	4-Jun-14				
2170	Short Pulse Buffer Booster	US	61/833,869	11-Jun-13				
2171	High Aspect Trench Fill Using Selective Deposition of NSG	US	61/839,674	26-Jun-13				
2172	Vertical 1T-1R Memory Cells, Memory Arrays and Methods of Forming the Same	US	14/075,010	8-Nov-13	2015-0131360	14-May-15	9,099,385	4-Aug-15
2173	Vertical 1T-1R Memory Cells, Memory Arrays and Methods of Forming the Same	WO	US14/062951	29-Oct-14	WO2015/069524	14-May-15		
2174	Vertical Thin Film Transistor Selection Devices and Methods of Fabrication	US	14/197,985	5-Mar-14	2015-0255619	10-Sep-15		
2175	Vertical Thin Film Transistors in Non-Volatile Storage Systems	US	14/195,636	3-Mar-14	2015-0249112	3-Sep-15		
2176	Transistor Device with Gate Bottom Isolation and Method of Making Thereof	US	14/224,290	25-Mar-14	2015-0279850	1-Oct-15		
2177	Transistor Device with Gate Bottom Isolation and Method of Making Thereof	WO	US15/021720	20-Mar-15				
2178	Transistor Device and Method of Making Thereof	US	14/206,196	12-Mar-14	2015-0263074	17-Sep-15		
2179	Transistor Device and Method of Making Thereof	WO	US15/019431	9-Mar-15	WO15/138314	9-Sep-15		
2180	MULTILEVEL CONTACT TO A 3D MEMORY ARRAY AND METHOD OF MAKING THEREOF	US	14/643,211	10-Mar-15				
2181	Multilevel Contact to a 3D Memory Array and Method of Making Thereof	CN	US2014/071397	19-Dec-14				
2182	Multilevel Contact to a 3D Memory Array and Method of Making Thereof	EP	14824733.1	19-Dec-14				
2183	Multilevel Contact to a 3D Memory Array and Method of Making Thereof	KR	US2014/071397	19-Dec-14				
2184	Multilevel Contact to a 3D Memory Array and Method of Making Thereof	US	14/136,103	20-Dec-13	2015-0179659	25-Jun-15		
2185	Multilevel Contact to a 3D Memory Array and Method of Making Thereof	WO	US14/071397	19-Dec-14	WO15/095653	25-Jun-15		
2186	Trench Multilevel Contact to a 3D Memory Array and Method of Making Thereof	US	14/150,162	8-Jan-14	2015-0194380	9-Jul-15	9,230,905	5-Jan-16
2187	Trench Multilevel Contact to a 3D Memory Array and Method of Making Thereof	WO	US14/072678	30-Dec-14	WO15/105709	16-Jul-15		

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2188	Oxygen Rich Electrodes for ReRAM Improvement	US	61/858,514	25-Jul-13				
2189	Improved Shared-Gate Vertical-TFT for VBL Array	US	61/860,061	31-Jul-13				
2190	SHARED-GATE VERTICAL-TFT FOR VERTICAL BIT LINE ARRAY	US	14/340,454	24-Jul-14	2015-0036414	5-Feb-15	9,236,122	12-Jan-16
2191	SHARED-GATE VERTICAL-TFT FOR VERTICAL BIT LINE ARRAY	WO	US14/048259	25-Jul-14	WO2015/017281	5-Feb-15		
2192	Deterministic Multi-Level Cell Programming in ReRAM	US	61/869,340	23-Aug-13				
2193	Methods to Reduce Location-based Variations in Switching Characteristics of 3D ReRAM Arrays	US	61/873,779	4-Sep-13				
2194	Methods and Systems to Reduce Location-based Variations in Switching Characteristics of 3D ReRAM Arrays	US	14/462,374	18-Aug-14	2014-0353573	4-Dec-14		
2195	Methods to Reduce Location-based Variations in Switching Characteristics of 3D ReRAM Arrays	WO	US14/053286	28-Aug-14	WO2015/034756	12-Mar-15		
2196	METHODS AND APPARATUS FOR VERTICAL CROSS POINT RE-RAM ARRAY BIAS CALIBRATION	US	14/502,093	30-Sep-14				
2197	APPARATUS AND METHODS FOR SENSING HARD BIT AND SOFT BITS	US	14/500,476	29-Sep-14				
2198	APPARATUS AND METHODS FOR SENSING HARD BIT AND SOFT BITS	WO	US15/047626	30-Aug-15				
2199	ReRam Switching using Multiple Pulses with Verify Skip	US	61/910,216	29-Nov-13				
2200	FLOATING STAIRCASE WORD LINES AND PROCESS IN A 3D NON-VOLATILE MEMORY HAVING VERTICAL BIT LINES	US	14/631,616	25-Feb-15				
2201	Methods of Forming Sidewall Gates	US	14/099,084	6-Dec-13	2015-0162338	11-Jun-15	9,177,964	3-Nov-15
2202	Methods of Forming Sidewall Gates	WO	US14/068647	4-Dec-14	WO15/085106	11-Jun-15		
2203	Method for Forming Oxide Below Control Gate in Vertical Channel Thin Film Transistor	US	14/193,451	28-Feb-14	2015-0249143	3-Sep-15		
2204	CONCAVE WORD LINE AND CONVEX INTERLAYER DIELECTRIC FOR PROTECTING A READ/WRITE LAYER	US	14/529,624	31-Oct-14				
2205	CONCAVE WORD LINE AND CONVEX INTERLAYER DIELECTRIC FOR PROTECTING A READ/WRITE LAYER	US	14/529,731	31-Oct-14				
2206	Plasma Reduction Method for Modifying Metal Oxide Stoichiometry in RERAM	US	14/196,647	4-Mar-14			9,054,308	9-Jun-15

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2207	Timed Multiplex Sensing	US	14/887,547	20-Oct-15	2016-0042771	11-Feb-16	9,245,599	26-Jan-16
2208	Timed Multiplex Sensing	US	14/191,130	26-Feb-14	2015-0243362	27-Aug-15	9,196,373	24-Nov-15
2209	Regrouping and Skipping Cycles In Non-Volatile Memory	CN	US2014/060907	15-Oct-14				
2210	Regrouping and Skipping Cycles In Non-Volatile Memory	DE	US2014/060907	15-Oct-14				
2211	Regrouping and Skipping Cycles In Non-Volatile Memory	US	61/891,771	16-Oct-13				
2212	Regrouping and Skipping Cycles in Non-Volatile Memory	US	14/515,387	15-Oct-14	2015-0106554	16-Apr-15		
2213	Regrouping and Skipping Cycles In Non-Volatile Memory	WO	US14/060907	15-Oct-14	WO2015/057967	23-Apr-15		
2214	Method of Manufacturing Semiconductor Device and Semiconductor Device Having Unequal Ptich Vertical Channel Transistors	US	14/449,417	1-Aug-14	2016-0035789	4-Feb-16		
2215	Dual Gate Structure	US	14/519,068	21-Oct-14				
2216	Content Addressable Memory Cells, Memory Arrays and Methods of Forming the Same	US	14/512,552	13-Oct-14				
2217	NON-VOLATILE 3D MEMORY WITH CELL-SELECTABLE WORD LINE DECODING	US	14/229,482	28-Mar-14			9,123,392	1-Sep-15
2218	NON-VOLATILE 3D MEMORY WITH CELL-SELECTABLE WORD LINE DECODING	WO	US15/022060	23-Mar-15	WO15/148399	1-Oct-15		
2219	Fully Isolated Selector for Memory Device	US	14/451,664	5-Aug-14	2016-0043143	11-Feb-16		
2220	Fully Isolated Selector for Memory Device	WO	US15/041947	24-Jul-15	WO16/022304	11-Feb-16		
2221	Word Line Connection for Memory Device and Method of Making Thereof	US	14/463,113	19-Aug-14				
2222	Word Line Connection for Memory Device and Method of Making Thereof	WO	US15/043544	4-Aug-15				
2223	DUAL CAPACITOR SENSE AMPLIFIER AND METHODS THEREFOR	US	14/499,717	29-Sep-14			9,224,466	29-Dec-15
2224	MONOLITHIC THREE DIMENSIONAL MEMORY ARRAYS WITH STAGGERED VERTICAL BIT LINES AND DUAL-GATE BIT LINE SELECT TRANSISTORS	US	14/522,777	24-Oct-14				
2225	SINGLE-STAGE FOLDED CASCODE BUFFER AMPLIFIERS WITH ANALOG COMPARATORS	US	14/522,678	24-Oct-14			9,225,304	29-Dec-15
2226	Smart Reprogramming to Eliminate Room Temp Relaxation and Improve high temp Retention	US	61/968,123	20-Mar-14				
2227	SENSING MULTIPLE REFERENCE LEVELS IN NON-VOLATILE STORAGE ELEMENTS	US	14/508,615	7-Oct-14				
2228	SENSING MULTIPLE REFERENCE LEVELS IN NON-VOLATILE STORAGE ELEMENTS	WO	US15/051270	21-Sep-15				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2229	SENSE AMPLIFIER INCLUDING A SINGLE-TRANSISTOR AMPLIFIER AND LEVEL SHIFTER AND METHODS THEREFOR	US	14/539,150	12-Nov-14				
2230	Reducing Disturbances in Memory Cells	US	14/324,259	7-Jul-14	2016-0005495	7-Jan-16		
2231	Intrinsic Vertical Bit Line Architecture	US	14/715,562	18-May-15	2016-0019952	21-Jan-16		
2232	Memory Hole Bit Line Structures	US	14/715,566	18-May-15	2016-0020255	21-Jan-16		
2233	Side Wall Bit Line Structures	US	14/716,382	19-May-15	2016-0020389	21-Jan-16		
2234	Operation Modes for Adjustable Resistance Bit Line Structures	US	14/715,575	18-May-15	2016-0019960	21-Jan-16		
2235	Setting Channel Voltages Using a Dummy Word Line	US	14/715,579	18-May-15	2016-0019953	21-Jan-16		
2236	Controlling Adjustable Resistance Bit Lines Connected to Word Line Combs	US	14/715,583	18-May-15	2016-0019961	21-Jan-16		
2237	Reducing Disturb With Adjustable Resistance Bit Line Structures	US	14/715,586	18-May-15	2016-0019957	21-Jan-16		
2238	Auto-Tracking Unselected Word Line Voltage Generator	US	14/716,388	19-May-15	2016-0019963	21-Jan-16		
2239	Intrinsic Vertical Bit Line Architecture	US	62/041,138	24-Aug-14				
2240	Intrinsic Vertical Bit Line Architecture	US	62/000,967	20-May-14				
2241	Intrinsic Vertical Bit Line Architecture	WO	US15/031804	20-May-15	WO2015/179537	26-Nov-15		
2242	Independent SET/RESET Programming Scheme	US	14/547,473	19-Nov-14				
2243	Vertical TFT with Tunnel Barrier	US	14/515,054	15-Oct-14			9,230,985	5-Jan-16
2244	MONOLITHIC THREE DIMENSIONAL MEMORY ARRAYS WITH STAGGERED VERTICAL BIT LINE SELECT TRANSISTORS AND METHODS THERFOR	US	14/542,213	14-Nov-14				
2245	MEMORY ARRAY HAVING DIVIDED APART BIT LINES AND PARTIALLY DIVIDED BIT LINE SELECTOR SWITCHES	US	14/543,690	17-Nov-14				
2246	INTERLEAVED GROUPED WORD LINES FOR THREE DIMENSIONAL NON-VOLATILE STORAGE	US	14/341,519	25-Jul-14	2016-0027477	28-Jan-16		
2247	Independent Sense Amplifier Addressing and Quota Sharing in Non-Volatile Memory	US	14/619,985	11-Feb-15				
2248	HIGH ENDURANCE NON-VOLATILE STORAGE	US	14/538,763	11-Nov-14				
2249	Vertical Bit Line Non-Volatile Memory with Recessed Word Lines	US	14/681,398	8-Apr-15				
2250	Leakage Current Compensation with Reference Bit Line Sensing in Non-Volatile Memory	US	14/663,786	20-Mar-15				
2251	Sense Amplifier with Integrating Capacitor and other methods of operation	CN	201510883691.9	4-Dec-15				

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	TITLE	COUNTRY	APPLICATION #	FILING DATE	PUBLICATION #	PUBLICATION DATE	PATENT #	ISSUE DATE
2252	Sense Amplifier with Integrating Capacitor and other methods of operation	US	14/663,775	20-Mar-15				
2253	VERTICAL TRANSISTOR AND LOCAL INTERCONNECT STRUCTURE	US	14/623,843	17-Feb-15				
2254	VERTICAL TRANSISTOR AND LOCAL INTERCONNECT STRUCTURE	WO	US15/062548	25-Nov-15				
2255	PARALLEL BIT LINE THREE-DIMENSIONAL RESISTIVE RANDOM ACCESS MEMORY	US	14/635,419	2-Mar-15				
2256	PARALLEL BIT LINE THREE-DIMENSIONAL RESISTIVE RANDOM ACCESS MEMORY	WO	US15/062780	25-Nov-15				
2257	MULTIPLE JUNCTION THIN FILM TRANSISTOR	US	14/723,038	27-May-15				
2258	SILICIDED BIT LINE FOR REVERSIBLE-RESISTIVITY MEMORY	US	14/795,211	9-Jul-15				
2259	THREE-DIMENSIONAL RESISTIVE RANDOM ACCESS MEMORY CONTAINING SELF-ALIGNED MEMORY ELEMENTS	US	14/851,296	11-Sep-15				
2260	Scan Chain Circuits in Non-Volatile Memory	US	14/919,154	21-Oct-15				
2261	RERAM MIM STRUCTURE FORMATION	US	14/928,999	30-Oct-15				
2262	MEMORY CELLS INCLUDING VERTICALLY-ORIENTED ADJUSTABLE RESISTANCE STRUCTURES	US	14/869,231	29-Sep-15				
2263	RESISTIVE RANDOM ACCESS MEMORY CONTAINING A STEERING ELEMENT AND A TUNNELING DIELECTRIC ELEMENT	US	14/924,144	27-Oct-15				
2264	MULTI-LEVEL REVERSIBLE RESISTANCE-SWITCHING MEMORY	US	15/049,088	21-Feb-16				
2265	WORD LINE COMPENSATION FOR MEMORY ARRAYS	US	15/015,672	4-Feb-16				
2266	MONOLITHIC THREE DIMENSIONAL MEMORY ARRAYS FORMED USING SACRIFICIAL POLYSILICON PILLARS	US	14/995,224	14-Jan-16				
2267	MEMORY CELLS WITH CONFIGURABLE POWER-UP STATE	US	15/045,580	17-Feb-16				
2268	DATA-PATH CONTROL WITH INTERNAL CLOCK AND ASYNCHRONOUS FIFO	US	62/278,227	13-Jan-16				
2269	Interface for Non-Volatile Memory	US	62/287,813	27-Jan-16				