PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3915717

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
MEGIT ACQUISITION CORP.	07/09/2014

RECEIVING PARTY DATA

Name:	QUALCOMM INCORPORATED
Street Address:	5775 MOREHOUSE DRIVE
City:	SAN DIEGO
State/Country:	CALIFORNIA
Postal Code:	92121

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	15181176

CORRESPONDENCE DATA

Fax Number: (310)201-5219

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 310 277 7200
Email: qualcomm-uspto@seyfarth.com
Correspondent Name: QUALCOMM INCORPORATED/SEYFARTH SHAW LLP
Address Line 1: 2029 CENTURY PARK EAST, SUITE 3500
Address Line 4: LOS ANGELES, CALIFORNIA 90067-3021

ATTORNEY DOCKET NUMBER:	093019C1D1
NAME OF SUBMITTER:	JOSEPH LUTZ
SIGNATURE:	/Joseph Lutz/
DATE SIGNED:	06/13/2016

Total Attachments: 65
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page1.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page2.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page3.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page4.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page5.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page6.tif

source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page7.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page8.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page9.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page10.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page11.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page12.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page13.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page14.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page15.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page16.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page17.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page18.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page19.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page20.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page21.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page22.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page23.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page24.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page25.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page26.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page27.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page28.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page29.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page30.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page31.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page32.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page33.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page34.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page35.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page36.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page37.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page38.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page39.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page40.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page41.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page42.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page43.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page44.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page45.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page46.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page47.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page48.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page49.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page50.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page51.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page52.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page53.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page54.tif

source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page55.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page56.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page57.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page58.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page59.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page60.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page61.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page62.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page63.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page64.tif
source=ASST_Megit Acquisition Corp. to QCI_2014-07-09#page65.tif

PATENT ASSIGNMENT

WHEREAS, Megit Acquisition Corp., a Delaware corporation having a place of business located at 5775 Morehouse Drive, San Diego, CA 92121 (hereinafter "**ASSIGNOR**"), hereby represents and warrants that it is the sole and exclusive owner of all right, title, and interest in, to and under the Patent Items (as defined below).

WHEREAS, QUALCOMM Incorporated, a Delaware corporation, having a place of business located at 5775 Morehouse Drive, San Diego, California, 92121, U.S.A. (hereinafter "**ASSIGNEE**"), has agreed to acquire all right, title and interest in, to and under (i) the registered patents and patent applications identified in the Exhibit attached hereto (hereinafter the "**Exhibit 1**"), and all provisional applications relating thereto; (ii) all patents issuing on any patent applications identified in the Exhibit; (iii) all reissues, reexaminations, extensions, divisionals, renewals, continuations, continuations-in-part and counterparts (whether foreign or domestic) claiming priority to any of the foregoing items in (i) or (ii) above, along with all patents issuing therefrom; and (iv) all inventions and improvements claimed or described in any of the foregoing items (i), (ii) or (iii) (subsections (i), (ii), (iii) and (iv) hereinafter collectively referred to as the "**Patent Items**").

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, there parties hereto agree as follows:

ASSIGNOR does hereby sell, assign, transfer, convey and deliver unto ASSIGNEE, its successors, legal representatives and assigns, all right, title and interest throughout the world in, to and under the Patent Items, including without limitation all foreign patents and any rights of priority based on or relating to the Patent Items.

ASSIGNOR hereby authorizes and requests the Commissioner of Patents of the United States of America, and any Official of any country or countries foreign to the United States of America, whose duty it is to issue patents on applications, to issue all patents for the Patent Items to ASSIGNEE, its successors, legal representatives and assigns, in accordance with the terms of this Patent Assignment.

ASSIGNOR hereby sells, assigns, transfers, conveys and delivers to ASSIGNEE, its successors, legal representatives and assigns, all rights of enforcement, all claims for damages and all remedies arising out of, relating to or resulting from the Patent Items or any violation(s) thereof, whether accrued prior to the date of this Patent Assignment or hereafter, including but not limited to the right to sue for, seek, collect, recover and retain damages and any other relief arising out of or resulting from any past, present or future infringement or violation of any of the Patent Items, and all other rights, including common law rights, that ASSIGNOR may have relating to the Patent Items, including but not limited to any ongoing or prospective royalties to which ASSIGNOR may be entitled, or that ASSIGNOR may collect for any infringements of any of the Patent Items or from any settlement or agreement related to the Patent Items arising before or after the date of this Patent Agreement, such rights to be held and enjoyed by ASSIGNEE, its successors, legal representatives and assigns, as fully and entirely as the same would have been held and enjoyed by ASSIGNOR if this Patent Assignment had not been made.

ASSIGNOR hereby represents and warrants that it has full right, power and authority to sell, assign, transfer, convey and deliver all of the subject matter set forth herein, and hereby covenants and agrees that upon the written request of ASSIGNEE, ASSIGNOR will communicate promptly to ASSIGNEE, its successors, legal representatives and assigns, all facts known to ASSIGNOR respecting the Patent Items, and will testify in any legal proceeding, sign all lawful papers, transfer all file histories,

make diligent effort to find or reach every inventor of the Patent Items necessary or appropriate in connection with preparation of any lawful document or proceeding relating to the Patent Items, make reasonable efforts to obtain all necessary or appropriate signed and executed documents relating to the Patent Items from every inventor named in the Patent Items, make all rightful declarations and/or oaths and generally do everything possible to aid ASSIGNEE, its successors, legal representatives and assigns, to obtain and enforce patent protection for the Patent Items on a worldwide basis in all countries. ASSIGNEE further covenants and agrees that it will wholly refrain from challenging the validity, enforceability or scope of the Patent Items, whether through opposition, reexamination and/or court proceedings.

[Remainder of Page Intentionally Left Blank]

IN WITNESS WHEREOF, I hereunto set my hand this 9th day of July, 2014.

Rhonda Meyer

[ASSIGNOR'S REPRESENTATIVE]

Printed Name: Rhonda S. Meyer

Title: President

State of California)
) ss.
County of San Diego)

On July 9th, 2014, before me, Gayle S. Gestrick, Notary Public
Date *Name of Notary Public*

personally appeared Rhonda S. Meyer
Name of Signer

who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal. Gayle S. Gestrick
Notary Public

GAYLE S. GESTRICK
Comission # 2040287
Notary Public - California
San Diego County
My Comm. Expires Dec 28, 2017

IN WITNESS WHEREOF, acknowledged and accepted on this 9th day of July, 2014.

On Behalf of QUALCOMM Incorporated

Printed Name: Timothy F. Loomis

Title: VP, Chief Patent Counsel

US Granted Patents: Megit Acquisition Corp.

EXHIBIT 1

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Image and light sensor chip packages	Granted	12/703,139	2/9/2010	8,193,555	093046
US	Chip structure with bumps and testing pads	Granted	12/941,069	11/7/2010	7,977,803	092967C1C1
US	Semiconductor package with interconnect layers	Granted	13/159,190	6/13/2011	8,492,870	092984D1C1C1
US	System-in packages	Granted	12/841,981	7/22/2010	8,503,186	093050
US	Chip packages	Granted	12/748,295	3/26/2010	8,159,070	093048
US	System-in packages	Granted	12/779,863	5/13/2010	8,164,171	093049
US	Integrated circuit chip using top post-passivation technology and bottom structure technology	Granted	12/722,483	3/11/2010	8,456,856	093047
US	Integrated circuit chips with fine-line metal and over-passivation metal	Granted	13/735,987	1/7/2013	8,618,580	093129U4D1
US	Chip package	Granted	13/236,507	9/19/2011	8,368,193	093013C1C1
US	Solder interconnect on IC chip	Granted	13/271,004	10/11/2011	8,742,582	093005C1
US	Chip structure and process for forming the same	Granted	13/277,142	10/19/2011	8,368,204	093036B4D2C1
US	Integrated chip package structure using organic substrate and method of manufacturing the same	Granted	13/031,163	2/18/2011	8,471,361	093105C1C1
US	Chip structure	Granted	13/098,379	4/29/2011	8,159,074	092962U1B1C1C1C1

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Integrated circuit and method for fabricating the same	Granted	13/197,630	8/3/2011	8,471,388	092996C1
US	Post passivation interconnection schemes on top of the IC chips	Granted	13/071,203	3/24/2011	8,456,013	092990D1B1C1C1C1
US	Method for making high-performance RF integrated circuits	Granted	13/077,009	3/31/2011	8,384,508	092983D1C1C1
US	Semiconductor chip with a bonding pad having contact and test areas	Granted	13/094,780	4/26/2011	8,304,766	093002C1
US	Circuit component with conductive layer structure	Granted	13/098,340	4/29/2011	8,334,588	092979B1C1C1
US	Semiconductor chip with coil element over passivation layer	Granted	13/159,147	6/13/2011	8,362,588	092960C1C1
US	Stacked chip package with redistribution lines	Granted	13/159,368	6/13/2011	8,426,958	093008C1C1
US	Chip structure and process for forming the same	Granted	13/191,356	7/26/2011	8,546,947	093036B3D2D1C3C1
US	Multiple selectable function integrated circuit module	Granted	13/197,633	8/3/2011	8,471,389	092992B2C1C1
US	Carbon nanotube circuit component structure	Granted	13/180,479	7/11/2011	8,692,374	093001C1
US	High performance sub-system design and assembly	Granted	13/174,317	6/30/2011	8,399,988	092993D1B1D1C1C3C1
US	Semiconductor chip with post-passivation scheme formed over passivation layer	Granted	13/181,255	7/12/2011	8,319,354	092966C1C1

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Chip package having a chip combined with a substrate via a copper pillar	Granted	13/207,350	8/10/2011	8,421,222	093021D1C1C1C1
US	Chip structure	Granted	13/207,346	8/10/2011	8,519,552	092962U2C1
US	Semiconductor chip and method for fabricating the same	Granted	12/534,885	8/4/2009	8,168,527	093024C1
US	Top layers of metal for high performance IC's	Granted	12/691,597	1/21/2010	8,350,386	093036B1C1B1D1C2C2
US	Method for Fabricating Circuit Component	Granted	13/108,743	5/16/2011	8,461,679	092970C1C1
US	Chip package and method for fabricating the same	Granted	13/107,058	5/13/2011	8,436,449	093023C1
US	Structure of gold bumps and gold conductors on one IC die and methods of manufacturing the structures	Granted	11/178,541	7/11/2005	7,465,654	092962U1
US	Post passivation structure for a semiconductor device and packaging process for same	Granted	11/430,513	5/8/2006	7,468,545	092961
US	Semiconductor chip with coil element over passivation layer	Granted	11/434,861	5/17/2006	7,470,927	092960
US	Integrated chip package structure using organic substrate and method of manufacturing the same	Granted	10/055,499	1/22/2002	7,413,929	093105
US	Stacked chip package with redistribution lines	Granted	11/416,134	5/3/2006	7,508,059	093008
US	Chip package	Granted	11/422,337	6/6/2006	7,495,304	093013

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No	Qualcomm Docket No
US	Semiconductor chip with passivation layer comprising metal interconnect and contact pads	Granted	11/262,182	10/28/2005	7,547,969	093010
US	Chip structure with redistribution traces	Granted	11/181,244	7/14/2005	7,319,277	093033
US	Chip package with capacitor	Granted	09/573,955	5/19/2000	7,247,932	092969
US	High performance system-on-chip using post passivation process and glass substrates	Granted	09/631,041	8/1/2000	6,399,997	093039
US	Thermally compliant PCB substrate for the application of chip scale packages	Granted	09/684,519	10/10/2000	6,809,935	093040
US	Post passivation interconnection schemes on top of the IC chips	Granted	09/691,497	10/18/2000	6,495,442	092990
US	Method and an apparatus to electroless plate a metal layer while eliminating the photoelectric effect	Granted	09/707,295	11/7/2000	6,387,801	092991
US	Reliable metal bumps on top of I/O pads with test probe marks	Granted	09/760,909	1/16/2001	6,426,556	093041
US	Reliable metal bumps on top of I/O pads after removal of test probe marks	Granted	09/783,384	2/15/2001	6,815,324	092978
US	Low fabrication cost, fine pitch and high reliability solder bump	Granted	09/798,654	3/5/2001	6,818,545	092977
US	Wide bit memory using post passivation interconnection scheme	Granted	09/801,327	3/7/2001	6,399,975	093042
US	Structure and manufacturing method of chip scale package	Granted	09/821,546	3/30/2001	7,498,196	092957

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Methods of IC rerouting option for multiple package system applications	Granted	09/858,528	5/17/2001	6,593,649	092988
US	Electrode for electroplating planar structures	Granted	09/932,729	8/20/2001	6,638,840	092986
US	Method for making high-performance RF integrated circuits	Granted	09/945,436	9/4/2001	6,759,275	092983
US	Method making a low fabrication cost, high performance, high reliability chip scale package	Granted	09/953,525	9/17/2001	6,642,136	092985
US	Structure of high performance combo chip and processing method	Granted	09/953,544	9/17/2001	6,613,606	092987
US	Structure of ceramic package with integrated passive devices	Granted	09/953,610	9/17/2001	6,495,912	093043
US	Wafer scale packaging scheme	Granted	09/131,429	8/10/1998	6,103,552	092994
US	Intergrated circuit has common function knows good intergrated circuit die with multiple selectable functions	Granted	09/246,303	2/8/1999	6,356,958	092992
US	Strain release contact system for integrated circuits	Granted	09/249,252	2/12/1999	6,159,773	093014
US	High performance sub-system design and assembly	Granted	09/258,911	3/1/1999	6,180,426	092993
US	Software programmable multiple function integrated circuit module	Granted	09/422,174	10/22/1999	6,555,398	092989
US	Semiconductor chip and process for forming the same	Granted	11/534,672	9/24/2006	7,473,999	093072

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No	Filing Date	Patent No	Qualcomm Docket No
US	Very thick metal interconnection scheme in IC chips	Granted	11/087,955	3/23/2005	8,552,559	093011
US	Process of bonding circuitry components	Granted	11/124,493	5/5/2005	8,232,192	093012
US	Circuitry component and method for forming the same	Granted	11/426,317	6/26/2006	7,582,556	093006
US	Carbon nanotube circuit component structure	Granted	11/563,215	11/27/2006	7,990,037	093001
US	Semiconductor chip with bond area	Granted	11/567,182	12/5/2006	7,947,978	093002
US	Method for forming a double embossing structure	Granted	11/491,117	7/24/2006	7,960,269	093003
US	Non-cyanide gold electroplating for fine-line gold traces and gold pads	Granted	11/750,332	5/17/2007	8,420,520	092998
US	Wire bonding method for preventing polymer cracking	Granted	11/425,155	6/20/2006	8,344,524	092999
US	Integrated circuit and method for fabricating the same	Granted	11/766,805	6/22/2007	8,022,552	092996
US	Integrated circuit (IC) chip and method for fabricating the same	Granted	11/769,735	6/28/2007	8,592,977	092997
US	Bonding pad on IC substrate and method for making the same	Granted	11/383,762	5/17/2006	8,148,822	093004U1
US	Metal pad or metal bump over pad exposed by passivation layer	Granted	11/461,416	7/31/2006	8,399,989	093004U2
US	Metallization structure over passivation layer for IC chip	Granted	11/157,186	6/17/2005	8,067,837	093005

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Semiconductor chip structure	Granted	11/769,736	6/28/2007	8,421,227	092995
US	High performance system-on-chip passive device using post passivation process	Granted	10/445,559	5/27/2003	7,531,417	093034
US	Chip structure with pads having bumps or wirebonded wires formed thereover or used to be tested thereto	Granted	10/730,834	12/8/2003	7,394,161	092967
US	Thin film semiconductor package utilizing a glass substrate with composite polymer/metal interconnect layers	Granted	10/054,001	1/19/2002	6,673,698	092984
US	Thermal compliant semiconductor chip wiring structure for chip scale packaging	Granted	10/279,267	10/24/2002	6,806,570	092979
US	Bonding structure with pillar and cap	Granted	10/874,704	6/22/2004	7,208,834	092970
US	Post passivation interconnection process and structures	Granted	10/937,543	9/9/2004	7,423,346	092963
US	Semiconductor chip with post-passivation scheme formed over passivation layer	Granted	11/262,184	10/28/2005	7,397,121	092966
US	Method of wire bonding over active area of a semiconductor circuit	Granted	10/434,142	5/8/2003	8,021,976	092968U1
US	Chip structure	Granted	11/178,753	7/11/2005	8,022,544	092962U2
US	Chip package with multiple chips connected by bumps	Granted	10/695,630	10/27/2003	7,242,099	093021
US	Fabrication of wire bond pads over underlying active devices, passive devices and/or dielectric layers in integrated circuits	Granted	10/434,524	5/8/2003	7,288,845	092968U2

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Integrated chip package structure using ceramic substrate and method of manufacturing the same	Granted	10/055,498	1/22/2002	6,800,941	092982
US	Semiconductor chip and process for forming the same	Granted	12/273,548	11/19/2008	7,932,172	093072C1
US	Chip structure and process for forming the same	Granted	12/032,706	2/18/2008	7,915,734	093036B3D2D1C7
US	Chip structure and process for forming the same	Granted	12/032,707	2/18/2008	7,906,849	093036B3D2D1C8
US	Chip structure and process for forming the same	Granted	11/930,181	10/31/2007	7,932,603	093036B3D2D1C1
US	Chip structure and process for forming the same	Granted	11/930,182	10/31/2007	7,906,422	093036B3D2D1C2
US	Chip structure and process for forming the same	Granted	12/024,998	2/2/2008	8,008,776	093036B3D2D1C3
US	Chip structure and process for forming the same	Granted	12/024,999	2/2/2008	7,919,867	093036B3D2D1C4
US	Semiconductor chip with passivation layer comprising metal interconnect and contact pads	Granted	12/464,896	5/13/2009	8,242,601	093010C1
US	Top layers of metal for high performance ICs	Granted	12/138,453	6/13/2008	8,022,546	093036B1C1B1D1C2
US	Chip package	Granted	12/353,250	1/13/2009	8,044,475	093013C1
US	High performance sub-system design and assembly	Granted	12/353,251	1/13/2009	7,923,848	092993D1B1D1C1C1

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	High performance sub-system design and assembly	Granted	12/353,252	1/13/2009	7,868,463	092993D1B1D1C1C2
US	Capacitor for high performance system-on-chip using post passivation device	Granted	10/303,451	11/25/2002	6,897,507	093036B2B1B1D3C1
US	High performance system-on-chip using post passivation process	Granted	11/877,647	10/23/2007	7,422,941	093036B2B1B1D3C1D1C5
US	High performance sub-system design and assembly	Granted	12/098,467	4/7/2008	7,535,102	092993D1B1D1C1
US	Stacked chip package with redistribution lines	Granted	12/269,045	11/12/2008	7,973,401	093008C1
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/273,085	11/14/2005	7,276,422	092990D1C1C2
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/273,105	11/14/2005	7,265,047	092990D1C1C3
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/273,447	11/14/2005	7,351,650	092990D1C1C4
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,072	9/17/2007	7,382,052	092990D1C1C1C7
US	Post passivation interconnection schemes on top of IC chips	Granted	11/927,719	10/30/2007	7,446,031	092990D1C1C1C26
US	Post passivation interconnection schemes on top of IC chips	Granted	11/927,721	10/30/2007	7,534,718	092990D1C1C1C27
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,083	9/17/2007	7,524,759	092990D1C1C1C17

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,077	9/17/2007	7,459,791	092990D1C1C1C12
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,078	9/17/2007	7,466,007	092990D1C1C1C13
US	Post passivation interconnection schemes on top of IC chips	Granted	11/856,081	9/17/2007	7,446,035	092990D1C1C1C15
US	Post passivation interconnection schemes on top of IC chip	Granted	11/854,555	9/13/2007	7,462,938	092990D1C1C1C2
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/858,904	9/21/2007	7,419,900	092990D1C1C1C20
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/858,905	9/21/2007	7,443,034	092990D1C1C1C21
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/861,295	9/26/2007	7,439,627	092990D1C1C1C22
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/861,299	9/26/2007	7,479,450	092990D1C1C1C23
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/906,833	10/4/2007	7,449,752	092990D1C1C1C24
US	Top layers of metal for high performance ICs	Granted	11/845,775	8/27/2007	7,396,756	093036B1D1D1C1C7C49
US	Top layers of metal for high performance ICs	Granted	11/840,242	8/17/2007	7,425,764	093036B1D1D1C1C7C29
US	Top layers of metal for high performance ICs	Granted	11/845,766	8/27/2007	7,382,058	093036B1D1D1C1C7C46

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Top layers of metal for high performance ICs	Granted	11/829,108	7/27/2007	7,358,610	093036B1D1D1C1C7C4
US	Top layers of metal for high performance ICs	Granted	11/845,115	8/27/2007	7,385,292	093036B1D1D1C1C7C40
US	Top layers of metal for high performance ICs	Granted	11/845,116	8/27/2007	7,388,292	093036B1D1D1C1C7C41
US	Top layers of metal for high performance ICs	Granted	11/842,160	8/21/2007	7,482,693	093036B1D1D1C1C7C34
US	Top layers of metal for high performance ICs	Granted	11/839,558	8/16/2007	7,442,969	093036B1D1D1C1C7C14
US	Top layers of metal for high performance ICs	Granted	11/839,559	8/16/2007	7,397,135	093036B1D1D1C1C7C15
US	Top layers of metal for high performance ICs	Granted	11/840,239	8/17/2007	7,465,975	093036B1D1D1C1C7C27
US	Top layers of metal for high performance ICs	Granted	11/930,682	10/31/2007	7,427,560	093036B1C1B1D1C1
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,075	9/17/2007	7,439,626	092990D1C1C1C10
US	Post passivation interconnection schemes on top of the IC chips	Granted	12/019,644	1/25/2008	7,498,255	092990D1B1C1C2
US	Post passivation interconnection schemes on top of the IC chips	Granted	10/653,628	9/2/2003	7,443,033	092990D1C1
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/273,071	11/14/2005	7,405,150	092990D1C1C1

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Top layers of metal for high performance IC's	Granted	11/121,477	5/4/2005	7,294,870	093036B1D1D1C1
US	Top layers of metal for high performance IC's	Granted	11/130,917	5/17/2005	7,329,954	093036B1D1D1C1C1
US	Top layers of metal for high performance IC's	Granted	11/131,481	5/18/2005	7,372,155	093036B1D1D1C1C2
US	Top layers of metal for high performance IC's	Granted	11/145,468	6/3/2005	7,384,864	093036B1D1D1C1C3
US	Top layers of metal for high performance IC's	Granted	11/149,092	6/9/2005	7,422,976	093036B1D1D1C1C4
US	Top layers of metal for high performance IC's	Granted	11/230,004	9/19/2005	7,294,871	093036B1D1D1C1C5
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/788,221	4/19/2007	7,459,790	092990D1B1C1
US	Chip structure with redistribution traces	Granted	11/861,290	9/26/2007	7,425,767	093033C1
US	Top layers of metal for high performance ICs	Granted	10/058,259	1/29/2002	6,620,728	093036B1C1
US	Top layers of metal for high performance IC's	Granted	11/230,101	9/19/2005	7,372,085	093036B1D1D1C1C6
US	Top layers of metal for high performance IC's	Granted	11/230,102	9/19/2005	7,368,376	093036B1D1D1C1C7
US	Top layers of metal for high performance ICs	Granted	11/829,105	7/27/2007	7,385,291	093036B1D1D1C1C7C1
US	Method for fabricating a circuit	Granted	12/025,002	2/2/2008	7,462,558	092962U1B1C1

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	component					
US	Method of wire bonding over active area of a semiconductor circuit	Granted	11/678,598	2/25/2007	7,521,812	092968U1C2
US	Wirebond pad for semiconductor chip or wafer	Granted	11/756,620	5/31/2007	7,554,208	092958C1
US	Reliable metal bumps on top of I/O pads after removal of test probe marks	Granted	10/962,964	10/12/2004	7,465,653	092978C1
US	Low fabrication cost, high performance, high reliability chip scale package	Granted	11/120,234	5/2/2005	7,355,288	092985D1C1
US	Low fabrication cost, high performance, high reliability chip scale package	Granted	11/136,650	5/24/2005	7,338,890	092985D1C2
US	Low fabrication cost, fine pitch and high reliability solder bump	Granted	11/930,163	10/31/2007	7,468,316	092977D1C3
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/818,028	6/13/2007	7,417,317	092990D1B1B1C1
US	Structure of high performance combo chip and processing method	Granted	11/901,079	9/14/2007	7,517,778	092987D1C3
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/877,658	10/23/2007	7,521,805	092990D1B1B1B1C1
US	Top layers of metal for high performance ICs	Granted	11/829,109	7/27/2007	7,999,384	09303681D1D1C1C7C5
US	Method for fabricating circuitry component	Granted	10/382,699	3/5/2003	8,211,791	093036B4D2
US	Integrated chip package structure using organic substrate and method of	Granted	12/172,275	7/14/2008	7,898,058	093105C1

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	manufacturing the same					
US	Semiconductor chip with post-passivation scheme formed over passivation layer	Granted	12/132,626	6/4/2008	8,004,092	092966C1
US	Method for fabricating chip package with die and substrate	Granted	10/454,972	6/4/2003	8,535,976	092982D1
US	Low fabrication cost, fine pitch and high reliability solder bump	Granted	10/935,451	9/7/2004	8,368,213	092977D1
US	High performance system-on-chip discrete components using post passivation process	Granted	11/062,276	2/18/2005	8,089,155	093036B2B1B1D3C1B2D1
US	High performance system-on-chip discrete components using post passivation process	Granted	11/062,277	2/18/2005	8,129,265	093036B2B1B1D3C1B2D2
US	Circuit component with bump formed over chip	Granted	11/123,328	5/6/2005	7,382,005	093021D1
US	Post passivation interconnection schemes on top of the IC chips	Granted	10/278,106	10/22/2002	6,734,563	092990D1
US	Multiple chips bonded to packaging structure with low noise and multiple selectable functions	Granted	10/371,505	2/21/2003	7,045,901	092969D1
US	Primary chips bonded to a printed circuit board supporting a secondary chip in a chip-on-chip connection	Granted	10/371,506	2/21/2003	6,791,192	092969D2
US	Electronic device and chip package	Granted	10/420,595	4/22/2003	7,205,646	092969D3
US	Multiple chips bonded to packaging	Granted	10/437,333	5/13/2003	7,468,551	092969D4

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	structure with low noise and multiple selectable functions					
US	Multiple chips bonded to packaging structure with low noise and multiple selectable functions	Granted	10/437,355	5/13/2003	6,768,208	092969D5
US	Software programmable multiple function integrated circuit module	Granted	10/385,953	3/11/2003	7,360,005	092989D1
US	Electrode for electroplating planar structures	Granted	10/462,251	6/16/2003	6,768,194	092986D1
US	Structure of high performance combo chip and processing method	Granted	10/614,928	7/8/2003	7,282,804	092987D1
US	Chip package with die and substrate	Granted	10/996,535	11/24/2004	7,397,117	092984D1D1
US	Low fabrication cost, high performance, high reliability chip scale package	Granted	10/638,454	8/11/2003	6,917,119	092985D1
US	Method for making high-performance RF integrated circuits	Granted	10/856,377	5/28/2004	7,319,377	092983D1
US	Electronic component with die and passive device	Granted	10/728,150	12/3/2003	7,345,365	093105D1
US	Method for fabricating circuitry component	Granted	10/794,472	3/5/2004	7,297,614	093105D2
US	Strain release contact system for integrated circuits	Granted	09/727,869	12/4/2000	6,351,035	093014D1
US	Wafer scale packaging scheme	Granted	09/619,017	7/19/2000	6,486,563	092994D1
US	Circuitry component with metal layer over	Granted	10/638,018	8/8/2003	7,511,376	093103D1

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	die and extending to place not over die					
US	Method for fabricating chip package	Granted	10/977,289	10/28/2004	7,271,033	093103D2
US	Top layers of metal for high performance IC's	Granted	09/972,639	10/9/2001	6,657,310	093036B1D1
US	Top layers of metal for high performance ICs	Granted	10/389,543	3/14/2003	6,965,165	093036B1D1D1
US	Integrated chip package structure using silicon substrate and method of manufacturing the same	Granted	10/174,462	6/17/2002	6,746,898	093104D1
US	Method of fabricating cylindrical bonding structure	Granted	10/174,357	6/17/2002	6,784,087	093032D1
US	High performance sub-system design and assembly	Granted	09/729,152	12/4/2000	6,303,996	092993D1
US	An apparatus to electroless plate a metal layer while eliminating the photo electric effect	Granted	10/117,888	4/8/2002	6,522,009	092991D1
US	Post passivation structure for semiconductor chip or wafer	Granted	10/783,195	2/20/2004	7,420,276	093036B1C1B1D1
US	High performance sub-system design and assembly	Granted	10/420,596	4/22/2003	7,378,735	092993D1B1D1
US	High performance system-on-chip using post passivation process	Granted	11/092,379	3/29/2005	7,459,761	093036B2B1B1D3C1D1
US	Inductor structure for high performance system-on-chip using post passivation process	Granted	09/970,005	10/3/2001	6,455,885	093036B2B1B1

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	High performance system-on-chip using post passivation process	Granted	10/156,412	5/28/2002	6,515,369	093036B2B1B1D1
US	A resistor for high performance system-on-chip using post passivation process	Granted	10/156,589	5/28/2002	6,489,656	093036B2B1B1D2
US	A capacitor for high performance system-on-chip using post passivation process structure	Granted	10/156,590	5/28/2002	6,489,647	093036B2B1B1D3
US	Chip structure and process for forming the same	Granted	10/997,145	11/24/2004	7,470,988	093036B3D2D1
US	Chip structure and process for forming the same	Granted	10/337,668	1/6/2003	6,798,073	093036B4D1
US	Chip structure and process for forming the same	Granted	10/337,673	1/6/2003	6,700,162	093036B3D1
US	Process of fabricating a chip structure	Granted	10/690,250	10/20/2003	6,936,531	093036B3D2
US	Method of fabricating chip package	Granted	12/206,754	9/9/2008	8,748,227	092957C3
US	Semiconductor chip with coil element over passivation layer	Granted	12/276,419	11/24/2008	7,985,653	092960C1
US	Post passivation interconnection process and structures	Granted	12/014,812	1/16/2008	8,018,060	092963B1C1
US	Post passivation interconnection process and structures	Granted	12/182,148	7/30/2008	8,120,181	092963C1
US	Chip structure	Granted	12/202,342	9/1/2008	7,964,973	092962U1B1C1C1
US	Structure of gold bumps and gold conductors on one IC die and methods of	Granted	12/262,195	10/31/2008	8,581,404	092962U1C1

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	manufacturing the structures					
US	Chip package with die and substrate	Granted	10/996,537	11/24/2004	7,977,763	092984D1C1
US	Method of metal sputtering for integrated circuit metal routing	Granted	11/364,375	2/28/2006	8,723,322	092980C2
US	Multiple chips bonded to packaging structure with low noise and multiple selectable functions	Granted	12/269,053	11/12/2008	8,148,806	092969C1
US	Structure and manufacturing method of a chip scale package	Granted	11/981,125	10/31/2007	8,158,508	092977B1C2
US	A structure and manufacturing method of a chip scale package with low fabrication cost, fine pitch and high reliability solder bump	Granted	11/981,138	10/31/2007	7,902,679	092977B1C3
US	Method for fabricating circuit component	Granted	11/685,216	3/13/2007	7,960,270	092970C1
US	Post passivation structure for a semiconductor device and packaging process for same	Granted	12/264,271	11/4/2008	8,558,383	092961C1
US	Low fabrication cost, fine pitch and high reliability solder bump	Granted	12/493,258	6/29/2009	8,072,070	092977D1C4C1
US	Method of wire bonding over active area of a semiconductor circuit	Granted	11/678,600	2/25/2007	8,742,580	092968U1C4
US	Method of wire bonding over active area of a semiconductor circuit	Granted	11/707,827	2/16/2007	8,026,588	092968U1C5
US	Method of wire bonding over active area of a semiconductor circuit	Granted	11/926,154	10/29/2007	8,138,079	092968U1C6

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Post passivation interconnection schemes on top of IC chip	Granted	11/854,561	9/13/2007	7,919,865	092990D1C1C1C5
US	Post passivation interconnection schemes on top of IC chip	Granted	11/854,562	9/13/2007	8,461,686	092990D1C1C1C6
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,073	9/17/2007	8,482,127	092990D1C1C1C8
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,074	9/17/2007	8,492,900	092990D1C1C1C9
US	Wirebond pad for semiconductor chip or wafer	Granted	11/756,621	5/31/2007	8,187,965	092958C2
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,076	9/17/2007	8,188,603	092990D1C1C1C11
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,082	9/17/2007	7,892,965	092990D1C1C1C16
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/906,840	10/4/2007	7,902,067	092990D1C1C1C25
US	Top layers of metal for high performance ICs	Granted	11/842,153	8/21/2007	8,471,384	093036B1D1D1C1C7C31
US	Top layers of metal for high performance ICs	Granted	11/845,123	8/27/2007	8,415,800	093036B1D1D1C1C7C43
US	Top layers of metal for high performance ICs	Granted	12/036,308	2/25/2008	8,022,545	0930368D1D1C1C7C56
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,087	9/17/2007	7,923,366	092990D1C1C1C18

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	High performance system-on-chip using post passivation process	Granted	12/186,530	8/6/2008	8,384,189	093036B2B1B1D3C1D1C5C1
US	Top layers of metal for high performance ICs	Granted	11/930,191	10/31/2007	7,456,100	093036B1D1D1C1C7C54
US	Top layers of metal for high performance ICs	Granted	12/203,154	9/3/2008	7,863,654	093036C14B1
US	Over-passivation process of forming polymer layer over IC chip	Granted	12/273,546	11/19/2008	7,919,412	093035C1
US	High performance sub-system design and assembly	Granted	12/353,255	1/13/2009	7,868,454	092993D1B1D1C1C4
US	Top layers of metal for high performance ICs	Granted	12/138,455	6/13/2008	8,035,227	093036B1C1B1D1C3
US	Multiple selectable function integrated circuit module	Granted	12/098,465	4/7/2008	8,013,448	092992B2C1
US	Chip structure and process for forming the same	Granted	12/025,000	2/2/2008	7,482,259	093036B3D2D1C5
US	Chip structure and process for forming the same	Granted	11/123,936	5/6/2005	7,309,920	093036B3D2C1
US	Top layers of metal for integrated circuits	Granted	11/877,657	10/23/2007	7,482,268	093077B1C1
US	Top layers of metal for high performance ICs	Granted	11/829,110	7/27/2007	8,531,038	093036B1D1D1C1C7C6
US	Top layers of metal for high performance ICs	Granted	11/839,554	8/16/2007	7,884,479	093036B1D1D1C1C7C11
US	High performance system-on-chip using	Granted	11/877,649	10/23/2007	8,487,400	093036B2B1B1D3C1D1C6

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	post passivation process					
US	Chip structure and process for forming the same	Granted	12/025,001	2/2/2008	7,915,157	093036B3D2D1C6
US	Top layers of metal for integrated circuits	Granted	12/001,676	12/12/2007	8,304,907	093077B1C2
US	High performance sub-system design and assembly	Granted	12/353,254	1/13/2009	7,999,381	092993D1B1D1C1C3
US	Post passivation interconnection schemes on top of the IC chips	Granted	12/019,635	1/25/2008	7,928,576	092990D1B1C1C1
US	Post passivation interconnection schemes on top of IC chip	Granted	11/854,552	9/13/2007	8,004,088	092990D1C1C1C1
US	Post passivation interconnection schemes on top of IC chip	Granted	11/856,080	9/17/2007	7,915,161	092990D1C1C1C14
US	Post passivation interconnection schemes on top of IC chips	Granted	11/856,088	9/17/2007	8,435,883	092990D1C1C1C19
US	Low fabrication cost, fine pitch and high reliability solder bump	Granted	11/930,998	10/31/2007	7,863,739	092977D1C4
US	Chip structure with bumps and testing pads	Granted	12/127,794	5/27/2008	7,855,461	092967C1
US	Method for making high-performance RF integrated circuits	Granted	11/930,664	10/31/2007	7,973,629	092983D1C1
US	Structure of high performance combo chip and processing method	Granted	11/842,957	8/22/2007	7,960,212	092987D1C1
US	Low fabrication cost, high performance, high reliability chip scale package	Granted	11/930,220	10/31/2007	8,481,418	092985D1C2C3

US Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Method of joining chips utilizing copper pillar	Granted	12/128,644	5/29/2008	8,021,921	093021D1C1C1
US	Structure of high performance combo chip and processing method	Granted	12/269,064	11/12/2008	7,919,873	092987D1C3C1
US	Structure of high performance combo chip and processing method	Granted	12/269,065	11/12/2008	7,960,842	092987D1C3C2
US	Structure of high performance combo chip and processing method	Granted	11/842,958	8/22/2007	8,124,446	092987D1C2
US	Post passivation interconnection schemes on top of the IC chips	Granted	12/370,617	2/13/2009	7,880,304	092990D1B1B1B1C1C1
US	Post passivation interconnection schemes on top of the IC chips	Granted	12/142,825	6/20/2008	8,013,449	092990D1B1B1C1C1
US	Top layers of metal for integrated circuits	Granted	10/948,020	9/23/2004	7,416,971	093077
US	Chip structure with a passive device and method for forming the same	Granted	10/710,596	7/23/2004	8,421,158	093022
US	Chip structure and process for forming the same	Granted	10/124,388	4/15/2002	6,756,295	093036B3
US	Chip structure and process for forming the same	Granted	10/125,226	4/16/2002	6,762,115	093036B4
US	Top layers of metal for integrated circuits	Granted	11/017,168	12/20/2004	7,381,642	093077B1
US	Method for forming high performance system-on-chip using post passivation process	Granted	09/721,722	11/27/2000	6,303,423	093036B2B1
US	High performance system-on-chip discrete components using post passivation	Granted	10/445,560	5/27/2003	6,869,870	093036B2B1B1D3C1B2

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	process					
US	Multiple selectable function integrated circuit module	Granted	09/961,767	9/21/2001	6,939,747	09299281
US	Multiple selectable function integrated circuit module	Granted	11/181,175	7/14/2005	7,372,162	09299282
US	Connection between a semiconductor chip and a circuit compenent with a large contact area	Granted	11/183,648	7/18/2005	8,198,729	093009
US	High performance sub-system design and assembly	Granted	09/849,039	5/4/2001	6,586,266	092993D1B1
US	Post passivation method for semiconductor chip or wafer	Granted	10/154,662	5/24/2002	7,405,149	093036B1C1B1
US	Top layers of metal for high performance ICs	Granted	09/251,183	2/17/1999	6,383,916	093036B1
US	Wafer scale packaging scheme	Granted	09/617,012	7/14/2000	6,350,705	09299481
US	Post passivation interconnection process and structures	Granted	10/970,871	10/22/2004	7,355,282	092963B1
US	Method for fabricating chip structure	Granted	11/202,730	8/12/2005	7,452,803	092982U1B1
US	Method for fabricating thermal compliant semiconductor chip wiring structure for chip scale packaging	Granted	10/925,302	8/24/2004	7,265,045	092979B1
US	Post passivation metal scheme for high-performance integrated circuit devices	Granted	09/998,862	10/24/2001	6,649,509	092990B1
US	Post passivation metal scheme for high-	Granted	10/004,027	10/24/2001	6,605,528	092990B2

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	performance integrated circuit devices					
US	Post passivation interconnection schemes on top of the IC chips	Granted	10/685,872	10/15/2003	7,230,340	092990D1B1
US	Post passivation interconnection schemes on top of the IC chips	Granted	10/962,963	10/12/2004	7,271,489	092990D1B1B1
US	Post passivation interconnection schemes on top of the IC chips	Granted	11/017,145	12/20/2004	7,372,161	092990D1B1B1B1
US	High performance system-on-chip inductor using post passivation process	Granted	10/445,558	5/27/2003	8,178,435	093036B2B1B1D3C1B1
US	Post passivation interconnection structures	Granted	11/017,169	12/20/2004	8,008,775	092963B1B1
US	Integrated chip package structure using metal substrate and method of manufacturing the same	Granted	10/055,560	1/22/2002	8,119,446	093103
US	Semiconductor chip with redistribution metal layer	Granted	11/183,300	7/15/2005	RE40,887	092988R1
US	Post passivation metal scheme for high-performance integrated circuit devices	Granted	11/518,595	10/24/2001	RE43,674	092990B2R1C3
US	Wirebond over post passivation thick metal	Granted	12/198,899	8/27/2008	8,030,775	093037
US	Wirebond pad for semiconductor chip or wafer	Granted	10/796,427	3/9/2004	7,470,997	092958
US	Integrated circuit chips with fine-line metal and over-passivation metal	Granted	11/864,917	9/29/2007	7,969,006	093129U1

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
US	Semiconductor chip and method for fabricating the same	Granted	11/850,677	9/6/2007	7,582,966	093024
US	Method for forming post passivation AU layer with clean surface	Granted	11/949,785	12/4/2007	8,440,272	093025
US	Voltage regulator integrated with semiconductor chip	Granted	11/964,015	12/25/2007	8,749,021	093026
US	Structure and manufacturing method of chip scale package	Granted	12/512,073	7/30/2009	8,426,982	092967C1C1
US	Method for fabricating thermal compliant semiconductor chip wiring structure for chip scale packaging	Granted	11/761,360	6/11/2007	7,960,272	092979B1C1
US	Software programmable multiple function integrated circuit module	Granted	12/034,668	2/21/2008	8,107,311	092989D1C1
US	Low fabrication cost, high performance, high reliability chip scale package	Granted	11/930,210	10/31/2007	8,178,967	092985D1C2C1
US	Chip package	Granted	12/101,127	4/10/2008	7,964,961	093029
US	Water level processing method and structure to manufacture two kinds of bumps, gold and solder, on one wafer	Granted	10/855,086	5/27/2004	8,674,507	093016
US	High performance IC chip having discrete decoupling capacitors attached to its IC surface	Granted	10/802,566	3/17/2004	8,368,150	093017
US	Chip package with dam bar restricting flow of underfill	Granted	11/307,127	1/24/2006	8,294,279	093018
US	Chip package and method for fabricating	Granted	11/836,816	8/10/2007	7,569,422	093019

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	the same					
US	Chip assembly with interconnection by metal bump	Granted	12/045,029	3/10/2008	8,193,636	093028
US	Chip package and method for fabricating the same	Granted	11/850,674	9/5/2007	7,960,825	093023
US	Integrated circuit chips with fine-line metal and over-passivation metal	Granted	11/864,927	9/29/2007	8,004,083	093129U3
US	Integrated circuit chips with fine-line metal and over-passivation metal	Granted	11/864,931	9/29/2007	8,373,202	093129U4
US	Integrated circuit chips with fine-line metal and over-passivation metal	Granted	11/864,935	9/29/2007	8,021,918	093129U5
US	Integrated circuit chips with fine-line metal and over-passivation metal	Granted	11/864,938	9/29/2007	7,989,954	093129U6
US	Over-passivation process of forming polymer layer over IC chip	Granted	11/183,658	7/18/2005	7,592,205	093035

US Pending Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	System-in packages	Allowed	13/935,135	7/3/2013	093050C1
US	Chip packages with power management integrated circuits and related techniques	Allowed	14/034,440	9/23/2013	093045D1
US	Integrated chip package structure using ceramic substrate and method of manufacturing the same	Allowed	13/887,093	5/3/2013	092982D1D1
US	Image and light sensor chip packages	Allowed	13/475,820	5/18/2012	093046D1
US	Circuitry component and method for forming the same	Application	12/545,880	8/24/2009	093006C1
US	Double embossing structure	Application	13/108,811	5/16/2011	093003C1
US	Structure and manufacturing method of chip scale package	Application	13/853,878	3/29/2013	092957C1C1C1
US	Integrated circuit chip using top post-passivation technology and bottom structure technology	Application	13/874,983	5/1/2013	093047C1
US	Low fabrication cost, high performance, high reliability chip scale package	Application	11/930,213	10/31/2007	092985D1C2C2
US	Chip package and method for fabricating the same	Application	12/506,278	7/21/2009	093019C1
US	Chip package with die and substrate	Application	10/055,568	1/22/2002	093104
US	Cylindrical bonding structure and method of manufacture	Application	12/132,628	6/4/2008	093032C1

US Pending Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	Chip package and method for fabricating the same	Allowed	11/681,219	3/2/2007	093000
US	Low fabrication cost, high performance, high reliability chip scale package	Application	11/930,224	10/31/2007	092985D1C2C4
US	Method of wire bonding over active area of a semiconductor circuit	Application	11/678,599	2/25/2007	092968U1C3
US	Method of wire bonding over active area of a semiconductor circuit	Application	11/926,156	10/29/2007	092968U1C7
US	Reliable metal bumps on top of I/O pads after removal of test probe marks	Application	12/182,145	7/30/2008	092978C1C1
US	Chip package	Application	12/206,751	9/9/2008	092957C2
US	Method of wire bonding over active area of a semiconductor circuit	Application	11/678,597	2/25/2007	092968U1C1
US	Integrated chip package structure using silicon substrate and method of manufacturing the same	Application	10/755,042	1/9/2004	093104D2

Foreign Pending Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
BR	System-in packages	Application	BR1120120021389	7/22/2010	093050BR
CN	Integrated Circuit Chip Using Top Post-Passivation Technology and Bottom Structure Technology	Application	201080015041.8	3/11/2010	093047CN
CN	System-in packages	Application	201080021321.X	5/13/2010	093049CN
CN	System-in packages	Application	201080032884.9	7/22/2010	093050CN
CN	Chip packages with power management integrated circuits and related techniques	Application	200980152887.3	12/22/2009	093045CN
EP	High performance system-on-chip using post passivation process	Application	01480078.3	8/27/2001	093036B2B1EP
EP	Post passivation interconnection schemes on top of the IC chips	Application	01480077.5	8/27/2001	092990EP
EP	Post passivation interconnection schemes on top of the IC chips	Application	11002133.4	8/27/2001	092990EPD1
EP	High performance system-on-chip using post passivation process	Application	10012711.7	8/27/2001	093036B2B1EPD1
EP	High performance system-on-chip using post passivation process	Application	10012699.4	8/27/2001	093036B2B1EPD2
EP	High performance system-on-chip using post passivation process	Application	10012703.4	8/27/2001	093036B2B1EPD3
EP	High performance sub-system design and assembly	Application	11005755.1	5/2/2002	092993EPD1
EP	System-in packages	Application	10740066.5	7/22/2010	093050EP

Foreign Pending Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
EP	System-in packages	Application	10719212.2	5/13/2010	093049EP
EP	Integrated Circuit Chip Using Top Post-Passivation Technology and Bottom Structure Technology	Application	10759186.9	3/11/2010	093047EP
EP	Chip Packages with Power Management Integrated Circuits and Related Techniques	Application	09835798.1	12/22/2009	093045EP
EP	Image or Light Sensor Chip Packages	Application	10741665.3	2/10/2010	093046EP
IN	Integrated Circuit Chip Using Top Post-Passivation Technology and Bottom Structure Technology	Application	6721/DELNP/2011	3/11/2010	093047IN
IN	System-in packages	Application	8700/DELNP/2011	5/13/2010	093049IN
IN	System-in packages	Application	452/DELNP/2012	7/22/2010	093050IN
IN	Chip Packages with Power Management Integrated Circuits and Related Techniques	Application	1461/MUMNP/2011	12/22/2009	093045IN
IN	Image and light sensor chip packages	Application	5732/DELNP/2011	2/10/2010	093046IN
JP	High performance system on-chip using post passivation method	Application	2001-267522	9/4/2001	093067JP
JP	Manufacturing method of line device	Application	2006-173775	6/23/2006	093006JP2
JP	Manufacturing method of line device	Application	2014-007143	1/17/2014	093006JP2D1

Foreign Pending Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
JP	Interconnecting structure body and forming method therefor	Application	2012-084641	4/3/2012	093066JPD1
JP	Manufacturing method of line device	Application	2013-141588	7/5/2013	093006JP1D1
JP	High performance system on-chip using post passivation method	Application	2013-214264	10/11/2013	093067JPD1
JP	Image or Light Sensor Chip Packages	Application	2014-081371	4/10/2014	093046JPD1
JP	Integrated circuit chip using top post-passivation technology and bottom structure technology	Application	2012-503470	3/11/2010	093047JP
JP	System-in packages	Application	2012-511030	5/13/2010	093049JP
JP	System-in packages	Application	2012-522911	7/22/2010	093050JP
JP	Interconnecting structure body and forming method therefor	Application	2012-223435	3/1/2001	093066JPD2
JP	High performance sub-system design and assembly	Application	2010-097554	4/21/2010	093069JPD1
TW	Chip package and method for fabricating the same	Application	102106461	2/23/2013	093023TWD1
TW	System-in package	Application	099143384	12/10/2010	093049TWD1
TW	Integrated circuit chip using post-passivation technology and bottom structure technology	Application	099107175	3/11/2010	093047TW
TW	System-in packages	Application	099115370	5/13/2010	093049TW
TW	System-in packages	Application	099124197	7/22/2010	093050TW

Foreign Pending Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
TW	Integrated circuit (IC) chip and method for fabricating the same	Application	096123393	6/28/2007	092997TW

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
CN	A circuit component	Granted	201110042223.0	7/24/2006	ZL201110042223.0	093003CN2D1
CN	Image or light sensor chip packages	Granted	201080014913.9	2/10/2010	ZL201080014913.9	093046CN
CN	Circuit component and method for fabricating the same	Granted	201010508077.1	6/23/2006	ZL201010508077.1	093006CN3D1
CN	Semiconductor device	Granted	201010265643.0	7/31/2006	ZL201010265643.0	093004CN1D1
CN	A semiconductor device	Granted	201010265667.6	7/31/2006	ZL201010265667.6	093004CN2D1
CN	Chip structure with capacitor element and method for forming capacitor on chip	Granted	200410045976.7	5/27/2004	ZL200410045976.7	093053CN
CN	Circuit component and method for fabricating the same	Granted	200610080847.0	5/18/2006	100454484	092960CN2
CN	Circuit component	Granted	200610080848.5	5/18/2006	100438029	092960CN3
CN	Circuit component	Granted	200610080849.X	5/18/2006	100438030	092960CN4
CN	Circuit component and method for fabricating the same	Granted	200610099174.3	7/31/2006	ZL200610099174.3	093004CN1
CN	Circuit assembly structure and method for making the same	Granted	200610099175.8	7/31/2006	ZL200610099175.8	093004CN2
CN	Circuit assembly structure and method for making the same	Granted	200610099176.2	7/31/2006	ZL200610099176.2	093004CN3
CN	Circuit component and method for fabricating the same	Granted	200610090120.0	6/23/2006	ZL200610090120.0	093006CN1

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
CN	Circuitry component and method for forming the same	Granted	200610090121.5	6/23/2006	ZL200610090121.5	093006CN2
CN	Circuit component and method for fabricating the same	Granted	200610090122.X	6/23/2006	ZL 200610090122.X	093006CN3
CN	Method for fabricating a circuitry component by continuous electroplating and circuitry component structure	Granted	200610099490.0	7/24/2006	ZL 200610099490.0	093003CN1
CN	Method for forming a double embossing structure	Granted	200610099491.5	7/24/2006	ZL200610099491.5	093003CN2
CN	Method for forming a double embossing structure	Granted	200610099492.X	7/24/2006	ZL200610099492.X	093003CN3
CN	Circuit component	Granted	200710003675.1	1/23/2007	ZL200710003675.1	093058CN
CN	Circuit component	Granted	200710003676.6	1/23/2007	ZL200710003676.6	093057CN
CN	Circuit component	Granted	200710003677.0	1/23/2007	ZL200710003677.0	093056CN
CN	Circuit component	Granted	200710003678.5	1/23/2007	ZL200710003678.5	093054CN
CN	Circuit component	Granted	200710003679.X	1/23/2007	ZL200710003679.X	093055CN
CN	Circuit component	Granted	200710003680.2	1/23/2007	ZL200710003680.2	093059CN
CN	Circuit component	Granted	200710107580.4	5/21/2007	ZL200710107580.4	093062CN
CN	Circuit component	Granted	200710107581.9	5/21/2007	ZL200710107581.9	093064CN
CN	Circuit component and method for	Granted	200610080846.6	5/18/2006	100521087	092960CN1

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
	fabricating the same					
CN	Circuitry component fabricating method	Granted	200910145302.7	5/18/2006	ZL200910145302.7	092960CN1D1
EP	Circuitry component and method for forming the same	Granted	11003815.5	6/23/2006	EP2421036	093006EP2D1
EP	Circuitry component and method for forming the same	Granted	06012984.8	6/23/2006	EP1737037	093006EP1
EP	Circuitry component	Granted	06013044.0	6/23/2006	EP1737038	093006EP2
FR	Circuitry component and method for forming the same	Granted	11003815.5	6/23/2006	EP2421036	093006FR2D1
DE	Circuitry component	Granted	602006032585.1	6/23/2006	EP1737038	093006DE2
DE	Circuitry component and method for forming the same	Granted	602006030917.1	6/23/2006	EP1737037	093006DE1
DE	Circuitry component and method for forming the same	Granted	602006038314.2	6/23/2006	EP2421036	093006DE2D1
GB	Circuitry component	Granted	06013044.0	6/23/2006	EP1737038	093006GB2
GB	Circuitry component and method for forming the same	Granted	06012984.8	6/23/2006	EP1737037	093006GB1
GB	Circuitry component and method for forming the same	Granted	11003815.5	6/23/2006	EP2421036	093006GB2D1
IT	Circuitry component and method for forming the same	Granted	11003815.5	6/23/2006	EP2421036	093006IT2D1

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
JP	Chip packages with power management integrated circuits and related techniques	Granted	2011-543655	12/22/2009	5335931	093045JP
JP	Intregrated circuit chip	Granted	2002-131172	5/7/2002	5085829	093069JP
JP	Method of forming inductor for high-performance integrated circuit overlaid on surface of semiconductor substrate	Granted	2001-028283	2/5/2001	5005856	093065JP
JP	Interconnecting structure body and forming method therefor	Granted	2001-056759	3/1/2001	5429764	093066JP
JP	Manufacturing method of line device	Granted	2006-173778	6/23/2006	5435524	093006JP3
NL	Circuitry component and method for forming the same	Granted	11003815.5	6/23/2006	EP2421036	093006NL2D1
KR	System-in packages	Granted	10-2012-7005571	7/22/2010	10-1332225	093050KR
KR	System-in packages	Granted	10-2011-7029816	5/13/2010	10-1354083	093049KR
KR	Integrated circuit chip using top post-passivation technology and bottom structure technology	Granted	10-2011-7025488	3/11/2010	10-1307490	093047KR
KR	Image or light sensor chip packages	Granted	10-2011-7021043	2/10/2010	10-1301646	093046KR
KR	Chip packages with power management integrated circuits and related techniques	Granted	10-2011-7017560	12/22/2009	10-1332228	093045KR

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
SG	High performance system-on-chip using post passivation process	Granted	200100488-6	1/30/2001	119136	093036B2B1SG1
SG	High performance system-on-chip using post passivation process	Granted	200104426-2	7/20/2001	98450	093036B2B1SG2
SG	High performance sub-system design and assembly	Granted	200006177-0	10/27/2000	106592	092990SG1
SG	Method of manufacture and identification of semiconductor chip marked for identification with internal marking indicia and protection thereof by non-black layer and device produced thereby	Granted	200100487-8	1/30/2001	106050	092990SG2
SG	Post passivation interconnection schemes on top of the IC chips	Granted	200101847-2	3/23/2001	96209	092990SG3
SG	Post passivation interconnection schemes on top of the IC chips	Granted	200502258-7	3/23/2001	135967	092990SG4
SG	Top layers of metal for high performance ICs	Granted	200006178-8	10/27/2000	93278	093071SG
SG	Method for forming high performance system-on-chip using post passivation process	Granted	200502934-3	7/20/2001	143973	093036B2B1SG3
SG	Integrated circuit chip	Granted	200805202-9	7/20/2001	173923	093036B2B1SG4
SG	Post passivation interconnection schemes on top of the IC chips	Granted	200803837-4	3/23/2001	177778	093036B2SG

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
SG	Post passivation interconnection schemes on top of the IC chips	Granted	200907385-9	3/23/2001	184576	092990SG4D1
ES	Circuitry component and method for forming the same	Granted	11003815.5	6/23/2006	EP2421036	093006ES2D1
TW	Chip structure with a capacitor and method for mounting a capacitor over a chip	Granted	100102330	4/2/2003	I359488	093125TWD1
TW	Circuit structure and fabrication method thereof	Granted	095122893	6/23/2006	I336098	093006TW1
TW	Method for forming circuitry component and structure of the same	Granted	095122894	6/23/2006	I371059	093006TW2
TW	Semiconductor chip, chip package and chip package process	Granted	093131516	10/18/2004	I320956	093005TW2
TW	Connection between two circuitry components	Granted	097117658	10/18/2004	I331370	093005TW3
TW	Method for forming a double embossing structure	Granted	095126894	7/24/2006	I320219	093003TW1
TW	High performance system-on-chip inductor using post passivation process	Granted	093111711	4/27/2004	I236763	093036B2B1B1D3C1B1TW
TW	Electronic component and fabricating the same	Granted	093111830	4/28/2004	I278984	093036B2B1B1D3C1B2TW
TW	Inductor structure for high performance system-on-chip	Granted	090104146	2/23/2001	NI-164075	093036B2TW
TW	Chip structure	Granted	093124492	8/12/2004	I236722	092962TW1

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
TW	Chip structure and method for fabricating the same	Granted	093138329	12/10/2004	I284385	092962TW2
TW	Chip package and process for the same	Granted	093128389	9/20/2004	I301647	093005TW1
TW	High performance sub-system design and assembly	Granted	089100185	1/7/2000	143635	092993TW1
TW	High performance sub-system design and assembly	Granted	089100185A01	8/23/2001	NI-143635	092993TW2
TW	Wafer scale packaging scheme	Granted	088111047	6/30/1999	NI-128975	092994TW
TW	Method for forming a double embossing structure	Granted	095126895	7/24/2006	I305951	093003TW2
TW	Semiconductor chip, chip package and chip package process	Granted	096126071	9/20/2004	I304239	093005TW4
TW	Wafer scale packaging scheme	Granted	090104145	2/23/2001	NI-155078	092994B1TW
TW	Semiconductor module with multiple selectable functions	Granted	089100043	1/4/2000	NI-134825	092992TW
TW	Semiconductor module with multiple selectable functions	Granted	088117852	10/15/1999	NI-135287	093079TW
TW	Chip package structure and method for fabricating the same	Granted	088117853	10/15/1999	NI-127783	093081TW
TW	Thinning process for silicon substrate	Granted	088117935	10/16/1999	NI-130349	093078TW

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
TW	Method of electroless plating	Granted	089107073	4/15/2000	NI-138299	093080TW
TW	Memory chip with wide line	Granted	089124239	11/16/2000	NI-154387	093086TW
TW	Substrate for chip scale package	Granted	089124865	11/23/2000	NI-168619	093082TW
TW	Post passivation interconnection schemes on top of IC Chips	Granted	090100176	1/4/2001	NI-157665	093085TW
TW	Chip with redistribution layer and process for forming the same	Granted	090100339	1/8/2001	NI-207028	093083TW
TW	Multi-chips package	Granted	090101748	1/30/2001	NI-146631	093087TW
TW	Structure of chip with passive device mounted on chip and method for forming the same	Granted	090102895	2/9/2001	NI-156617	093084TW
TW	Flip chip and method for fabricating the same	Granted	090104143	2/23/2001	NI-153730	093091TW
TW	Flip chip and method for fabricating the same	Granted	090104144	2/23/2001	146485	093092TW
TW	Flip chip structure and method for fabricating the same	Granted	090104979	3/5/2001	NI-164564	093093TW
TW	Structure of ceramic package	Granted	090108996	4/16/2001	NI-159044	093088TW
TW	Structure and manufacturing method of chip scale package	Granted	090110093	4/27/2001	NI-153150	093090TW

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
TW	Chip structure and method for fabricating the same	Granted	090131796	12/21/2001	NI-171950	093109TW
TW	Chip package structure and method for fabricating the same	Granted	090133092	12/31/2001	NI-200791	092982TW
TW	Chip package structure and method for fabricating the same	Granted	090133093	12/31/2001	NI-183086	093105TW
TW	Method for transporting semiconductor wafer	Granted	090133094	12/31/2001	NI-167048	093100TW
TW	Chip package and method for fabricating the same	Granted	090133194	12/31/2001	NI-170294	093103TW
TW	Chip package and method for fabricating the same	Granted	090133195	12/31/2001	NI-163882	093104TW
TW	Semiconductor module with multiple selectable functions	Granted	090133196	12/31/2001	NI-168755	093095TW
TW	Metal pillar and method for fabricating the same	Granted	091100092	1/7/2002	I245402	093032TW
TW	Metal bump process	Granted	091103106	2/22/2002	NI-169699	093110TW
TW	Method of forming circuit layer	Granted	091116870	7/29/2002	NI-181685	093111TW
TW	Process of probing a wafer	Granted	091117854	8/8/2002	I220170	093114TW
TW	Process of forming metal bump on semiconductor wafer	Granted	091117855	8/8/2002	NI-187179	093113TW

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
TW	Package for flip chip appled to LCD device	Granted	091118756	8/20/2002	NI-187190	093112TW
TW	Structure of wire bonding over semiconductor chip	Granted	091121967	9/25/2002	I299550	093116TW
TW	Process of conductive structure on semiconductor	Granted	091125109	10/25/2002	NI-185193	093115TW
TW	Method for assembling chips	Granted	091125126	10/25/2002	I313507	093021TW1
TW	Circuit structure	Granted	091133112	11/12/2002	NI-192933	093118TW
TW	Process for forming flip chip	Granted	091133113	11/12/2002	I279895	093119TW
TW	Chip structure with a capacitor and method for mounting a capacitor over a chip	Granted	092107480	4/2/2003	I344689	093125TW
TW	Chip structure with capacitor and method for forming the same	Granted	092112545	5/8/2003	NI-237847	093124TW
TW	Chip structure and method for fabricating the same	Granted	092114226	5/27/2003	I317548	093016TW
TW	Chip structure with passive devices and method for forming the same	Granted	092120050	7/23/2003	I231004	093022TW
TW	Chip structure	Granted	092124295	9/3/2003	I225288	093127TW
TW	Chip bonding method	Granted	093112610	5/5/2004	I230989	093012TW1

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
TW	Chip structure with redistribution circuit, chip package and manufacturing process thereof	Granted	093120946	7/14/2004	I249822	093033TW
TW	Post-passivation process and process of forming a polymer layer on the chip	Granted	093121260	7/16/2004	I283443	093035TW
TW	Post passivation interconnection schemes on top of the ic chips	Granted	093139720	12/17/2004	I298188	093121TW
TW	Chip structure with bumps and testing pads	Granted	094103006	2/1/2005	I250598	093126TW
TW	Stacked chip package and process thereof	Granted	094114203	5/3/2005	I269420	093008TW
TW	Flip chip and method for fabricating the same	Granted	090122319	9/10/2001	169589	093097TW
TW	Flip chip structure and method for fabricating the same	Granted	090122966	9/19/2001	161373	093094TW
TW	Flip chip structure	Granted	090126844	10/30/2001	NI-163772	093096TW
TW	Post passivation interconnection schemes on top of IC Chips	Granted	090130876	12/13/2001	NI-171945	093099TW
TW	Chip structure and method for fabricating the same	Granted	090131029	12/14/2001	NI-167708	093106TW
TW	Chip structure and method for fabricating the same	Granted	090131030	12/14/2001	NI-166544	093107TW
TW	Chip package and method for fabricating the same	Granted	090131210	12/17/2001	178254	093101TW

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
TW	Chip structure and method for fabricating the same	Granted	094133248	9/23/2005	I308785	093072TW
TW	Chip-package structure and manufacturing process thereof	Granted	095134734	9/20/2006	I317175	093131TW
TW	Chip structure and method for fabricating the same	Granted	095135704	9/23/2005	I331788	093128TW
TW	Circuit component and process for forming the same	Granted	095136114	9/29/2006	I344686	093130TW
TW	Circuit component	Granted	095136115	9/29/2006	I370515	093129TW
TW	Structure of wire bonding over semiconductor chip	Granted	095138283	9/25/2002	I300963	093117TW
TW	High performance system-on-chip passive device using post passivation process	Granted	096100433	4/28/2004	I342598	093122TW
TW	Top layers of metal for high performance ICs	Granted	088120584	11/25/1999	NI-140721	093036TW
TW	Chip packaging structure and manufacturing process thereof	Granted	095115973	5/5/2006	I375284	093012TW2
TW	Chip package and method for fabricating the same	Granted	096107211	3/2/2007	I427718	093000TW1
TW	Chip package and method for fabricating the same	Granted	096107214	3/2/2007	I376758	093000TW2
TW	Carbon allotropy of circuit structure and fabrication method thereof	Granted	095143682	11/27/2006	I364058	093001TW

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
TW	Semiconductor chip	Granted	095145100	12/5/2006	I339419	093002TW
TW	Method for fabricating chip package	Granted	096117886	5/18/2007	I351082	092998TW
TW	Chip package and method for fabricating the same	Granted	096107829	3/7/2007	I357139	092999TW
TW	Integrated circuit and method for fabricating the same	Granted	096122418	6/22/2007	I353652	092996TW
TW	Bonding pad on IC substrate and method for making the same	Granted	095127947	7/31/2006	I371069	093004TW1
TW	Bonding pad on IC substrate and method for making the same	Granted	095127948	7/31/2006	I370496	093004TW2
TW	Circuit component structure	Granted	096114823	4/26/2007	I368982	093133TW
TW	Circuit component structure	Granted	096114825	4/26/2007	I347668	093132TW
TW	Semiconductor chip with coil element over passivation layer	Granted	095117392	5/17/2006	I330863	092960TW
TW	Semiconductor chip with post-passivation scheme formed over passivation layer	Granted	095140066	10/30/2006	I328264	092966TW
TW	Multi chips assembling structure and method for assembling chips	Granted	093113040	5/10/2004	I226114	093021TW2
TW	Software programmable multiple function integrated circuit module	Granted	089115929	8/8/2000	NI-163213	092989TW

Foreign Granted Patents: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Patent No.	Qualcomm Docket No.
TW	Method of wire bonding over active area of a semiconductor circuit	Granted	093111710	4/27/2004	I233653	092968U1TW
TW	Chip assembly	Granted	097132724	8/27/2008	I368286	093037TW
TW	Chip structure and process for forming the same	Granted	095118566	5/25/2006	I312169	093007TW1
TW	Semiconductor chip and method for fabricating the same	Granted	096133089	9/5/2007	I342594	093024TW
TW	Method for fabricating and testing semiconductor wafer	Granted	096146006	12/4/2007	I369724	093025TW
TW	Chip package and method for fabricating the same	Granted	096133091	9/5/2007	I395275	093023TW
TW	Circuit structure and fabrication method thereof	Granted	097146146	6/23/2006	I398903	093007TW3
TW	High performance system-on-chip passive device using post passivation process	Granted	093111833	4/28/2004	I312181	093034TW
TW	Chip with redistribution layer and process for forming the same	Granted	NI-207028	1/08/2001	090100339	093083TW

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
CN	On chip transformer	Not Filed			092960CN1D1D1
EP	High performance sub-system design and assembly	Abandoned	02368046.5	5/2/2002	092993EP
EP	Low fabrication cost, fine pitch and high reliability solder bump	Abandoned	02392002.8	3/5/2002	092977EP
JP	Method for forming metal bump on semiconductor surface	Abandoned	2002-056997	3/4/2002	093068JP
JP	High performance sub-system design and assembly	Abandoned	2012-034385	2/20/2012	093069JPD1D1
JP	Image or Light Sensor Chip Packages	Do Not Pursue	2011-550201	2/10/2010	093046JP
JP	Method for forming metal bumps on semiconductor surface	Do Not Pursue	2006-200592	7/24/2006	093070JP
JP	Manufacturing method of line device	Do Not Pursue	2006-173769	6/23/2006	093006JP1
WO	System-in packages	Expired	PCT/US2010/034815	5/13/2010	093049WO
WO	Integrated Circuit Chip Using Top Post-Passivation Technology and Bottom Structure Technology	Expired	PCT/US2010/027056	3/11/2010	093047WO
WO	Chip Packages	Expired	PCT/US2010/029066	3/29/2010	093048WO
WO	Chip Packages with Power Management Integrated Circuits and	Expired	PCT/US2009/069303	12/22/2009	093045WO

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
	Related Techniques				
WO	Image or Light Sensor Chip Packages	Expired	PCT/US2010/023762	2/10/2010	093046WO
WO	System-in packages	Expired	PCT/US2010/042958	7/22/2010	093050WO
SG	Method for forming a double embossing structure	Do Not Pursue	201000390-3	1/19/2010	093003SGD1
SG	Circuit structure and fabrication method thereof	Do Not Pursue	201003764-6	5/31/2010	093006SGD1
SG	Metal pad or metal bump over pad exposed by passivation layer	Do Not Pursue	200605100-7	7/28/2006	093004SG
SG	Method for forming a double embossing structure	Do Not Pursue	200702344-3	3/28/2007	093003SG
SG	Circuit structure and fabrication method thereof	Do Not Pursue	200604348-3	6/23/2006	093006SG
SG	Low fabrication cost, fine pitch and high reliability solder bump	Do Not Pursue	200201291-2	3/5/2002	092977SG
SG	Reliable metal bumps on top of I/O pads with test probe marks	Do Not Pursue	200103355-4	5/31/2001	093041SG
SG	Metal pad or metal bump over pad exposed by passivation layer	Do Not Pursue	201004591-2	7/28/2006	093004SGD1
TW	Strain release contact system for integrated circuits	Abandoned	088123094	12/28/1999	093014TW
TW	Post passivation interconnection process and structures	Abandoned	094130996	9/8/2005	092963TW

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
TW	Chip structure and method for fabricating the same	Abandoned	090131795	12/21/2001	093108TW
TW	Chip package and method for fabricating the same	Abandoned	090129241	11/27/2001	093098TW
TW	Chip-package structure and manufacturing process thereof	Abandoned	094118540	6/6/2005	093013TW
TW	Electrode for electroplating planar structures	Abandoned	090110094	4/27/2001	093089TW
TW	Chip packages with power management integrated circuits and related techniques	Do Not Pursue	099105855	12/25/2009	093045TWD1
TW	Light Sensor Chip	Do Not Pursue	099121904	2/10/2010	093046TWD1
TW	Chip packages with power management integrated circuits and related techniques	Do Not Pursue	098145193	12/25/2009	093045TW
TW	Chip Packages	Do Not Pursue	099109440	3/29/2010	093048TW
TW	Image and Light Sensor Chip Packages	Do Not Pursue	099104229	2/10/2010	093046TW
TW	Semiconductor chip structure	Do Not Pursue	096123392	6/28/2007	092995TW
TW	Chip structure and manufacturing process thereof	Do Not Pursue	096100892	5/27/2003	093120TW
TW	Chip package	Do Not Pursue	097113137	4/11/2008	093029TW

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
TW	Voltage regulator integrated with semiconductor chip	Do Not Pursue	096149614	12/24/2007	093026TW
TW	Chip assembly	Do Not Pursue	097108486	3/11/2008	093028TW
TW	Chip package and method for fabricating the same	Do Not Pursue	096127428	7/27/2007	093019TW
TW	Chip structure and process for forming the same	Do Not Pursue	097143274	5/25/2006	093007TW2
US	Chip Package	Abandoned	13/105,866	5/11/2011	093029C1
US	Structure and manufacturing method of a chip scale package with low fabrication cost, fine pitch and high reliability solder bump	Abandoned	12/852,467	8/7/2010	092977B1C4C1
US	Structure and manufacturing method of a chip scale package with low fabrication cost, fine pitch and high reliability solder bump	Abandoned	12/852,470	8/7/2010	092977B1C4C1C2
US	Chip packages with power management integrated circuits and related techniques	Abandoned	12/645,361	12/22/2009	093045
US	High performance IC chip having discrete decoupling capacitors attached to its IC surface	Abandoned	13/735,894	1/7/2013	093017D1
US	Chip structure with a passive device and method for forming the same	Abandoned	13/851,050	3/26/2013	093022C1
US	Method of assembling chips	Abandoned	12/121,778	5/15/2008	093021D1C2

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	Method of assembling chips	Abandoned	12/109,367	4/25/2008	093021D1C1
US	High performance system-on-chip using post passivation process	Abandoned	09/637,926	8/14/2000	093036B2
US	Structure and manufacturing method of a chip scale package	Abandoned	09/837,007	4/18/2001	092977B1
US	Integrated circuit chips with fine-line metal and over-passivation metal	Abandoned	11/865,059	9/30/2007	093129U7
US	Integrated circuit chips with fine-line metal and over-passivation metal	Abandoned	11/864,926	9/29/2007	093129U2
US	Method of manufacture and identification of semiconductor chip marked for identification with internal marking indicia and protection thereof by non-black layer and device Produced Thereby	Abandoned	12/260,086	10/28/2008	093038C1
US	High performance system-on-chip using post passivation process	Abandoned	11/877,651	10/23/2007	093036B2B1B1D3C1D1C7
US	Method of metal sputtering for integrated circuit metal routing	Abandoned	10/954,781	9/30/2004	092980C1
US	Top layers of metal for high performance ICs	Abandoned	11/893,659	8/17/2007	093036B1D1D1C1C7C50
US	Top layers of metal for high performance ICs	Abandoned	11/930,185	10/31/2007	093036B1D1D1C1C7C51
US	Top layers of metal for high performance ICs	Abandoned	11/930,187	10/31/2007	093036B1D1D1C1C7C52
US	Top layers of metal for high	Abandoned	11/930,189	10/31/2007	093036B1D1D1C1C7C53

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
	performance ICs				
US	Top layers of metal for high performance IC's	Abandoned	12/036,306	2/25/2008	093036B1D1D1C1C7C55
US	Top layers of metal for high performance ICs	Abandoned	12/186,523	8/6/2008	093036B1C1B1D1C2C1
US	Method of manufacture and indentification of semiconductor chip marked for identification with internal marking indicia and protection thereof by non-black layer and device produced thereby	Abandoned	09/523,990	3/13/2000	093038
US	Top layers of metal for high performance IC's	Abandoned	09/216,791	12/21/1998	093036
US	Process of rectifying a wafer thickness	Abandoned	09/997,941	11/29/2001	092954
US	Method of metal sputtering for integrated circuit metal routing	Abandoned	10/336,871	1/6/2003	092980
US	Method for improving semiconductor wafer test accuracy	Abandoned	10/786,807	2/25/2004	093015
US	High performance integrated circuit device and method of making the same	Abandoned	11/420,226	5/25/2006	093007
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/518,596	9/8/2006	092990B2R1C4
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/518,598	9/8/2006	092990B2R1C5

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/730,607	4/3/2007	092990B2R1C6
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/730,608	4/3/2007	092990B2R1C7
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/730,609	4/3/2007	092990B2R1C8
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/730,610	4/3/2007	092990B2R1C9
US	Electrodes for electroplating planar structures	Abandoned	11/545,822	10/10/2006	092986D1R1
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/203,646	8/12/2005	092990B2R1
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/518,592	9/8/2006	092990B2R1C1
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/730,611	4/3/2007	092990B2R1C10
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/730,612	4/3/2007	092990B2R1C11
US	Post passivation metal scheme for high-performance integrated circuit	Abandoned	11/730,613	4/3/2007	092990B2R1C12

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
	devices				
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/930,140	10/31/2007	092990B2R1C13
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/930,151	10/31/2007	092990B2R1C14
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/930,166	10/31/2007	092990B2R1C15
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/930,174	10/31/2007	092990B2R1C16
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/930,179	10/31/2007	092990B2R1C17
US	Post passivation metal scheme for high-performance integrated circuit devices	Abandoned	11/518,594	9/8/2006	092990B2R1C2
US	High performance system-on-chip using post passivation process	Abandoned	12/208,353	9/11/2008	093036B2B1B1D3C1D1C8C1
US	High performance system-on-chip inductor using post passivation process	Abandoned	11/668,483	1/30/2007	093036B2B1B1D3C1B1C4
US	High performance system-on-chip inductor using post passivation process	Abandoned	11/668,484	1/30/2007	093036B2B1B1D3C1B1C5
US	Top layers of metal for high performance ICs	Abandoned	11/839,560	8/16/2007	093036B1D1D1C1C7C16

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	Top layers of metal for high performance ICs	Abandoned	11/839,561	8/16/2007	093036B1D1D1C1C7C17
US	Top layers of metal for high performance ICs	Abandoned	11/840,230	8/17/2007	093036B1D1D1C1C7C18
US	Top layers of metal for high performance ICs	Abandoned	11/840,231	8/17/2007	093036B1D1D1C1C7C19
US	Top layers of metal for high performance ICs	Abandoned	11/829,106	7/27/2007	093036B1D1D1C1C7C2
US	Top layers of metal for high performance ICs	Abandoned	11/840,232	8/17/2007	093036B1D1D1C1C7C20
US	Top layers of metal for high performance ICs	Abandoned	11/840,233	8/17/2007	093036B1D1D1C1C7C21
US	Top layers of metal for high performance ICs	Abandoned	11/840,234	8/17/2007	093036B1D1D1C1C7C22
US	Top layers of metal for high performance ICs	Abandoned	11/840,235	8/17/2007	093036B1D1D1C1C7C23
US	Top layers of metal for high performance ICs	Abandoned	11/840,236	8/17/2007	093036B1D1D1C1C7C24
US	Top layers of metal for high performance ICs	Abandoned	11/840,237	8/17/2007	093036B1D1D1C1C7C25
US	Top layers of metal for high performance ICs	Abandoned	11/840,238	8/17/2007	093036B1D1D1C1C7C26
US	Top layers of metal for high performance ICs	Abandoned	11/839,552	8/16/2007	093036B1D1D1C1C7C10
US	Top layers of metal for high performance ICs	Abandoned	11/839,556	8/16/2007	093036B1D1D1C1C7C12

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	Top layers of metal for high performance ICs	Abandoned	11/839,557	8/16/2007	093036B1D1D1C1C7C13
US	Top layers of metal for high performance ICs	Abandoned	11/829,107	7/27/2007	093036B1D1D1C1C7C3
US	Top layers of metal for high performance ICs	Abandoned	11/840,243	8/17/2007	093036B1D1D1C1C7C30
US	Top layers of metal for high performance ICs	Abandoned	11/833,225	8/2/2007	093036B1D1D1C1C7C7
US	Top layers of metal for high performance ICs	Abandoned	11/839,550	8/16/2007	093036B1D1D1C1C7C8
US	Top layers of metal for high performance ICs	Abandoned	11/839,551	8/16/2007	093036B1D1D1C1C7C9
US	High performance system-on-chip inductor using post passivation process	Abandoned	11/653,171	1/12/2007	093036B2B1B1D3C1B1C1
US	Top layers of metal for integrated circuits	Abandoned	12/142,829	6/20/2008	093077C1
US	Integrated circuit chip with discrete component over passivation layer	Abandoned	11/874,906	10/19/2007	093036B2B1B1D3C1D1C1
US	Top layers of metal for high performance ICs	Abandoned	12/036,309	2/25/2008	093036B1D1D1C1C7C57
US	Top layers of metal for high performance ICs	Abandoned	11/845,759	8/27/2007	093036B1D1D1C1C7C44
US	Top layers of metal for high performance ICs	Abandoned	11/845,764	8/27/2007	093036B1D1D1C1C7C45
US	Top layers of metal for high performance ICs	Abandoned	11/840,241	8/17/2007	093036B1D1D1C1C7C28

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	Top layers of metal for high performance ICs	Abandoned	11/845,771	8/27/2007	093036B1D1D1C1C7C47
US	Top layers of metal for high performance ICs	Abandoned	11/845,773	8/27/2007	093036B1D1D1C1C7C48
US	Top layers of metal for high performance ICs	Abandoned	11/842,158	8/21/2007	093036B1D1D1C1C7C32
US	Top layers of metal for high performance ICs	Abandoned	11/842,159	8/21/2007	093036B1D1D1C1C7C33
US	Top layers of metal for high performance ICs	Abandoned	11/842,161	8/21/2007	093036B1D1D1C1C7C35
US	Top layers of metal for high performance ICs	Abandoned	11/845,110	8/27/2007	093036B1D1D1C1C7C37
US	Top layers of metal for high performance ICs	Abandoned	11/845,111	8/27/2007	093036B1D1D1C1C7C38
US	Top layers of metal for high performance ICs	Abandoned	11/845,113	8/27/2007	093036B1D1D1C1C7C39
US	Top layers of metal for high performance ICs	Abandoned	11/845,122	8/27/2007	093036B1D1D1C1C7C42
US	Post passivation interconnection schemes on top of IC chip	Abandoned	11/854,556	9/13/2007	092990D1C1C1C3
US	Post passivation interconnection schemes on top of IC chip	Abandoned	11/854,559	9/13/2007	092990D1C1C1C4
US	High performance system-on-chip using post passivation process	Abandoned	11/957,510	12/17/2007	093036B2B1B1D3C1D1C11
US	High performance system-on-chip using post passivation process	Abandoned	11/874,909	10/19/2007	093036B2B1B1D3C1D1C2

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	High performance system-on-chip using post passivation process	Abandoned	11/874,910	10/19/2007	093036B2B1B1D3C1D1C3
US	Low fabrication cost, fine pitch and high reliability solder bump	Abandoned	11/930,149	10/31/2007	092977D1C1
US	Low fabrication cost, fine pitch and high reliability solder bump	Abandoned	11/930,156	10/31/2007	092977D1C2
US	Structure and manufacturing method of a chip scale package	Abandoned	11/389,717	3/27/2006	092977B1C1
US	Low fabrication cost, fine pitch and high reliability solder bump	Abandoned	12/098,468	4/7/2008	092977D1C5
US	Low fabrication cost, fine pitch and high reliability solder bump	Abandoned	12/098,469	4/7/2008	092977D1C6
US	Structure and manufacturing method of a chip scale package with low fabrication cost, fine pitch and high reliability solder bump	Abandoned	12/384,977	4/9/2009	092977B1C4
US	Multiple chips bonded to packaging structure with low noise and multiple selectable functions	Abandoned	12/269,054	11/12/2008	092969C2
US	Chip package	Abandoned	12/202,341	9/1/2008	092957C1
US	Method for fabricating circuitry component	Abandoned	10/933,961	9/2/2004	093036B4D2D1
US	Thin film semiconductor package and method of fabrication	Abandoned	10/690,350	10/21/2003	092984D1
US	High performance system-on-chip using post passivation process	Do Not Pursue	11/877,652	10/23/2007	093036B2B1B1D3C1D1C8

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	High performance system-on-chip using post passivation process	Do Not Pursue	11/877,654	10/23/2007	093036B2B1B1D3C1D1C9
US	Semiconductor device with metal pillar	Do Not Pursue	10/055,580	1/22/2002	093032
US	System-on-chip with post-passivation capacitor	Do Not Pursue	12/365,180	2/4/2009	093034C1
US	Top layers of metal for high performance ICs	Do Not Pursue	11/845,109	8/27/2007	093036B1D1D1C1C7C36
US	High performance system-on-chip using post passivation process	Do Not Pursue	11/957,509	12/17/2007	093036B2B1B1D3C1D1C10
US	High performance system-on-chip inductor using post passivation process	Do Not Pursue	11/668,481	1/30/2007	093036B2B1B1D3C1B1C2
US	High performance system-on-chip inductor using post passivation process	Do Not Pursue	11/668,482	1/30/2007	093036B2B1B1D3C1B1C3
US	High performance system-on-chip using post passivation process	Do Not Pursue	11/877,641	10/23/2007	093036B2B1B1D3C1D1C4
US	System in-package	Expired	61/229,756	7/30/2009	093050P2
US	AU landing on IC pads	Expired	60/703,933	7/29/2005	093004P2
US	Semiconductor integrated circuit package with flexible interposal	Expired	60/914,771	4/30/2007	093029P2
US	Composite metal bump and package	Expired	60/911,514	4/12/2007	093028P2
US	Wire bonding pad structure of integrated circuit device	Expired	60/418,551	10/15/2002	092968P1
US	High performance IC chip having discrete decoupling capacitors	Expired	60/455,154	3/17/2003	093017P1

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
	attached to its IC surface				
US	Post-passivation metal scheme on an IC chip with copper interconnection	Expired	60/489,564	7/23/2003	092958P1
US	Post-passivation metal scheme on an IC chip with copper interconnection	Expired	60/580,747	6/18/2004	093005P1
US	Structure of gold bumps and gold conductors on one IC die and methods of manufacturing the structures	Expired	60/586,840	7/9/2004	092962P1
US	Thick gold conductor on IC chip	Expired	60/588,595	7/16/2004	093009P1
US	Very thick metal interconnection scheme in IC chips	Expired	60/592,358	7/29/2004	093011P1
US	Carbon allotropy on a chip and package	Expired	60/597,351	11/28/2005	093001P1
US	Pad for testing	Expired	60/597,493	12/5/2005	093002P1
US	Gold bump array on IC chip	Expired	60/623,553	10/29/2004	093010P1
US	Underfill dam on chip-on-chip assembly structure	Expired	60/647,129	1/25/2005	093018P1
US	Contacting and stress relieving system for IC chip	Expired	60/678,525	5/6/2005	092961P1
US	On chip transformer	Expired	60/682,721	5/18/2005	092960P1
US	Very thick metal interconnection scheme in IC chip	Expired	60/684,815	5/25/2005	093007P1
US	Packaging structure with stress relieving system built on IC chip	Expired	60/693,549	6/24/2005	093006P1

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	Double embossing structure	Expired	60/701,849	7/22/2005	093003P1
US	AU landing pads with barrier Ni on IC pads	Expired	60/703,932	7/29/2005	093004P1
US	System-in package	Expired	60/705,537	8/4/2005	093050P1
US	Over passivation metal RC scheme	Expired	60/711,281	8/25/2005	093051P1
US	Integrated circuit chips with voltage regulators and over-passivation metal	Expired	60/715,473	9/9/2005	093052P1
US	Wirebonding on thick polymer layer	Expired	60/743,426	3/7/2006	092999P1
US	Chip structure and method for fabricating thereof	Expired	60/767,080	3/2/2006	093000P1
US	Non-cyanide Au electroplating for fine-line Au traces and gold pads	Expired	60/801,067	5/18/2006	092998P1
US	Very thick metal interconnection scheme in IC chip	Expired	60/805,981	6/27/2006	092996P1
US	Enhanced barrier/adhesion layer between two metals	Expired	60/805,986	6/28/2006	092997P1
US	Post passivation metal scheme on an IC chip with copper interconnection	Expired	60/805,987	6/28/2006	092995P1
US	BGA package and method for making the same	Expired	60/822,085	8/11/2006	093019P1
US	Bump pad structure and fabrication method	Expired	60/824,614	9/6/2006	093024P1
US	Pad structure for wire bonding package	Expired	60/824,617	9/6/2006	093023P1

Inactive Cases: Megit Acquisition Corp.

Country	Title	Status	Application No.	Filing Date	Qualcomm Docket No.
US	Method for forming post passivation Au layer with clean surface	Expired	60/868,353	12/4/2006	093025P1
US	Fully integrated on chip regulator	Expired	60/871,837	12/26/2006	093026P1
US	Composite metal bump and package	Expired	60/894,459	3/13/2007	093028P1
US	Semiconductor integrated circuit package with Flexible interposal	Expired	60/911,512	4/12/2007	093029P1
US	Wirebond over Post passivation thick metal	Expired	60/968,082	8/27/2007	093037P1
US	Voltage regulator integrated with semiconductor chip	Expired	61/140,895	12/26/2008	093045P1
US	Image sensor	Expired	61/151,529	2/11/2009	093046P1
US	Integrated Circuit Chip Using Top Post-Passivation Technology And Bottom Post-Passivation Technology	Expired	61/164,473	3/30/2009	093047P1
US	Chip Package	Expired	61/164,914	3/31/2009	093048P1
US	System-in Package	Expired	61/178,493	5/14/2009	093049P1