## PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1 Stylesheet Version v1.2 EPAS ID: PAT3967287

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

## **CONVEYING PARTY DATA**

Name	Execution Date
HGST, INC.	07/12/2016

## **RECEIVING PARTY DATA**

Name:	JPMORGAN CHASE BANK, N.A., AS COLLATERAL AGENT	
Street Address:	IL 1-1145/54/63, P.O. BOX 6026	
City:	CHICAGO	
State/Country:	ILLINOIS	
Postal Code:	60680	

## **PROPERTY NUMBERS Total: 57**

Property Type	Number
Patent Number:	7038870
Application Number:	14794762
Patent Number:	7460384
Patent Number:	9195540
Application Number:	14733919
Application Number:	14743132
Patent Number:	9305624
Patent Number:	9270269
Patent Number:	7682981
Patent Number:	7149934
Patent Number:	9070878
Application Number:	13385371
Patent Number:	9349448
Application Number:	14561679
Application Number:	14616128
Patent Number:	5889694
Patent Number:	6586327
Patent Number:	6598164
Patent Number:	6956757
Patent Number:	7183206

PATENT REEL: 039389 FRAME: 0684

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Patent Number:         7376008           Patent Number:         7548454           Patent Number:         7593256           Patent Number:         7593246           Patent Number:         7652916           Patent Number:         7667996           Patent Number:         RE41733           Patent Number:         7813157           Patent Number:         7916530           Patent Number:         7933133           Patent Number:         8000129           Patent Number:         8000129           Patent Number:         8108735           Patent Number:         8116109           Patent Number:         8325556           Patent Number:         8351238           Patent Number:         8358526           Patent Number:         8358526           Patent Number:         8378456           Patent Number:         8451024           Patent Number:         8526217           Patent Number:         8537618           Patent Number:         8635426           Patent Number:         873881           Patent Number:         873881           Patent Number:         8980532           Patent Number:         8980532	Property Type	Number
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Patent Number: 7507663	Patent Number:	8980532
	Patent Number:	9007801
Application Number: 14795836	Patent Number:	7507663
	Application Number:	14795836
Patent Number: 9054031	Patent Number:	9054031

#### **CORRESPONDENCE DATA**

#### Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Email: michael.barys@thomsonreuters.com

Correspondent Name: ELAINE CARRERA, LEGAL ASSISTANT

Address Line 1: 80 PINE STREET

Address Line 2: C/O CAHILL GORDON & REINDEL LLP

Address Line 4: NEW YORK, NEW YORK 10005

NAME OF SUBMITTER:	ELAINE CARRERA
SIGNATURE:	/Michael Barys/
DATE SIGNED:	07/19/2016

#### **Total Attachments: 7**

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#### **Patent Collateral Agreement**

This July 12, 2016, HGST, INC. ("Debtor"), for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, grants to JPMORGAN CHASE BANK, N.A., a national banking association (the "Agent"), acting as collateral agent hereunder for the Secured Parties as defined in the Security Agreement, dated as of May 12, 2016, among Debtor, Agent and the other debtors party thereto, as the same may be amended, restated, amended and restated or otherwise modified from time to time (the "Security Agreement") for the benefit of the Secured Parties, a lien on and security interest in, all right, title, and interest of such Debtor in and to all of the following (collectively, "Patent Collateral"):

- (i) Each patent and patent application owned by Debtor, other than to the extent the same constitutes Excluded Property, that is listed on <u>Schedule A</u> hereto (the "*Patents*"); and
- (ii) All proceeds of the foregoing, including any claim by Debtor against third parties for damages by reason of past, present or future infringement of any Patent, in each case together with the right to sue for and collect said damages.

All capitalized terms used herein without definition have the meanings given to such terms in the Security Agreement.

Debtor and Agent do hereby further acknowledge and affirm that the rights and remedies of the Agent with respect to the grant of a security interest in the Patent Collateral made hereby are more fully set forth in, and subject to, the Security Agreement, the terms and provisions of which are incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Patent Collateral Agreement and the terms of the Security Agreement, the terms of the Security Agreement shall govern.

THIS PATENT COLLATERAL AGREEMENT AND THE RIGHTS AND OBLIGATIONS OF THE PARTIES HEREUNDER SHALL BE GOVERNED BY, AND CONSTRUED BY AND INTERPRETED IN ACCORDANCE WITH, THE LAW OF THE STATE OF NEW YORK.

[SIGNATURE PAGE TO FOLLOW]

IN WITNESS WHEREOF, Debtor has caused this Patent Collateral Agreement to be duly executed as of the date and year last above written.

HGST, INC., as Debtor

By:

Name: Michael C. Ray

Title: Secretary

**REEL: 039389 FRAME: 0688** 

Accepted and agreed to as of the date and year last above written.

JPMORGAN CHASE BANK, N.A., as Agent

By:

Name: Caitlin Stewart

Title: Vice President

REEL: 039389 FRAME: 0689

# SCHEDULE A TO PATENT COLLATERAL AGREEMENT

## U.S. PATENTS AND PATENT APPLICATIONS

	Erite	
1.	DATA STORAGE DEVICE, DATA WRITE METHOD, AND PROGRAM	7038870
2.	SELF-ALIGNED MEMORY CELL CONTACT	14/794762
3.	LOW COST HIGH DENSITY RECTIFIER MATRIX MEMORY	7460384
4.	Multiple sector parallel access memory array with error correction	9195540
5.	EMBEDDED NON-VOLATILE MEMORY	14/733919
6.	VARIABLE SELECTIVITY SILICON GROWTH PROCESS	14/743132
7.	Vertical switch three-dimensional memory array	9305624
8.	Bipolar-MOS memory circuit	9270269
9.	TOPOGRAPHY TRANSFER METHOD WITH ASPECT RATIO SCALING	7682981
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11.	PINCHED CENTER RESISTIVE CHANGE MEMORY CELL	9070878
12.	EMBEDDED NON-VOLATILE MEMORY	9054031
13.	Current steering element formation for memory arrays	13/385371
14.	OPERATING A RESISTIVE ARRAY	9349448
15.	MULTIPLE BIT PER CELL DUAL-ALLOY GST MEMORY ELEMENTS	14/561679
16.	SOLID STATE DEVICES HAVING FINE PITCH STRUCTURES	14/616128
17.	DUAL-ADDRESSED RECTIFIER STORAGE DEVICE	5889694
18.	FABRICATION OF SEMICONDUCTOR DEVICES	6586327
19.	DEVICE AND METHOD FOR REDUCING PIRACY OF DIGITIZED INFORMATION	6598164
20.	LOW COST HIGH DENSITY RECTIFIER MATRIX MEMORY	6956757
21.	FABRICATION OF SEMICONDUCTOR DEVICES	7183206
22.	SCR MATRIX STORAGE DEVICE	7376008

23.	MEMORY ARRAY WITH READOUT ISOLATION	7548454
24.	MEMORY ARRAY WITH READOUT ISOLATION	7548453
25.	MEMORY ARRAY WITH READOUT ISOLATION	7593256
26.	LOW COST HIGH DENSITY RECTIFIER MATRIX MEMORY	7593246
27.	SCR MATRIX STORAGE DEVICE	7652916
28.	NANO-VACUUM-TUBES AND THEIR APPLICATION IN STORAGE DEVICES	7667996
29.	DUAL-ADDRESSED RECTIFIER STORAGE DEVICE	RE41733
30.	NON-LINEAR CONDUCTOR MEMORY	7813157
31.	LOW COST HIGH DENSITY RECTIFIER MATRIX MEMORY	7826244
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33.	DUAL-ADDRESSED RECTIFIER STORAGE DEVICE	RE42310
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36.	BIPOLAR-MOS DRIVER CIRCUIT	8035416
37.	ERROR CORRECTING MEMORY ACCESS MEANS AND METHOD	8108735
38.	LOW-COST HIGH-DENSITY RECTIFIER MATRIX MEMORY	8116109
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46.	METHOD FOR FORMING SELF-ALIGNED PHASE-CHANGE SEMICONDUCTOR DIODE MEMORY	8455298
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49.	Diagonally accessed memory array circuit	8635426
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	STRUCTURES	
55.	Bipolar-MOS Memory Circuit	9007801
56.	FABRICATION OF SEMICONDUCTOR	7507663
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57.	NMOS REGULATED VOLTAGE REFERENCE	14/795,836

**RECORDED: 07/19/2016**