

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT4010187

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	SECURITY AGREEMENT	
CONVEYING PARTY DATA		
	Name	Execution Date
	CAVIUM, INC.	08/16/2016
	CAVIUM NETWORKS LLC	08/16/2016
RECEIVING PARTY DATA		
Name:	JPMORGAN CHASE BANK, N.A., AS COLLATERAL AGENT	
Street Address:	10 S. DEARBORN, FLOOR L-2	
Internal Address:	CB COLLATERAL SERVICES	
City:	CHICAGO	
State/Country:	ILLINOIS	
Postal Code:	60603	
PROPERTY NUMBERS Total: 422		
Property Type	Number	
Patent Number:	7941585	
Patent Number:	7594081	
Patent Number:	7606998	
Patent Number:	9141548	
Patent Number:	7895431	
Patent Number:	8392590	
Patent Number:	7535907	
Patent Number:	7613813	
Patent Number:	7930349	
Patent Number:	7558925	
Patent Number:	8560475	
Patent Number:	8818921	
Patent Number:	9336328	
Patent Number:	8301788	
Patent Number:	7096292	
Patent Number:	7653763	
Patent Number:	7436954	
Patent Number:	7243179	

PATENT

Property Type	Number
Patent Number:	7605658
Patent Number:	8471601
Patent Number:	8086609
Patent Number:	8819217
Patent Number:	8180803
Patent Number:	8176300
Patent Number:	8601139
Patent Number:	8677144
Patent Number:	8843764
Patent Number:	7949683
Patent Number:	8473523
Patent Number:	8886680
Patent Number:	7961033
Patent Number:	8356194
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Patent Number:	8826271
Patent Number:	9065781
Patent Number:	9264385
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Patent Number:	9239753
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Patent Number:	8525572
Patent Number:	8896360
Patent Number:	8519785
Patent Number:	9263151
Patent Number:	9143140
Patent Number:	9306584
Patent Number:	8634509
Patent Number:	8536944
Patent Number:	8456331
Patent Number:	9054729
Patent Number:	8350732
Patent Number:	9203805
Patent Number:	8937952
Patent Number:	8934488
Patent Number:	8937954
Patent Number:	9208438
Patent Number:	9191321

Property Type	Number
Patent Number:	8990259
Patent Number:	8885480
Patent Number:	9128769
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Patent Number:	9059836
Patent Number:	9129060
Patent Number:	8711861
Patent Number:	9031075
Patent Number:	8560757
Patent Number:	8850101
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Patent Number:	8606959
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Patent Number:	8995449
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Patent Number:	9065860
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Patent Number:	9195939
Patent Number:	9323715
Patent Number:	8963601

Property Type	Number
Patent Number:	9335784
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Patent Number:	9094669
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Patent Number:	9256380
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Application Number:	13565271
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Application Number:	14040431
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Application Number:	14192100
Application Number:	14045602
Application Number:	14045674
Application Number:	14040577

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Application Number:	14193899
Application Number:	14201541
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Application Number:	14328951
Application Number:	14514596
Application Number:	14637533
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Application Number:	14541902
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Application Number:	14638266
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Application Number:	14106827
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Application Number:	14140488
Application Number:	14140494
Application Number:	14140503
Application Number:	14140585
Application Number:	14141681
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Application Number:	14940982
Application Number:	14941082
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Application Number:	62274062
Application Number:	62274686
Application Number:	62279345
Application Number:	62335366
Application Number:	14141076
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Application Number:	14675710
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Application Number:	14673836
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Application Number:	14664680
Application Number:	14671900
Application Number:	14675450
Application Number:	14675307
Application Number:	14675356
Application Number:	14675342
Application Number:	14657403
Application Number:	12774608
Application Number:	14042403
Application Number:	14150602
Application Number:	14150622
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Application Number:	14537758
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Property Type	Number
Application Number:	14540927
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Application Number:	14542509
Application Number:	14542528
Application Number:	14577448
Application Number:	14609164
Application Number:	14616580
Application Number:	14662012
Application Number:	14667238
Application Number:	14675696
Application Number:	14681978
Application Number:	14723858
Application Number:	14829233
Application Number:	14870675
Application Number:	14939982
Application Number:	14941396

CORRESPONDENCE DATA

Fax Number: (800)914-4240

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 800-713-0755

Email: Michael.Violet@wolterskluwer.com

Correspondent Name: MICHAEL VIOLET

Address Line 1: 4400 EASTON COMMONS WAY

Address Line 2: SUITE 125

Address Line 4: COLUMBUS, OHIO 43219

NAME OF SUBMITTER:	ELAINE CARRERA
SIGNATURE:	/Elaine Carrera/
DATE SIGNED:	08/17/2016

Total Attachments: 19

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Patent Security Agreement

This **Patent Security Agreement** dated as of August 16, 2016 made by Cavium, Inc., as pledgors and debtors (in such capacities and together with any successors in such capacities, individually, a “Pledgor”, and, collectively, the “Pledgors”), in favor of JPMORGAN CHASE BANK, N.A., in its capacity as Collateral Agent pursuant to the Credit Agreement (as defined in the Security Agreement), as pledgee, assignee and secured party (in such capacities and together with any successors in such capacities, the “Collateral Agent”).

WITNESSETH:

WHEREAS, the Pledgors are party to a Security Agreement of even date herewith (as amended, amended and restated, supplemented or otherwise modified from time to time in accordance with the provisions thereof, the “Security Agreement”) made in favor of the Collateral Agent pursuant to which the Pledgors are required to execute and deliver this Patent Security Agreement;

NOW, THEREFORE, in consideration of the foregoing premises and other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, and to induce the Collateral Agent, for the benefit of the Secured Parties, to enter into the Credit Agreement, the Pledgors and the Collateral Agent hereby agree as follows:

SECTION 1. Defined Terms. Unless otherwise defined herein, terms defined in the Security Agreement and used herein have the meaning given to them in the Security Agreement.

SECTION 2. Grant of Security Interest in Patent Collateral. As collateral security for the payment and performance in full of all Secured Obligations, each Pledgor hereby pledges and grants to the Collateral Agent for the benefit of the Secured Parties, a lien on and security interest in all of the right, title and interest of such Pledgor in, to and under the following property, wherever located, and whether now existing or hereafter arising or acquired from time to time (collectively, the “Patent Collateral”):

(a) all patents and all patent applications (whether issued, allowed or filed in the United States or any other country or any trans-national patent registry) of such Pledgor now or hereafter, owned, filed or acquired by, or assigned to, such Pledgor, including the patents and patent applications listed on Schedule I attached hereto, together with any and all (i) rights and privileges arising under applicable law with respect to the foregoing and all rights corresponding thereto throughout the world, (ii) inventions, discoveries, designs and improvements described or claimed therein, (iii) reissues, divisions, continuations, reexaminations, extensions and continuations-in-part thereof and amendments thereto and (iv) rights to sue for past, present and future infringements thereof; and

(b) all Proceeds of any and all of the foregoing.

Notwithstanding anything to the contrary contained in clauses (a) and (b) above or otherwise set forth in this Patent Security Agreement, the security interest created by this Patent Security Agreement shall not extend to, and the term "Patent Collateral" shall not include, any Excluded Property.

SECTION 3. Security Agreement. The lien and security interest granted pursuant to this Patent Security Agreement is granted in conjunction with the lien and security interest granted to the Collateral Agent pursuant to the Security Agreement and the Pledgors hereby acknowledge and affirm that the rights and remedies of the Collateral Agent with respect to the security interest in the Patent Collateral made and granted hereby are more fully set forth in the Security Agreement, the terms and provisions of which are incorporated by reference herein as if fully set forth herein. In the event that any provision of this Patent Security Agreement is deemed to conflict with the Security Agreement, the provisions of the Security Agreement shall control unless the Collateral Agent shall otherwise determine.

SECTION 4. Termination. Upon the payment in full of the Secured Obligations and termination of the Security Agreement and at the other times required by Section 9.15 of the Credit Agreement, the Collateral Agent shall execute, acknowledge, and deliver to the Pledgors an instrument in writing in recordable form releasing the collateral pledge, grant, assignment, lien and security interest in the Patent Collateral under this Patent Security Agreement, all at the Pledgors' sole cost and expense.

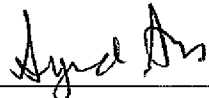
SECTION 5. Counterparts. This Patent Security Agreement and any amendments, waivers, consents or supplements hereto may be executed in any number of counterparts and by different parties hereto in separate counterparts, each of which when so executed and delivered shall be deemed to be an original, but all such counterparts together shall constitute one and the same instrument. Delivery of any executed counterpart of a signature page of this Patent Security Agreement by facsimile or other electronic transmission shall be effective as delivery of a manually executed counterpart of this Patent Security Agreement.

SECTION 6. Governing Law; Consent to Jurisdiction and Service of Process; Waiver of Jury Trial. Sections 9.09 and 9.10 of the Credit Agreement are incorporated herein, *mutatis mutandis*, as if a part hereof.

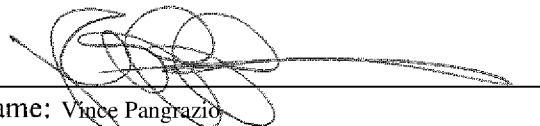
[signature page follows]

IN WITNESS WHEREOF, each Pledgor and the Collateral Agent have caused this Patent Security Agreement to be duly executed and delivered by their duly authorized officers as of the date first above written.

CAVIUM, INC., as Pledgor

By: 
Name: Syed Ali
Title: Chief Executive Officer

CAVIUM NETWORKS LLC, as Pledgor

By: 
Name: Vince Pangrazio
Title: Secretary

[Signature Page to Patent Security Agreement]

Accepted and Agreed:

JPMORGAN CHASE BANK, N.A.,
as Collateral Agent

By: 

Name:

Timothy D. Lee

Title:

Vice President

[Signature Page to Patent Security Agreement]

PATENT

REEL: 039715 FRAME: 0465

SCHEDULE I
to
PATENT SECURITY AGREEMENT
UNITED STATES PATENT REGISTRATIONS AND UNITED STATES PATENT
APPLICATIONS

United States Patent Registrations:

<u>OWNER</u>	<u>REGISTRATION NUMBER</u>	<u>DESCRIPTION</u>
Cavium, Inc.	7,941,585	Local Scratchpad And Data Caching System
Cavium, Inc.	7,594,081	Direct Access To Low-Latency Memory
Cavium, Inc.	7,606,998	Store Instruction Ordering For Multi-Core Processor
Cavium, Inc.	9,141,548	Method And Apparatus For Managing Write Back Cache
Cavium, Inc.	7,895,431	Packet Queuing, Scheduling And Ordering
Cavium, Inc.	8,392,590	Deterministic Finite Automata (DFA) Processing
Cavium, Inc.	7,535,907	TCP Engine
Cavium, Inc.	7,613,813	TCP Host
Cavium, Inc.	7,930,349	Method And Apparatus For Reducing Host Overhead In A Socket Server Implementation
Cavium, Inc.	7,558,925	Selective Replication Of Data Structures
Cavium, Inc.	8,560,475	Content Search Mechanism That Uses A Deterministic Finite Automata (DFA) Graph, A DFA State Machine, And A Walker Process
Cavium, Inc.	8,818,921	Content Search Mechanism That Uses A Deterministic Finite Automata (DFA) Graph, A DFA State Machine, And A Walker Process
Cavium, Inc.	9,336,328	Content Search Mechanism Using Finite Automata
Cavium, Inc.	8,301,788	Deterministic Finite Automata (DFA) Instruction
Cavium, Inc.	7,096,292	On-Chip Inter-Subsystem Communication
Cavium, Inc.	7,653,763	Subsystem Boot and Peripheral Data Transfer Architecture For A Subsystem of A System-On-Chip
Cavium, Inc.	7,436,954	Security System With An Intelligent Dma Controller
Cavium, Inc.	7,243,179	On-Chip Inter-Subsystem Communication
Cavium, Inc.	7,605,658	Resistively Loaded Single Stage Differential Amplifier Having Zero Volt Common Mode Input
Cavium, Inc.	8,471,601	Single-Ended to Differential Converter
Cavium, Inc.	8,086,609	Graph Caching
Cavium, Inc.	8,819,217	Intelligent Graph Walking
Cavium, Inc.	8,180,803	Deterministic Finite Automata (DFA) Graph Compression
Cavium, Inc.	8,176,300	Method And Apparatus For Content Based Searching
Cavium, Inc.	8,601,139	Multiple Core Session Initiation Protocol (SIP)
Cavium, Inc.	8,677,144	Secure Software And Hardware Association Technique

Cavium, Inc.	8,843,764	Secure Software And Hardware Association Technique
Cavium, Inc.	7,949,683	Method And Apparatus For Traversing A Compressed Deterministic Finite Automata (DFA) Graph
Cavium, Inc.	8,473,523	Deterministic Finite Automata Graph Traversal With Nodal Bit Mapping
Cavium, Inc.	8,886,680	Deterministic Finite Automata Graph Traversal With Nodal Bit Mapping
Cavium, Inc.	7,961,033	DLL-Based Temperature Sensor
Cavium, Inc.	8,356,194	Method And Apparatus For Estimating Overshoot After Estimating Power of Executing Events
Cavium, Inc.	8,868,949	Method And Apparatus For Power Control
Cavium, Inc.	8,826,271	Method And Apparatus For A Virtual System On Chip
Cavium, Inc.	9,065,781	Messaging With Flexible Transmit Ordering
Cavium, Inc.	9,264,385	Messaging With Flexible Transmit Ordering
Cavium, Inc.	8,977,944	DRAM Address Protection
Cavium, Inc.	9,239,753	DRAM Address Protection
Cavium, Inc.	8,513,994	State Machine For Deskew Delay Locked Loop
Cavium, Inc.	8,525,572	Level-Up Shifter Circuit
Cavium, Inc.	8,896,360	Level-Up Shifter Circuit For High Speed And Low Power Applications
Cavium, Inc.	8,519,785	Differential Amplifier With Duty Cycle Compensation
Cavium, Inc.	9,263,151	Memory Interface With Selectable Evaluation Modes
Cavium, Inc.	9,143,140	Multi-Function Delay Locked Loop
Cavium, Inc.	9,306,584	Multi-Function Delay Locked Loop
Cavium, Inc.	8,634,509	Synchronized Clock Phase Interpolator
Cavium, Inc.	8,536,944	Differential Amplifier With De-Emphasis
Cavium, Inc.	8,456,331	System And Method Of Compression And Decompression
Cavium, Inc.	9,054,729	System And Method Of Compression And Decompression
Cavium, Inc.	8,350,732	Compression With Adjustable Quality/Bandwidth Capability
Cavium, Inc.	9,203,805	Reverse NFA Generation And Processing
Cavium, Inc.	8,937,952	Packet Classification
Cavium, Inc.	8,934,488	Identifying Duplication in Decision Trees
Cavium, Inc.	8,937,954	Decision Tree Level Merging
Cavium, Inc.	9,208,438	Duplication In Decision Trees
Cavium, Inc.	9,191,321	Packet Classification
Cavium, Inc.	8,990,259	Anchored Patterns
Cavium, Inc.	8,885,480	Packet Priority In A Network Processor
Cavium, Inc.	9,128,769	Processor With Dedicated Virtual Functions And Dynamic Assignment Of Functional Resources
Cavium, Inc.	8,855,248	Word Boundary Lock
Cavium, Inc.	9,059,836	Word Boundary Lock
Cavium, Inc.	9,129,060	QoS Based Dynamic Execution Engine Selection
Cavium, Inc.	8,711,861	Lookup Front End Packet Input Processor
Cavium, Inc.	9,031,075	Lookup Front End Packet Input Processor

Cavium, Inc.	8,560,757	System And Method To Reduce Memory Access Latencies Using Selective Replication Across Multiple Memory Ports
Cavium, Inc.	8,850,101	System And Method To Reduce Memory Access Latencies Using Selective Replication Across Multiple Memory Ports
Cavium, Inc.	8,850,125	System And Method To Provide Non-Coherent Access To A Coherent Memory System
Cavium, Inc.	8,989,220	High Speed Variable Bandwidth Ring-Based System
Cavium, Inc.	9,059,945	Work Request Processor
Cavium, Inc.	8,473,658	Input Output Bridging
Cavium, Inc.	8,595,401	Input Output Bridging
Cavium, Inc.	8,606,959	Lookup Front End Packet Output Processor
Cavium, Inc.	9,344,366	A System And Method For Rule Matching In A Processor
Cavium, Inc.	8,472,452	Lookup Cluster Complex
Cavium, Inc.	8,995,449	Lookup Cluster Complex
Cavium, Inc.	9,225,643	Lookup Cluster Complex
Cavium, Inc.	9,137,340	Incremental Update
Cavium, Inc.	9,183,244	Rule Modification in Decision Trees
Cavium, Inc.	8,719,331	Work Migration In A Processor
Cavium, Inc.	8,966,152	On-Chip Memory (OCM) Physical Bank Parallelism
Cavium, Inc.	9,065,860	Method And Apparatus For Multiple Access Of Plural Memory Banks
Cavium, Inc.	9,319,316	A Method And Apparatus For Managing Transfer Of Transport Operations From A Cluster In A Processor
Cavium, Inc.	8,954,700	Method and Apparatus for Managing Processing Thread Migration Between Clusters Within A Processor
Cavium, Inc.	9,330,002	Multi-Core Interconnect In A Network Processor
Cavium, Inc.	9,065,626	Bit Error Rate Impact Reduction
Cavium, Inc.	9,219,560	Multi-Protocol Serdes Phy Apparatus
Cavium, Inc.	9,152,494	Method And Apparatus For Data Packet Integrity Checking In A Processor
Cavium, Inc.	8,923,306	Phased Bucket Pre-Fetch In A Network Processor
Cavium, Inc.	9,112,767	Method And An Accumulator Scoreboard For Out-Of-Order Rule Response Handling
Cavium, Inc.	9,130,819	Method And Apparatus For Scheduling Rule Matching In A Processor
Cavium, Inc.	9,276,846	Packet Extraction Optimization In A Network Processor
Cavium, Inc.	9,195,939	Scope In Decision Trees
Cavium, Inc.	9,323,715	Method And Apparatus To Represent A Processor Context With Fewer Bits
Cavium, Inc.	8,963,601	Clock Gated Delay Line Based On Setting Value
Cavium, Inc.	9,335,784	Clock Distribution Circuit With Distributed Delay Locked Loop
Cavium, Inc.	9,087,567	Method And Apparatus For Amplifier Offset Calibration
Cavium, Inc.	9,268,694	Maintenance Of Cache And Tags In A Translation Lookaside Buffer
Cavium, Inc.	9,041,432	Clock Multiplexing And Repeater Network
Cavium, Inc.	9,130,549	Multiplexer Flop
Cavium, Inc.	9,264,023	Scannable Flop With A Single Storage Element

Cavium, Inc.	9,208,103	Translation Bypass In Multi-Stage Address Translation
Cavium, Inc.	9,281,034	Data Strobe Generation
Cavium, Inc.	8,619,923	System And Method For Optimizing Use Of Channel State Information
Cavium, Inc.	8,891,706	System And Method For Optimizing Use Of Channel State Information
Cavium, Inc.	6,151,295 ¹	OFDM Receiving System
Cavium, Inc.	7,352,778 ²	Synchronizing Method And Apparatus
Cavium, Inc.	8,340,205	Method And Apparatus For Correcting Linear Error Phase Of An Ofdm Signal
Cavium, Inc.	7,035,889	Method And Apparatus For Montgomery Multiplication
Cavium, Inc.	6,954,770	Random Number Generator
Cavium, Inc.	6,789,147	Interface For A Security Coprocessor
Cavium, Inc.	7,240,203	Method And Apparatus For Establishing Secure Sessions
Cavium, Inc.	7,076,059	Method And Apparatus To Implement The Data Encryption Standard Algorithm
Cavium, Inc.	7,260,217	Speculative Execution For Data Ciphering Operations
Cavium, Inc.	7,305,567	Decoupled Architecture For Data Ciphering Operations
Cavium, Inc.	7,337,314	Apparatus And Method For Allocating Resources Within A Security Processor
Cavium, Inc.	6,861,865	Apparatus And Method For Repairing Logic Blocks
Cavium, Inc.	7,205,785	Apparatus And Method For Repairing Logic Blocks
Cavium, Inc.	7,209,531	Apparatus And Method For Data Deskew
Cavium, Inc.	7,814,310	Ipssec Performance Optimization
Cavium, Inc.	7,398,386	Transparent Ipssec Processing Inline Between A Framer And A Network Component
Cavium, Inc.	7,661,130	Apparatus And Method For Allocating Resources Within A Security Processing Architecture Using Multiple Queuing Mechanisms
Cavium, Inc.	7,657,933	Apparatus And Method For Allocating Resources Within A Security Processing Architecture Using Multiple Groups
Cavium, Inc.	6,949,423 ³	Mosfet-Fused Nonvolatile Read-Only Memory Cell (Mofrom)
Cavium, Inc.	8,009,923 ⁴	Method And System For Motion Estimation With Multiple Vector Candidates
Cavium, Inc.	8,661,266	System And Method For Secure Device Key Storage
Cavium, Inc.	8,544,106	System And Method For Enabling Access To A Protected Hardware Resource
Cavium, Inc.	9,025,672	On-Demand Intra-Refresh For End-To-End Coded Video Transmission Systems

¹ Outstanding lien: Comerica Bank security agreement executed 6/26/2009 and recorded 7/1/2009 at reel/frame 022892/0829

² Outstanding lien: Comerica Bank security agreement executed 6/26/2009 and recorded 7/1/2009 at reel/frame 022892/0829

³ There is a break in the chain of title. No assignment from "Oakvale Technology" to Celestial Semiconductor Ltd." Outstanding lien: Venture Lending & Leasing IV, Inc. security agreement executed 8/9/2006 and recorded 10/4/2006 at reel/frame 018454/0035

⁴ Outstanding lien: Venture Lending & Leasing IV, Inc. security agreement executed 8/9/2006 and recorded 10/4/2006 at reel/frame 018454/0035

Cavium, Inc.	8,831,108	Low Latency Rate Control System And Method
Cavium, Inc.	9,025,665	Video Encoder Bit Estimator For Macroblock Encoding
Cavium, Inc.	9,094,669	Video Encoder Bit Estimator For Macroblock Encoding
Cavium, Inc.	8,358,699	Method And System For Selection Of Reference Picture And Mode Decision
Cavium, Inc.	9,237,581	Apparatus And Method For Media Access Control Scheduling With A Sort Hardware Coprocessor
Cavium, Inc.	9,256,380	Apparatus And Method For Packet Memory Datapath Processing In High Bandwidth Packet Processing Devices
Cavium, Inc.	9,331,942	Apparatus And Method For Processing Alternately Configured Longest Prefix Match Tables
Cavium, Inc.	9,264,357	Apparatus And Method For Table Search With Centralized Memory Pool In A Network Switch
Cavium, Inc.	9,009,364	Apparatus And Method For Accelerated Page Link List Processing In A Packet Processor Operating At Wirespeed
Cavium, Inc.	9,262,369	Apparatus And Method For Accelerated Page Link List Processing In A Packet Processor Operating At Wirespeed
Cavium, Inc.	9,305,129	System For And Method Of Tuning Clock Networks Constructed Using Variable Drive-Strength Clock Inverters With Variable Drive-Strength Clock Drivers Built Out Of A Smaller Subset Of Base Cells
Cavium, Inc.	9,330,227	Testbench Reference Model and Scoreboard Dispatcher
Cavium, Inc.	7,693,070	Congestion Reducing Reliable Transport Packet Retry Engine
Cavium, Inc.	9,058,463	Systems And Methods For Specifying, Modeling, Implementing and Verifying IC Design Protocols
Cavium, Inc.	9,294,567	Systems And Methods For Enabling Access To Extensible Storage Devices Over A Network As Local Storage Via NVME Controller
Cavium, Inc.	9,307,057	Systems And Methods For Resource Management In A Single Instruction Multiple Data Packet Parsing Cluster
Cavium, Inc.	9,355,206	System And Method for Automated Functional Coverage Generation And Management For IC Design Protocols
Cavium, Inc.	9,378,033	Apparatus And Method For A Virtual System On Chip
Cavium, Inc.	9,398,033	Regular Express Processing Automaton

United States Patent Applications:

OWNER	APPLICATION NUMBER	DESCRIPTION
Cavium, Inc.	15/134,919	Content Search Mechanism Using Finite Automata
Cavium, Inc.	13/311,244	Graph Caching
Cavium, Inc.	14/324,682 ⁵	Intelligent Graph Walking
Cavium, Inc.	14/067,524 ⁶	Multiple Core Session Initiation Protocol (Sip)
Cavium, Inc.	14/340,225	Secure Software And Hardware Association Technique
Cavium, Inc.	14/516,807	Traversal With Arc Configuration Information

⁵ This patent application is in the process of being abandoned.

⁶ This patent application is in the process of being abandoned.

Cavium, Inc.	12/505,324 ⁷	Profile-Based And Dictionary Based Graph Caching
Cavium, Inc.	14/488,724	Method And Apparatus For Power Control
Cavium, Inc.	14/452,873	Method And Apparatus For A Virtual System On Chip
Cavium, Inc.	14/452,878	Method And Apparatus For A Virtual System On Chip
Cavium, Inc.	13/168,395	Regular Expression Processing Automaton
Cavium, Inc.	13/326,091	Messaging With Flexible Transmit Ordering
Cavium, Inc.	14/863,484	Reverse Nfa Generation And Processing
Cavium, Inc.	14/863,816 ⁸	Reverse Nfa Generation And Processing
Cavium, Inc.	13/168,450	Regex Compiler
Cavium, Inc.	14/632,448	Anchored Patterns
Cavium, Inc.	13/283,252	Packet Traffic Control In A Network Processor
Cavium, Inc.	13/274,767	Processor With Efficient Work Queuing
Cavium, Inc.	14/828,884	Qos Based Dynamic Execution Engine Selection
Cavium, Inc.	13/284,289	Network Processor With Distributed Trace Buffers
Cavium, Inc.	13/599,276	Lookup Front End Packet Input Processor
Cavium, Inc.	14/466,384	System And Method To Provide Non-Coherent Access To A Coherent Memory System
Cavium, Inc.	14/670,934	Work Request Processor
Cavium, Inc.	14/082,365	Lookup Front End Packet Output Processor
Cavium, Inc.	13/565,271	A System And Method For Storing Lookup Request Rules In Multiple Memories
Cavium, Inc.	13/565,389	A Method And Apparatus Encoding A Rule For A Lookup Request In A Processor
Cavium, Inc.	15/145,052	System And Method For Rule Matching In A Processor
Cavium, Inc.	13/831,191	Incremental Update Heuristics
Cavium, Inc.	14/230,698	Work Migration In A Processor
Cavium, Inc.	14/604,975 ⁹	On-Chip Memory (Ocm) Physical Bank Parallelism
Cavium, Inc.	13/565,741 (Patent No. 9,391,892)	A Method And Apparatus For Managing Transport Operations To A Cluster Within A Processor
Cavium, Inc.	13/565,746	Method And Apparatus For Assigning Resources Used To Manage Transport Operations Between Clusters Within A Processor
Cavium, Inc.	14/592,384	Method And Apparatus For Managing Processing Thread Migration Between Clusters Within A Processor
Cavium, Inc.	13/896,798	Compiler With Mask Nodes
Cavium, Inc.	14/207,933	Nsp Manager
Cavium, Inc.	14/207,928	Merging Independent Writes, Separating Dependent And Independent Writes, And Error Roll Back
Cavium, Inc.	13/831,415	Batch Incremental Update
Cavium, Inc.	13/841,743	Multi-Host Processing

⁷ This patent application is in the process of being abandoned.

⁸ This patent application is in the process of being abandoned.

⁹ This patent application is in the process of being abandoned.

Cavium, Inc.	14/583,968	Phased Bucket Pre-Fetch In A Network Processor
Cavium, Inc.	14/922,449	Scope In Decision Trees
Cavium, Inc.	14/325,841	Engine Architecture For Processing Finite Automata
Cavium, Inc.	14/252,293	Compilation Of Finite Automata Based On Memory Hierarchy
Cavium, Inc.	14/252,299	Processing Of Finite Automata Based On Memory Hierarchy
Cavium, Inc.	14/186,978	Generating A Non-Deterministic Finite Automata (Nfa) Graph For Regular Expression Patterns With Advanced Features
Cavium, Inc.	14/186,913	System And Method To Traverse A Non-Deterministic Finite Automata (Nfa) Graph Generated For Regular Expression Patterns With Advanced Features
Cavium, Inc.	14/169,967	Finite Automata Processing Based On A Top Of Stack (Tos) Memory
Cavium, Inc.	14/143,586	Method And Apparatus For Processing Of Finite Automata
Cavium, Inc.	14/252,354	Memory Management For Finite Automata Processing
Cavium, Inc.	14/015,248	Method And Apparatus For Compilation Of Finite Automata
Cavium, Inc.	14/015,929	Method And Apparatus For Processing Finite Automata
Cavium, Inc.	14/038,549	Method And Apparatus For Managing Global Chip Power On A Multicore System On Chip
Cavium, Inc.	14/038,156	Merged TLB Structure For Multiple Sequential Address Translations
Cavium, Inc.	14/038,189	Collapsed Address Translation With Multiple Page Sizes
Cavium, Inc.	14/040,532	Method And Apparatus For Reference Voltage Calibration In A Single-Ended Receiver
Cavium, Inc.	14/046,879	Method And Apparatus For Aligning Signals
Cavium, Inc.	14/040,431	Dynamically Adjusting Supply Voltage Based On Monitored Chip Temperature
Cavium, Inc.	14/039,846	Auto-Blow Memory Repair
Cavium, Inc.	14/036,709	Memory Interface With Integrated Tester
Cavium, Inc.	14/192,100	Cdr Voter With Improved Frequency Offset Tolerance
Cavium, Inc.	14/045,602	Method And Apparatus For Supporting Wide Operations Using Atomic Sequences
Cavium, Inc.	14/045,674 (Patent No. 9,390,023)	Method And Apparatus For Conditional Storing Of Data Using A Compare-And-Swap Based Approach
Cavium, Inc.	14/040,577	Method And Apparatus For Calibrating An Input Interface
Cavium, Inc.	14/193,899	Method And Apparatus For Power Gating Hardware Components In A Chip Device
Cavium, Inc.	14/201,541	Method And System For Work Scheduling In A Multi-Chip System
Cavium, Inc.	14/204,374	Method And Apparatus For Low Latency Exchange Of Data Between A Processor And Coprocessor
Cavium, Inc.	14/201,507 ¹⁰	Multi-Core Network Processor Interconnect With Multi-Node Connection
Cavium, Inc.	14/201,557	Method And System For Ordering I/O Access In A Multi-Node Environment
Cavium, Inc.	14/201,513 (Patent No. 9,372,800)	Inter-Chip Interconnect Protocol For A Multi-Chip System

¹⁰ This patent application is in the process of being abandoned.

Cavium, Inc.	14/194,049	System On Chip Link Layer Protocol
Cavium, Inc.	14/193,793	Partitioned Error Code Computation
Cavium, Inc.	14/186,743	Multiple Ethernet Ports And Port Types Using A Shared Data Path
Cavium, Inc.	14/193,895	Packet Output Processing
Cavium, Inc.	14/193,933 (Patent No. 9,397,938)	Packet Scheduling In A Network Processor
Cavium, Inc.	14/194,038	Packet Shaping In A Network Processor
Cavium, Inc.	14/191,163	Method And Apparatus For Memory Access Management
Cavium, Inc.	14/169,830	Method And Apparatus For Optimizing Finite Automata Processing
Cavium, Inc.	14/201,594	Method And Apparatus For Memory Allocation In A Multi-Node System
Cavium, Inc.	14/252,390	Processing Of Finite Automata Based On A Node Cache
Cavium, Inc.	14/538,484	Adder Decoder
Cavium, Inc.	14/540,175	Programmable Validation Of Transaction Requests
Cavium, Inc.	14/540,379	Programmable Ordering And Prefetch
Cavium, Inc.	14/540,414	Register Access Control Among Multiple Devices
Cavium, Inc.	14/540,656	Independent Ordering Of Independent Transactions
Cavium, Inc.	14/540,436	Arbitrated Access To Resources Among Multiple Devices
Cavium, Inc.	14/541,917	Bypass Fifo For Multiple Virtual Channels
Cavium, Inc.	14/940,981	Automatic Data Rate Matching
Cavium, Inc.	15/136,330	Method And Apparatus For Dynamic Virtual System On Chip
Cavium, Inc.	15/000,840	Voltage-Controlled Oscillator With Improved Tuning Curve Linearization
Cavium, Inc.	15/143,282	Edge Rate Control Calibration
Cavium, Inc.	15/143,302	Voltage Regulator With Adaptive Bias Network
Cavium, Inc.	14/328,923	Managing Instruction Order In A Processor Pipeline
Cavium, Inc.	14/328,951	Managing Instruction Order In A Processor Pipeline
Cavium, Inc.	14/514,596	Flexible Instruction Execution In A Processor Pipeline
Cavium, Inc.	14/637,533	Communication And Control Topology For Efficient Testing Of Sets Of Devices
Cavium, Inc.	14/514,708	Flexible Instruction Execution In A Processor Pipeline
Cavium, Inc.	14/541,498	Translation Lookaside Buffer Management
Cavium, Inc.	14/541,616	Caching Tlb Translations Using A Unified Page Table Walker Cache
Cavium, Inc.	14/541,726	Translation Lookaside Buffer Invalidation Suppression
Cavium, Inc.	14/541,807	Filtering Translation Lookaside Buffer Invalidations
Cavium, Inc.	14/541,826	Instruction Cache Translation Management
Cavium, Inc.	14/541,902	Managing Buffered Communication Between Sockets
Cavium, Inc.	14/541,882	Managing History Information For Branch Prediction
Cavium, Inc.	14/541,977	Testing Semiconductor Devices
Cavium, Inc.	14/541,952	Managing Skew In Data Signals
Cavium, Inc.	14/542,060	Controlled Multi-Step De-Alignment Of Clocks
Cavium, Inc.	14/542,039	Frequency Division Clock Alignment

Cavium, Inc.	14/542,136	Instruction Ordering For In-Progress Operations
Cavium, Inc.	14/542,118	Managing Buffered Communication Between Cores
Cavium, Inc.	14/542,188	Controlled Dynamic De-Alignment Of Clocks
Cavium, Inc.	14/542,202	Managing Skew In Data Signals With Multiple Modes
Cavium, Inc.	14/542,216	Frequency Division Clock Alignment Using Pattern Selection
Cavium, Inc.	14/672,787	Managing Skew In Data Signals With Adjustable Strobe
Cavium, Inc.	14/672,874 (Patent No. 9,349,434)	Variable Strobe For Alignment Of Partially Invisible Data Signals
Cavium, Inc.	14/637,579	Managing Reuse Information For Memory Pages
Cavium, Inc.	14/638,194	Managing Reuse Information With Mult Trans Stages
Cavium, Inc.	14/638,266	Managing Reuse Information In Caches
Cavium, Inc.	14/662,405	Managing Address-Independent Page Attributes
Cavium, Inc.	14/840,323	Local Instruction Ordering
Cavium, Inc.	15/088,302	Managing Translation Invalidation
Cavium, Inc.	15/088,354	Managing Synonyms In Virtual-Address Caches
Cavium, Inc.	15/193,535	Managing Virtual-Address Caches For Multiple Memory Page Sizes
Cavium, Inc.	14/083,894 (Patent No. 9,363,193)	Virtualized Network Interface For Tcp Reassembly Buffer Allocation
Cavium, Inc.	14/106,827	Virtualized Network Interface For Lockdown And Overlay Of Data In Transmitted Packets
Cavium, Inc.	14/106,841 (Patent No. 9,313,029)	Virtualized Network Interface For Remote Direct Memory Access Over Converged Ethernet
Cavium, Inc.	14/140,488 (Patent No. 9,306,916)	A System And A Method For A Remote Direct Memory Access Over Converged Ethernet
Cavium, Inc.	14/140,494	A Method And An Apparatus For Memory Address Allignment
Cavium, Inc.	14/140,503 (Patent No. 9,379,992)	A Method And An Apparatus For Virtualization Of A Quality-Of-Service
Cavium, Inc.	14/140,585	A Method And An Apparatus For Converting Interrupts Into A Scheduled Events
Cavium, Inc.	14/141,681	A Method And An Apparatus For Interrupt Collecting And Reporting
Cavium, Inc.	14/171,290	A Method And An Apparatus For Pre-Fetching And Processing Work For Procesor Cores In A Network Processor
Cavium, Inc.	14/141,987	A Look-Aside Processor Unit With Internal And External Access For Multicore Processors
Cavium, Inc.	14/171,108	A Method And An Apparatus For Work Request Arbitration In A Network Processor
Cavium, Inc.	14/170,955	A Method And An Apparatus For Work Packet Queuing, Scheduling, And Ordering With Conflict Queuing
Cavium, Inc.	14/447,732	A Method And An Apparatus For Co-Processor Data Plane Virtualization
Cavium, Inc.	14/542,485	Network Switching With Co-Resident Data-Plane And Network Interface Controllers
Cavium, Inc.	14/480,469	Low Latency Rate Control System And Method

Cavium, Inc.	13/830,492	Apparatus And Method For Media Access Control Scheduling With A Priority Calculation Hardware Coprocessor
Cavium, Inc.	14/630,554	Apparatus And Method For Software Enabled Access To Protected Hardware Resources
Cavium, Inc.	15/140,424	Apparatus And Method For Processing Alternately Configured Longest Prefix Match Tables
Xpliant, Inc.	13/921,090	Apparatus And Method For Uniquely Enumerating Paths In A Parse Tree
Cavium, Inc.	14/142,623	Apparatus And Method For Time Stamping Packets Across Several Nodes In A Network
Cavium, Inc.	14/142,631	Apparatus And Method For Optimizing The Number Of Accesses To Page-Reference Count Storage In Page Link List Based Switches
Cavium, Inc.	14/142,653	Method For Storing And Retrieving Packets In High-Bandwidth And Low-Latency Packet Processing Devices
Cavium, Inc.	9,275,336	Method And System For Skipping Over Group(S) Of Rules Based On Skip Group Rule 31686-3001
Cavium, Inc.	9,268,855	Processing Request Keys Based On A Key Size Supported By Underlying Processing Elements
Cavium, Inc.	14/145918	Multi-Rule Approach To Encoding A Group Of Rules 31686-3005
Cavium, Inc.	14/152817	Blocking Mask Register
Cavium, Inc.	14/150572	Method And Apparatus For Compiling Search Trees For Processing Request Keys Based On A Key Size Supported By Underlying Processing Elements
Cavium, Inc.	14/150761	Condition Code Approach For Comparing Rule And Key Data That Are Provided In Portions
Cavium, Inc.	14/940,538	Carry Chain For Simd Operations
Cavium, Inc.	14/940,585	Implementing 128-Bit Simd Operations On A 64-Bit Datapath
Cavium, Inc.	14/940,982	Multiple Memory Management Units
Cavium, Inc.	14/941,082	Distributing Resource Requests In A Computing System
Cavium, Inc.	14/940,679	Method And System For Compressing Data For A Translation Look Aside Buffer (Tlb)
Cavium, Inc.	14/941,182	Sharing Resources In A Multi-Context Computing System
Cavium, Inc.	14/838,088	Method And Apparatus For Providing A Low Latency Transmission System Using Adjustable Buffers
Cavium, Inc.	62/274,709	Method And Apparatus For Configuring Multiple Sectors WITH MULTIPLE RADIO FREQUENCY FRAMES
Cavium, Inc.	15/159,729	Method And Apparatus For Providing Soft And Blind Combining For PUSCH CQI Processing
Cavium, Inc.	62/267,221	Method And Apparatus For Providing Soft And Blind Combining Techniques For PUSCH Baseband Processing
Cavium, Inc.	62/288,382	Method And Apparatus For Providing FFT Engine Using Single Delay Feedback Scheme
Cavium, Inc.	62/274,062	Method And Apparatus For Providing Programmable Mixed-Radix DFT Processor Using Vector Engines
Cavium, Inc.	62/274,686	Method And Apparatus For Dynamically Generating Mixed-Radix Twiddle Coefficient Vectors
Cavium, Inc.	62/279,345	Method And Apparatus For Providing Programmable Mixed Radix DFT Processor Using Vector Memory Subsystem
Cavium, Inc.	62/335,366	Frequency Offset Estimation Method And Apparatus For LTE Uplink
Cavium, Inc.	14/141,076 (Patent No.	System For And Method Of Combining Cmos Inverters Of Multiple Drive Strengths To Create Tune-Able Clock Inverters Of Variable Drive

	9,390,209)	Strengths In Hybrid Tree-Mesh Clock Distribution Networks
Cavium, Inc.	14/141,096	System For And Method Of Placing And Routing Clock Stations Using Variable Drive Strength Clock Drivers Built Out Of A Smaller Subset Of Base Cells For Hybrid Tree-Mesh Clock Distribution Networks
Cavium, Inc.	14/144,260	Method And Apparatus For Parallel And Conditional Data Manipulation In A Software-Defined Network Processing Engine
Cavium, Inc.	14/142,497	A Matrix Of On-Chip Routers Interconnecting A Plurality Of Processing Engines And A Method Of Routing Using Thereof
Cavium, Inc.	14/142,511	Method And System For Reconfigurable Parallel Lookups Using Multiple Shared Memories
Cavium, Inc.	14/144,270 (Patent No. 9,379,963)	Apparatus And Method Of Generating Lookups And Making Decisions For Packet Modifying And Forwarding In A Software-Defined Network Engine
Cavium, Inc.	15/167,704	Apparatus And Method Of Generating Lookups And Making Decisions For Packet Modifying And Forwarding In A Software-Defined Network Engine
Cavium, Inc.	14/331,105	A Baseboard Interconnection Device, System And Method
Cavium, Inc.	14/289,533	Method And Apparatus For Flexible And Efficient Analytics In A Network Switch
Cavium, Inc.	14/289,548	Method And Apparatus For Table Aging In A Network Switch
Cavium, Inc.	14/302,343	Counter With Overflow Fifo And A Method Thereof
Cavium, Inc.	14/302,351	Hierarchical Statistically Multiplexed Counters And A Method Thereof
Cavium, Inc.	14/309,603	A Method Of Modifying Packets To A Generic Format For Enabling Programmable Modifications And An Apparatus Thereof
Cavium, Inc.	14/309,619	A Method Of Representing A Generic Format Header Using Continuous Bytes And An Apparatus Thereof
Cavium, Inc.	14/309,633	A Method Of Using A Unique Packet Identifier To Identify Structure Of A Packet And An Apparatus Thereof
Cavium, Inc.	14/309,650	A Method Of Using Generic Modification Instructions To Enable Flexible Modifications Of Packets And An Apparatus Thereof
Cavium, Inc.	14/309,659	A Method Of Using Bit Vectors To Allow Expansion And Collapse Of Header Layers Within Packets For Enabling Flexible Modifications And An Apparatus Thereof
Cavium, Inc.	14/309,679	A Method Of Splitting A Packet Into Individual Layers For Modification And Intelligently Stitching Layers Back Together After Modification And An Apparatus Thereof
Cavium, Inc.	14/309,700 ¹¹	A Leaky-Bucket Model To Mimic Behavior Of A Mac And A Method Thereof
Cavium, Inc.	14/309,726	A Method Of Extracting Data From Packets And An Apparatus Thereof
Cavium, Inc.	14/309,739	A Method Of Forming A Hash Input From Packet Contents And An Apparatus Thereof
Cavium, Inc.	14/309,763	A Method Of Handling Large Protocol Layers For Configurable Extraction Of Layer Information And An Apparatus Thereof
Cavium, Inc.	14/309,773	A Method Of Reducing Latency In A Flexible Parser And An Apparatus Thereof
Cavium, Inc.	14/309,789	A Method Of Dynamically Renumbering Ports And An Apparatus Thereof
Cavium, Inc.	14/309,802	A Method Of Internal Destinations For Network Packets And An Apparatus Thereof
Cavium, Inc.	14/675,710	A Programmable Integrated Circuit Compiler, System And Method

¹¹ This patent application is in the process of being abandoned.

Cavium, Inc.	14/675,702	A Programmable Integrated Circuit Compiler Having An Instruction Generator
Cavium, Inc.	14/675,692	A Programmable Integrated Circuit Compiler Having A Logic Generator
Cavium, Inc.	14/675,682	A Programmable Integrated Circuit Compiler Having A Cloud Mapper
Cavium, Inc.	14/494,168	A Hierarchical Hardware Linked List Approach For Multicast Replication Engine In A Network Asic
Cavium, Inc.	14/494,187	Fast Hardware Switchover In Control Path In A Network Asic
Cavium, Inc.	14/494,229	Session Based Packet Mirroring In A Network Asic
Cavium, Inc.	14/494,291	A Multicast Replication Engine Of A Network Asic And Methods Thereof
Cavium, Inc.	14/521,333	An Apparatus And A Method Of Detecting Errors On Registers
Cavium, Inc.	14/521,354	Two Modes Of Configuration Interface In A Network Asic
Cavium, Inc.	14/521,359	Smart Holding Register To Enable Multiple Register Access
Cavium, Inc.	14/521,367	Multiple-Interrupt Propagation Scheme In A Network Asic
Cavium, Inc.	14/536,937	Hybrid Wild-Card Match Table
Cavium, Inc.	14/932,791	Hybrid Wild-Card Match Table
Cavium, Inc.	14/671,993 (Patent No. 9,372,772)	Co-Verification Of Hardware And Software
Cavium, Inc.	14/617,522	Creating Generic Testbench Interface Driver
Cavium, Inc.	14/671,983	Device Verification Simulation Phase Synchronization
Cavium, Inc.	14/617,546	Testbench Builder
Cavium, Inc.	14/617,645	Testbench Generic Interface Monitor
Cavium, Inc.	14/675,667	A Parser Engine Programming Tool For Programmable Network Devices
Cavium, Inc.	14/675,674	A Programmable Integrated Circuit Compiler Having A Front End Parser
Cavium, Inc.	14/676,679	Acm Policer Architecture
Cavium, Inc.	14/672,016	Packet Tracking In A Verification Environment
Cavium, Inc.	14/617,699	Testbench Builder, System, Device And Method Having Agent Loopback Functionality
Cavium, Inc.	14/672,025	Testbench Builder, System, Device And Method Including Latency Detection
Cavium, Inc.	14/672,006	Software Assisted Hardware Configuration For Software Defined Network System-On-Chip
Cavium, Inc.	14/667,488	Packet Processor Forwarding Database Cache
Cavium, Inc.	14/667,568	Phantom Queue Link Level Load Balancing System, Method And Device
Cavium, Inc.	14/673,807	A Packet Memory System, Method And Device For Preventing Underrun
Cavium, Inc.	14/673,813	A Packet Processing System, Method And Device To Optimize Packet Buffer Space
Cavium, Inc.	14/673,819	A Packet Processing System, Method And Device Having Reduced Static Power Consumption
Cavium, Inc.	14/673,828	A Packet Processing System, Method And Device Utilizing A Port Client Chain
Cavium, Inc.	14/673,835	A Packet Processing System, Method And Device Utilizing Memory Sharing
Cavium, Inc.	14/673,836	A Control Path Subsystem, Method And Device Utilizing Memory Sharing
Cavium, Inc.	14/673,840	A Datapath Subsystem, Method And Device Utilizing Memory Sharing

Cavium, Inc.	14/675,728	A Barrel Compactor System, Method And Device
Cavium, Inc.	15/067,139	Pips: Protocol Independent Programmable Switch (Pips) For Software Defined Data Center Networks
Cavium, Inc.	14/675,734	A Barrel Compactor System, Method And Device Having Cell Combination Logic
Cavium, Inc.	14/634,446	Automated Flip-Flop Insertions In Physical Design Without Perturbation Of Routing
Cavium, Inc.	14/664,680	Repeater Insertions Providing Reduced Routing Perturbation Caused By Flip-Flop Insertions
Cavium, Inc.	14/671,900	Method And Apparatus For Bypass Routing Of Multicast Data Packets And Avoiding Replication To Reduce Overall Switch Latency
Cavium, Inc.	14/675,450	Method And Apparatus For Using Multiple Linked Memory Lists For Storing Tokens Of Data
Cavium, Inc.	14/675,307	Identifying Inversion Error In Logic Equivalence Check
Cavium, Inc.	14/675,356	Determination Of Flip-Flop Count In Physical Design
Cavium, Inc.	14/675,342	Approach For Chip-Level Flop Insertion And Verification Based On Logic Interface Definition
Gigavac, LLC	14/657,403	Approach For Logic Signal Rouping And Rtl Geneation Using Xml
Cavium, Inc.	12/774,608	System and Method For Low-Latency Multimedia Streaming
Cavium, Inc.	14/042,403	Protocol Switching Over Multi-Network Interface
Cavium, Inc.	14/150,602	System and Method For Single Instruction Multiple Data Programmable Packet Parsers
Cavium, Inc.	14/150,622	Packet Parsing Engine
Cavium, Inc.	14/150,635	Systems and Method For Distribution Of Packets Among Parsing Clusters
Cavium, Inc.	14/150,657	Systems and Methods For Flexible Packet Classification
Cavium, Inc.	14/150,664	Floating Mask Generation For Network Packet Flow
Cavium, Inc.	14/279,712	Systems and Methods for NVME Controller Virtualization to Support Multiple Virtual Machines Running On A Host
Cavium, Inc.	14/299,739	Systems and Methods For Cloud-Based Web Services Security Management Based on Hardware Security Module
Cavium, Inc.	14/317,467	Systems and Methods For Enabling Local Caching For Remote Storage Devices Over A Network , via NVME Controller
Cavium, Inc.	14/331,099	Network Device, System and Method Having A Rotated Chip Floorplan
Cavium, Inc.	14/473,111	Systems and Methods For Improving Data Integrity Using Compressed Soft Information
Cavium, Inc.	14/493,865	Apparatus and Method For Improving Data Integrity Using Compressed Soft Information
Cavium, Inc.	14/493,897	Apparatus and Method for Quantizing Soft Information Using Non-Linear LLR Quantization
Cavium, Inc.	14/493,953	Apparatus and Method for Quantizing Soft Information Using Linear Quantization
Cavium, Inc.	14/537,758	Systems and Methods For Supporting Migration Of Virtual Machines Accessing Remote Storage Devices Over Network Via NVME Controllers
Cavium, Inc.	14/540,868	Apparatus and Method For Scalable and Flexible Table Search In A Network Switch
Cavium, Inc.	14/540,927	Apparatus and Method For Fast Search Table Update In A Network Switch
Cavium, Inc.	14/541,685	Distributed Interrupt Scheme In A Multi-Processor System
Cavium, Inc.	14/541,769	Apparatus and Method For Distributed Instruction Trace In A Processor System

Cavium, Inc.	14/541,841	Apparatus and Method For Distributed Instruction Trace In A Processor System
Cavium, Inc.	14/541,917	Bypass FIFO for Multiple Virtual Channels
Cavium, Inc.	14/541,971	Debug Interface For Multiple CPU Cores
Cavium, Inc.	14/542,065	Distributed Timer Subsystem Across Multiple Devices
Cavium, Inc.	14/542,216	Frequency Division Clock Alignment Using Pattern Selection
Cavium, Inc.	14/542,298	Method and Apparatus For Performing A Weighted Queue Scheduling Using A Set Of Fairness Factors
Cavium, Inc.	14/542,350	Packet Scheduling Using Hierarchical Scheduling Process
Cavium, Inc.	14/542,383	Apparatus and Method For A Multi-Entity Secure Software Transfer
Cavium, Inc.	14/542,393	Packet Scheduling Using Hierarchical Scheduling Process With Priority Propagation
Cavium, Inc.	14/542,509	Management Of An Over-Subscribed Shared Buffer
Cavium, Inc.	14/542,528	Method and System For Improved Load Balancing Of Received Network Traffic
Cavium, Inc.	14/577,448	Network Switching With Layer 2 Switch Coupled Co-Resident Data-Plane And Network Interface Controllers
Cavium, Inc.	14/609,164	Method To Measure Edge-Rate Timing Penalty Of Digital Integrated Circuits
Cavium, Inc.	14/616,580	High Performance Shifter Circuit
Cavium, Inc.	14662,012	Systems and Methods For Secured Hardware Security Module Communication With Web Service Hosts
Cavium, Inc.	14667,238	Systems and Methods For Secured Key Management Via Hardware Security Module For Cloud-Based Web Services
Cavium, Inc.	14/675,696	Algorithm To Achieve Optimal Layout Of Instruction Tables For Programmable Network Devices
Cavium, Inc.	14/681,978	Systems and Methods For Hardware Accelerated Timer Implementation For Openflow Protocol
Cavium, Inc.	14/723,858	Systems and Methods For Secured Backup Of Hardware Security Modules For Cloud-Based Web Services
Cavium, Inc.	14/829233	Systems and Methods For Secured Communication Hardware Security Module And Network-Enabled Devices
Cavium, Inc.	14/870675	Systems and Methods For Allowing Flexible Chip Configuration By External Entity While Maintaining Secured Boot Environment
Cavium, Inc.	14/939982	Systems and Methods for Hardware Accelerated Metering for Openflow Protocol
Cavium, Inc.	14/941396	Systems and Methods For Enabling Local Caching For Remote Storage Devices Over A Network Via NVME Controller