PATENT ASSIGNMENT COVER SHEET

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Stylesheet Version v1.2

EPAS ID: PAT4075237

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
AEHR TEST SYSTEMS	09/06/2016

RECEIVING PARTY DATA

Name:	QVT FUND LP
Street Address:	1177 AVENUE OF THE AMERICAS, 9TH FLOOR
Internal Address:	C/O QVT FINANCIAL LP
City:	NEW YORK
State/Country:	NEW YORK
Postal Code:	10036
Name:	QUINTESSENCE FUND L.P.
Street Address:	1177 AVENUE OF THE AMERICAS, 9TH FLOOR
Internal Address:	C/O QVT FINANCIAL LP
City:	NEW YORK
State/Country:	NEW YORK
Postal Code:	10036

PROPERTY NUMBERS Total: 7

Property Type	Number
Patent Number:	9291668
Patent Number:	9316683
Application Number:	14918038
Application Number:	14973506
Application Number:	62276746
Application Number:	15060443
Application Number:	15015051

CORRESPONDENCE DATA

Fax Number: (703)610-6200

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 7036106100
Email: boxip@hoganlovells.com

Correspondent Name:	VALERIE BRENNAN, HOGAN LOVELLS US LLP
Address Line 1:	7930 JONES BRANCH DRIVE, 9TH FLOOR
Address Line 2:	ATTN: BOX INTELLECTUAL PROPERTY
Address Line 4:	MCLEAN, VIRGINIA 22102

NAME OF SUBMITTER:	VALERIE BRENNAN
SIGNATURE:	/vb/
DATE SIGNED:	09/29/2016

Total Attachments: 13
source=Aehr Test Security Agreement and Grant of Security#page1.tif
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September 6, 2016

Via E-mail and U.S. Mail

QVT Fund LP
Quintessence Fund L.P.
c/o QVT Financial LP
1177 Avenue of the Americas, 9th Floor
New York, NY 10036
Attn: Tracy Fu and Oren Eisner

Re: Aehr Test Systems – Security Agreement

Dear Ms. Fu and Mr. Eisner:

This letter constitutes written notice pursuant to the Security Agreement executed by Aehr Test Systems (the "Company") in favor of QVT Fund LP and Quintessence Fund L.P. dated as of April 10, 2015 (the "Security Agreement") of the changes in the Company's Intellectual Property (as defined in the Security Agreement) set forth on Exhibit A since the date of the Security Agreement.

Sincerely,

Aehr Test Systems

By: _____
Name: Gayn Erickson
Title: Chief Executive Officer

cc: Mark Heimlich, Hogan Lovells US LLP
Mark L. Reinstra, Wilson Sonsini Goodrich & Rosati, P.C.

Exhibit A

The following patents and patent applications have expired:

Application Number	File Date	Country Name	Patent Number	Issue Date	Invention Title
08/948,696	5/6/1997	United States of America	6,025,732	2/15/2000	REUSABLE DIE CARRIER FOR BURN-IN AND BURN-IN PROCESS
1998-709076	5/12/1997	Republic of Korea	468308	1/18/2005	REUSABLE DIE CARRIER FOR BURN-IN AND BURN-IN PROCESS
20107019151	8/19/2003	Republic of Korea	1062643	8/31/2011	DIE CARRIER
20107019149	8/19/2003	Republic of Korea	1062644	8/31/2011	DIE CARRIER
20057004550	8/19/2003	Republic of Korea	1019942	2/28/2011	DIE CARRIER
20077016269	12/7/2005	Republic of Korea	10-1177596	8/21/2012	A SYSTEM FOR TESTING AND BURNING IN OF INTEGRATED CIRCUITS
62066276	10/20/2014	United States of America			ELECTRONCIS TESTER WITH OUTPUT CIRCUITS OPERABLE IN VOLTAGE COMPENSATE D POWER MODE, DRIVER MODE OR CURRENT COMPENSATE D POWER MODE

The status of the following patent applications have changed from pending to issued:

Application Number	File Date	Country Name	Patent Number	Issue Date	Invention Title
14263826	4/28/2014	United States of America	9151797	10/6/2015	APPARATUS FOR TESTING ELECTRONIC DEVICES

2014241129	4/4/2008	Japan	5694480	2/13/2015	A PORTABLE PACK, A TESTER APPARATUS AND A METHOD OF TESTING A MICROELECTRI C CIRCUIT
13474581	5/17/2012	United States of America	9086449	7/21/2015	ADHESIVELY ATTACHED STAND- OFFS ON A PORTABLE PACK FOR AN ELECTRONICS TESTER
13554722	7/10/2012	United States of America	9250291	2/2/2016	SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE
201293894	12/15/2008	Singapore	186674	6/23/2016	SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE
99114534	5/6/2010	Taiwan	I484199	5/11/2015	SEPARATE TEST ELECTRONICS AND BLOWER MODULES IN AN APPARATUS FOR TESTING AN INTEGRATED CIRCUIT

The status of the following patents have changed from allowed to issued:

Application Number	**File Date**	**Country Name**	**Patent Number**	**Issue Date**	**Invention Title**
13223319	1/1/2011	United States of America	8947116	2/3/2015	SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND

					ITS METHOD
13168910	6/24/2011	United States of America	8986048	3/24/2015	INTEGRATED FEEDTHROUGH MODULE

The following patents have been issued:

Application Number	File Date	Country Name	Patent Number	Issue Date	Invention Title
58533894	12/7/2005	Germany	602005016146	8/19/2009	A SYSTEM FOR TESTING AND BURNING IN OF INTEGRATED CIRCUITS
104111527	5/6/2010	Taiwan	I519792	2/1/2016	SEPARATE TEST ELECTRONICS AND BLOWER MODULES IN AN APPARATUS FOR TESTING AN INTEGRATED CIRCUIT
14741273	6/16/2015	United States of America	9291668	3/22/2016	ELECTRONICS TESTER WITH A VALVE INTEGRALLY FORMED IN A COMPONENT OF A PORTABLE PACK
14833938	8/24/2015	United States of America	9316683	4/19/2016	APPARATUS FOR TESTING ELECTRONIC DEVICES

The following patent applications are pending:

Application Number	File Date	Country Name	Patent Number	Issue Date	Invention Title
10201604826R	12/15/2008	Singapore			SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE
14918038	10/20/2015	United States of America			ELECTRONICS TESTER WITH OUTPUT CIRCUITS

					OPERABLE IN VOLTAGE COMPENSATED POWER MODE, DRIVER MODE OR CURRENT COMPENSATED POWER MODE
104134353	10/20/2015	Taiwan			TESTER FOR DEVICE, METHOD OF OPERATING SWITCHING CIRCUIT, AND METHOD OF TESTING
PCTUS1556429	10/20/2015	WO			ELECTRONICS TESTER WITH OUTPUT CIRCUITS OPERABLE IN VOLTAGE COMPENSATED POWER MODE, DRIVER MODE OR CURRENT COMPENSATED POWER MODE
14973506	12/17/2015	United States of America			SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE
62276746	1/8/2016	United States of America			METHOD AND SYSTEM FOR THERMAL CONTROL OF DEVICES IN AN

					ELECTRONICS TESTER
15060443	3/3/2016	United States of America			APPARATUS FOR TESTING ELECTRONIC DEVICES

The following patents have been allowed:

Application Number	File Date	Country Name	Patent Number	Issue Date	Invention Title
15015051	2/3/2016	United States of America			ELECTRONICS TESTER WITH HOT FLUID THERMAL CONTROL

GRANT OF A SECURITY INTEREST -- PATENTS

This Patent Security Agreement (this "Patent Security Agreement") is made as of April 10, 2015, by Aehr Test Systems, a California corporation ("Grantor"), in favor of QVT Fund LP, a Cayman Islands limited partnership ("QVT Fund"), and Quintessence Fund L.P., a Cayman Islands limited partnership ("Quintessence", and together with QVT Fund and their respective successors and assigns in such capacity, "Grantees").

WHEREAS, the Grantor holds all right, title and interest in the letter patents, design patents and utility patents listed on the attached Schedule A, which patents are issued or applied for in the United States Patent and Trademark Office (the "Patents");

WHEREAS, the Grantor has entered into a Security Agreement, dated as of the date hereof (as amended, restated, supplemented, modified or otherwise changed from time to time, the "Security Agreement"), in favor of Grantees; and

WHEREAS, pursuant to the Security Agreement, the Grantor has granted to the Grantees, a continuing security interest in all right, title and interest of the Grantor in, to and under the Patents and the applications and registrations thereof, and all proceeds thereof, including, without limitation, any and all causes of action which may exist by reason of infringement thereof and any and all damages arising from past, present and future violations thereof (the "Collateral"), to secure the payment, performance and observance of the Obligations (as defined in the Security Agreement).

NOW, THEREFORE, as collateral security for the prompt and complete payment, performance and observance when due of all of the Obligations, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Grantor does hereby grant to the Grantees a continuing security interest in the Collateral to secure the prompt payment, performance and observance of the Obligations.

All capitalized terms used but not otherwise defined herein have the meanings given to them in the Security Agreement

The Grantor does hereby further acknowledge and affirm that the rights and remedies of the Grantees with respect to the Collateral are more fully set forth in the Security Agreement, the terms and provisions of which are hereby incorporated herein by reference as if fully set forth herein.

This Patent Security Agreement may be executed in any number of counterparts and by different parties in separate counterparts, each of which when so executed shall be deemed to be an original and all of which taken together shall constitute one and the same agreement. Delivery of an executed counterpart by facsimile or electronic mail shall be equally effective as delivery of an original executed counterpart.

This Patent Security Agreement shall be governed by and construed in accordance with the laws of the State of New York without reference to conflicts of law rules.

[*Remainder of page intentionally left blank*]

IN WITNESS WHEREOF, the Grantor has caused this Patent Security Agreement to be duly executed by its officer thereunto duly authorized as of the date first set forth above.

AEHR TEST SYSTEMS

By: Gary L. Larson
Name: Gary L. Larson
Title: Chief Financial Officer and Vice President of Finance

[Signature Page to Patent Security Agreement]

IN WITNESS WHEREOF, the Grantor has caused this Patent Security Agreement to be duly executed by its officer thereunto duly authorized as of the date first set forth above.

AEHR TEST SYSTEMS

By:_____
Name:
Title:

QUINTESSENCE FUND L.P.

By: QVT Associates GP LLC,
its general partner

By: _____
Name: Tracy Fu
Title: Managing Member

QVT FUND LP

By: QVT Associates GP LLC,
its general partner

By: _____
Name: Tracy Fu
Title: Managing Member

SCHEDULE A TO GRANT OF A SECURITY INTEREST

Patents and Patent Applications

	Title	Application No. / Publication No. / Patent No.	Filing Date / Issue Date
1.	ADHESIVELY ATTACHED STAND-OFFS ON A PORTABLE PACK FOR AN ELECTRONICS TESTER	13474581 20120223729	05/17/2012
2.	APPARATUS FOR TESTING ELECTRONIC DEVICES	11413323 7762822	04/27/2006 07/27/2010
3.	APPARATUS FOR TESTING ELECTRONIC DEVICES	11522216 7826995	09/14/2006 11/02/2010
4.	APPARATUS FOR TESTING ELECTRONIC DEVICES	12772932 8118618	05/03/2010 02/21/2012
5.	APPARATUS FOR TESTING ELECTRONIC DEVICES	13353269 8388357	01/18/2012 03/05/2013
6.	APPARATUS FOR TESTING ELECTRONIC DEVICES	13754765 8506335	01/30/2013 08/13/2013
7.	APPARATUS FOR TESTING ELECTRONIC DEVICES	13939364 8628336	07/11/2013 01/14/2014
8.	APPARATUS FOR TESTING ELECTRONIC DEVICES	14097541 8747123	12/05/2013 06/10/2014
9.	APPARATUS FOR TESTING ELECTRONIC DEVICES	14263826 20140232424	04/28/2014
10.	ASSEMBLY FOR ELECTRICALLY CONNECTING A TEST COMPONENT TO A TESTING MACHINE FOR TESTING ELECTRICAL CIRCUITS ON THE TEST COMPONENT	10197104 6867608	07/16/2002 03/15/2005
11.	ASSEMBLY FOR ELECTRICALLY CONNECTING A TEST COMPONENT TO A TESTING MACHINE FOR TESTING ELECTRICAL CIRCUITS ON THE TEST COMPONENT	10912785 7046022	08/06/2004 05/16/2006
12.	ASSEMBLY FOR ELECTRICALLY CONNECTING A TEST COMPONENT TO A	11433845	05/12/2006

	Title	Application No. / Publication No. / Patent No.	Filing Date / Issue Date
	TESTING MACHINE FOR TESTING ELECTRICAL CIRCUITS ON THE TEST COMPONENT	7385407	06/10/2008
13.	ASSEMBLY FOR ELECTRICALLY CONNECTING A TEST COMPONENT TO A TESTING MACHINE FOR TESTING ELECTRICAL CIRCUITS ON THE TEST COMPONENT	12045480 7511521	03/10/2008 03/10/2008
14.	CONNECTOR	29327294 D630166	11/03/2008 01/04/2011
15.	CONTACTOR ASSEMBLY FOR TESTING ELECTRICAL CIRCUITS	10197133 6853209	07/16/2002 02/08/2005
16.	CONTACTOR ASSEMBLY FOR TESTING ELECTRICAL CIRCUITS	10971897 7301358	10/22/2004 11/27/2007
17.	DIE CARRIER	10245934 6859057	09/17/2002 02/22/2005
18.	DIE CARRIER	11032846 7126363	01/10/2005 10/24/2006
19.	ELECTRONICS TESTER WITH A SIGNAL DISTRIBUTION BOARD AND A WAFER CHUCK HAVING DIFFERENT COEFFICIENTS OF THERMAL EXPANSION	12062988 7667475	04/04/2008 02/23/2010
20.	ELECTRONICS TESTER WITH A SIGNAL DISTRIBUTION BOARD AND A WAFER CHUCK HAVING DIFFERENT COEFFICIENTS OF THERMAL EXPANSION	12684051 7902846	01/07/2010 03/08/2011
21.	ELECTRONICS TESTER WITH A SIGNAL DISTRIBUTION BOARD AND A WAFER CHUCK HAVING DIFFERENT COEFFICIENTS OF THERMAL EXPANSION	13022803 8198909	02/08/2011 06/12/2012
22.	ENHANCEMENTS IN TESTING DEVICES ON BURN-IN BOARDS	09407659 6292415	09/28/1999 09/18/2001
23.	INTEGRATED FEEDTHROUGH MODULE	13168910 20110256774	06/24/2011
24.	INTERFACE ON AN ELECTRONICS CONNECTOR	29327293 D629760	11/03/2008 12/28/2010
25.	KINEMATIC COUPLING	09353123 6413113	07/14/1999 07/02/2002

	Title	Application No. / Publication No. / Patent No.	Filing Date / Issue Date
26.	METHOD AND SYSTEM FOR TESTING MEMORY PROGRAMMING DEVICES	08407103 5682472	03/17/1995 10/28/1997
27.	RELOADING OF DIE CARRIERS WITHOUT REMOVAL OF DIE CARRIERS FROM SOCKETS ON TEST BOARDS	10940288 7303929	09/13/2004 12/04/2007
28.	REUSABLE DIE CARRIER FOR BURN-IN AND BURN-IN PROCESS	08948696 6025732	05/06/1997 02/15/2000
29.	SEPARATE TEST ELECTRONICS AND BLOWER MODULES IN AN APPARATUS FOR TESTING AN INTEGRATED CIRCUIT	12437465 7969175	05/07/2009 06/28/2011
30.	SYSTEM FOR BURN-IN TESTING OF ELECTRONIC DEVICES	10184525 6815966	06/27/2002 11/09/2004
31.	SYSTEM FOR BURN-IN TESTING OF ELECTRONIC DEVICES	10917139 7063544	08/11/2004 06/20/2006
32.	SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE	11960453 7800382	12/19/2007 09/21/2010
33.	SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE	12411233 8030957	03/25/2009 10/04/2011
34.	SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE	12885373 8228085	09/17/2010 07/24/2012
35.	SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE	13223319 8947116	09/01/2011 02/03/2015
36.	SYSTEM FOR TESTING AN INTEGRATED CIRCUIT OF A DEVICE AND ITS METHOD OF USE	13554722 20120280704	07/20/2012
37.	SYSTEM FOR TESTING AND BURNING IN OF INTEGRATED CIRCUITS	11013855 7053644	12/15/2004 05/30/2006
38.	WAFER BURN-IN AND TEST EMPLOYING DETACHABLE CARTRIDGE	09884537 6556032	06/18/2001 04/29/2003
39.	WAFER BURN-IN AND TEST EMPLOYING DETACHABLE CARTRIDGE	10396170 7088117	03/24/2003 08/08/2006
40.	WAFER BURN-IN AND TEST EMPLOYING DETACHABLE CARTRIDGE	11276314 7541822	02/23/2006 06/02/2009

	Title	Application No. / Publication No. / Patent No.	Filing Date / Issue Date
41.	WAFER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD	09353121 6562636	07/14/1999 05/13/2003
42.	WAFER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD	09865957 6682945	05/25/2001 01/27/2004
43.	WAFER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD	10718825 7619428	11/21/2003 11/17/2009
44.	WAFER LEVEL BURN-IN AND ELECTRICAL TEST SYSTEM AND METHOD	12574447 7928754	10/06/2009 04/19/2011
45.	WAFER LEVEL BURN-IN AND TEST METHODS	09353116 6580283	07/14/1999 06/17/2003
46.	WAFER LEVEL BURN-IN AND TEST THERMAL CHUCK AND METHOD	09161323 6140616	09/25/1998 10/31/2000
47.	WAFER-LEVEL BURN-IN AND TEST CARTRIDGE	09353214 6340895	07/14/1999 01/22/2002
48.	PRINTED CIRCUIT BOARD LOADER/UNLOADER	07/526069 5093984	5/18/1990 3/10/1992
49.	REUSABLE DIE CARRIER FOR BURN-IN AND BURN-IN PROCESS	08/089752 5517125	7/9/1993 5/14/1996
50.	HIGH-DENSITY INTERCONNECT TECHNIQUE	08/161282 5429510	12/1/1993 7/4/1995