PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4052512

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
INPHI CORPORATION	08/04/2016

RECEIVING PARTY DATA

Name:	RAMBUS INC.
Street Address:	1050 ENTERPRISE WAY
Internal Address:	SUITE 700
City:	SUNNYVALE
State/Country:	CALIFORNIA
Postal Code:	94089

PROPERTY NUMBERS Total: 63

Property Type	Number
Application Number:	11195910
Application Number:	12267355
Application Number:	12611834
Application Number:	13653373
Application Number:	12505344
Application Number:	12563308
Application Number:	13558332
Application Number:	14178241
Application Number:	13782348
Application Number:	13791807
Application Number:	14527644
Application Number:	13587887
Application Number:	13359877
Application Number:	13619692
Application Number:	14228673
Application Number:	14665968
Application Number:	13768986
Application Number:	13786325
Application Number:	13787282

Property Type	Number
Application Number:	13787350
Application Number:	13445143
Application Number:	14228847
Application Number:	13460307
Application Number:	13783155
Application Number:	13791792
Application Number:	13791161
Application Number:	13797623
Application Number:	14593257
Application Number:	13530647
Application Number:	13778531
Application Number:	13797814
Application Number:	13797583
Application Number:	13791814
Application Number:	14473872
Application Number:	13791124
Application Number:	14194574
Application Number:	13909489
Application Number:	14245991
Application Number:	14242292
Application Number:	14194416
Application Number:	14175857
Application Number:	14316707
Application Number:	15137802
Application Number:	14951377
Application Number:	13797700
Application Number:	14923345
Application Number:	14181422
Application Number:	14975273
Application Number:	14536312
Application Number:	15137467
Application Number:	14444225
Application Number:	14798340
Application Number:	14861079
Application Number:	14989323
Application Number:	14706886
Application Number:	14884496
Application Number:	14883155

Property Type	Number
Application Number:	15156691
Application Number:	14885031
Application Number:	14963098
Application Number:	12132488
Application Number:	13620288
Application Number:	13797708

CORRESPONDENCE DATA

Fax Number: (650)493-6811

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: (650)493-9300
Email: shahn@wsgr.com
Correspondent Name: WILSON SONSINI GOODRICH & ROSATI
Address Line 1: 650 PAGE MILL ROAD
Address Line 4: PALO ALTO, CALIFORNIA 94304-1050

NAME OF SUBMITTER:	HEATHER ERWIN
SIGNATURE:	/Heather Erwin/
DATE SIGNED:	09/14/2016

Total Attachments: 13
source=Project Insignia - Master Patent Assignment (executed)#page1.tif
source=Project Insignia - Master Patent Assignment (executed)#page2.tif
source=Project Insignia - Master Patent Assignment (executed)#page3.tif
source=Project Insignia - Master Patent Assignment (executed)#page4.tif
source=Project Insignia - Master Patent Assignment (executed)#page5.tif
source=Project Insignia - Master Patent Assignment (executed)#page6.tif
source=Project Insignia - Master Patent Assignment (executed)#page7.tif
source=Project Insignia - Master Patent Assignment (executed)#page8.tif
source=Project Insignia - Master Patent Assignment (executed)#page9.tif
source=Project Insignia - Master Patent Assignment (executed)#page10.tif
source=Project Insignia - Master Patent Assignment (executed)#page11.tif
source=Project Insignia - Master Patent Assignment (executed)#page12.tif
source=Project Insignia - Master Patent Assignment (executed)#page13.tif

MASTER PATENT ASSIGNMENT

THIS MASTER PATENT ASSIGNMENT (this "Patent Assignment"), dated as of August 4, 2016, is entered into by and among, on the one hand, Rambus Inc., a Delaware corporation ("Buyer Parent") and Bell ID Singapore PTD Ltd, a Singapore private limited company ("Buyer," and together with Buyer Parent, the "Assignees") and, on the other hand, Inphi Corporation, a Delaware corporation ("Seller") and Inphi International Pte. Ltd., a Singapore private limited company ("Seller Sub" and together with Seller, the "Assignors"). All capitalized terms used but not defined herein shall have the meaning given in the Asset Purchase Agreement (as defined below).

WHEREAS, Assignors and Assignees have entered into an Asset Purchase Agreement, dated as of June 29, 2016 (the "Asset Purchase Agreement"), pursuant to which, among other things, Assignors have agreed to assign to Assignees the Assigned Patents (as defined below).

In consideration of the foregoing and the mutual covenants and agreements contained herein and in the Asset Purchase Agreement, and intending to be legally bound hereby, the parties agree as follows:

1. Assigned Patents. The term "Assigned Patents" means the issued patents, pending patent applications, and invention disclosures listed on Attachment 1.

2. Assignment. For good and valuable consideration, the receipt and adequacy of which is hereby acknowledged, Assignors hereby assign, transfer, sell and deliver to Assignees all of their right, title and interest throughout the world in and to the Assigned Patents, as well as any reexaminations, extensions, substitutions and reissues of any of the Assigned Patents, and all rights, claims and privileges pertaining to any of the Assigned Patents, including, without limitation, rights to the underlying inventions, the right to claim priority from the aforementioned patents and pending applications, the right to prosecute and maintain any of the Assigned Patents and the right to sue and recover damages for past, present and future infringement or other violation or impairment of any of the Assigned Patents.

3. No Warranties. This Patent Assignment provides no warranties of any kind, express or implied, with respect to the Assigned Patents, provided that the foregoing shall not be deemed or interpreted to modify or limit any representations or warranties with respect to the Assigned Patents provided in the Asset Purchase Agreement.

4. Further Assurances. Assignors will, without demanding any further consideration therefor, at the request and expense of Assignees (except for the value of the time of Assignor's employees), use their commercially reasonable efforts to do (and cause their Affiliates to do) all lawful acts that are necessary for recording and perfecting Assignees' rights to any Assigned Patents, including but not limited to (a) execution and acknowledgement of (and causing their Affiliates to execute and acknowledge) assignments and other instruments in a form reasonably required by Assignees for each Patent jurisdiction and (b) providing Assignees with reasonable assistance to secure Assignees' rights in any inventions within the Assigned Patents, in any and all applicable countries, including the disclosure to Assignees of all pertinent information and

data with respect thereto, the execution of all assignments, and all other instruments necessary in order to apply for, register, and in order to deliver, assign and convey to Assignees, their successors, assigns, and nominees the sole and exclusive rights, title, and interest in and to all such inventions within the Assigned Patents. In addition, and without limiting and not in lieu of the preceding sentence, Assignors shall complete, as soon as practicable after the Closing as agreed by the parties, any necessary re-execution and notarization, if any, and other procedural steps to be taken by Assignors to render Patent assignments suitable for filing in each jurisdiction in which such Assigned Patents have been filed or issued. Assignors represent to Assignees, their successors and assigns, that Assignors have not and shall not execute any writing or do any act whatsoever conflicting with this Patent Assignment.

5. Successors and Assigns. This Patent Assignment will be binding upon, inure to the benefit of, and be enforceable by, the parties and their respective permitted successors and assigns.

6. Severability. Whenever possible, each provision or portion of any provision of this Patent Assignment shall be interpreted in such manner as to be effective and valid under applicable law, but if any provision or portion of any provision of this Patent Assignment is held to be invalid, illegal or unenforceable in any respect under any applicable law or rule in any jurisdiction, such invalidity, illegality or unenforceability shall not affect any other provision or portion of any provision in such jurisdiction, and this Patent Assignment shall be reformed, construed and enforced in such jurisdiction as if such invalid, illegal or unenforceable provision or portion of any provision had never been contained herein.

7. Governing Law. This Patent Assignment shall be governed in all respects by the internal laws of the State of California as applied to agreements entered into among California residents to be performed entirely within California, without regard to principles of conflict of laws. With respect to any disputes arising out of or related to this Patent Assignment, the parties consent to the exclusive jurisdiction of, and venue in, the state courts in Santa Clara County in the State of California (or in the event of exclusive federal jurisdiction, the courts of the Northern District of California). Each of the parties hereto irrevocably and unconditionally waives any objection to the laying of venue of any suit or proceeding arising out of or relating to this Patent Assignment or the transactions contemplated hereby in the state courts in Santa Clara County in the State of California (or in the event of exclusive federal jurisdiction, the courts of the Northern District of California) and irrevocably and unconditionally waives and agrees not to plead or claim in any such court that any such suit or proceeding in any such court has been brought in an inconvenient forum. Each of the parties hereto further agrees, (a) to the extent such party is not otherwise subject to service of process in the State of California, to appoint and maintain an agent in the State of California as such party's agent for acceptance of legal process, and (b) that service of process may also be made on such party at its respective address set forth in **Section 9.1** of the Asset Purchase Agreement by prepaid certified mail with a proof of mailing receipt validated by U.S. Postal Service constituting evidence of valid service. Service made pursuant to (a) or (b) above shall have the same legal force and effect as if served upon such party personally with the State of California.

8. Counterparts. This Patent Assignment may be executed in two or more counterparts (including by facsimile or other electronic transmission), all of which shall be

considered one and the same instrument and shall become effective when one or more counterparts have been signed by each of the parties and delivered to the other party.

9. Precedence. Those patent assignments executed and delivered to Assignees purporting to assign any Assigned Patents in a particular Patent jurisdiction (the "Jurisdiction Specific Patent Assignment(s)") are solely for registration or recordation purposes. The Asset Purchase Agreement shall take precedence over this Patent Assignment and/or any Jurisdiction Specific Patent Assignment; and this Patent Assignment shall take precedence over any Jurisdiction Specific Patent Assignment. In the event of any difference, discrepancy or conflict between any term or condition in the Asset Purchase Agreement and any term or condition in this Patent Assignment or in any Jurisdiction Specific Patent Assignment, the terms and conditions of the Asset Purchase Agreement shall prevail and govern. In the event of any difference, discrepancy or conflict between any term or condition in this Patent Assignment and any term or condition in any Jurisdiction Specific Patent Assignment, the terms and conditions of this Patent Assignment shall prevail and govern.

[The remainder of this page is intentionally left blank.]

Witness Signature: Bill

Witness Name (print): Bill Krause

ASSIGNEES:

RAMBUS INC.

By: _____
Name: Joe Ennis
Title: SVP, General Counsel

BELL ID SINGAPORE PTD LTD

By: _____
Name: Joe Ennis
Title: SVP, General Counsel

IN WITNESS WHEREOF, Assignors and Assignees have caused this Patent Assignment to be executed as of the date first written above by their respective officers thereunto duly authorized.

Witness Signature: Parul Dutt

Witness Name (print):

PARUL DUTT

ASSIGNORS:

INPHI CORPORATION

By: _____

Name: Richard Ogawa

Title: General Counsel

INPHI INTERNATIONAL PTE. LTD

By: _____

Name: Richard Ogawa

Title: Director

ATTACHMENT 1

ASSIGNED PATENTS

ISSUED FOREIGN PATENTS

N/A

PENDING FOREIGN PATENT APPLICATIONS

Inphi #	Application #	Status	Country	Title	Inventor
0117-CN	201320685722.6	Pending	China	Memory Interface Devices and Integrated Circuit Devices	David Wang
0117-DE	202013009597.0	Pending	Germany	Replacement of a Faulty Memory Cell with a Spare Cell for a Memory Circuit	David Wang

ISSUED US PATENTS

Inphi #	Application #	Patent #	Status	Country	Title	Inventor
0077-US	11/195,910	7,307,863	Issued	USA	Programmable strength output buffer for RDIMM address register	Raghavan, Gopal, Srivastava, Nikhil, Yen, Jeffery
0089-US	12/267,355	8,898,368	Issued	USA	Redriven/Retimed Registered Dual Inline Memory Module	Chris Haywood, Gopal Raghavan
0091-US	12/611,834	8,316,175	Issued	USA	High Throughput Flash Memory System	Francis Ho
0091-US2	13/653,373	9,053,009	Issued	USA	High Throughput Flash	Francis Ho

Inphi #	Application #	Patent #	Status	Country	Title	Inventor
					Memory System	
0092-US	12/505,344	8,233,304	Issued	USA	High Speed Memory Module	Chau Xu
0114-US	12/563,308	8,275,936	Issued	USA	Load reduction technique and DIMM DRAM striping	Chris Haywood
0115-US	13/558,332	8,687,451	Issued	USA	Power Management in Semiconductor Memory System	David Wang
0115-US2	14/178,241	8,879,348	Issued	USA	Power Management in Semiconductor Memory System	David Wang
0117-US2	13/782,348	8,971,094	Issued	USA	Replacement of a Faulty Memory Cell with a Spare Cell for a Memory Circuit	David Wang
0117-US3	13/791,807	8,902,638	Issued	USA	Replacement of a Faulty Memory Cell with a Spare Cell for a Memory Circuit	David Wang
0117-US4	14/527,644	9,001,567	Issued	USA	Replacement of a Faulty Memory Cell with a Spare Cell for a Memory Circuit	David Wang
0118-US	13/587,887	9,158,726	Issued	USA	Self Terminated Dynamic Random Access Memory	Chao Xu
0119-US	13/359,877	8,694,721	Issued	USA	Memory Buffer with one or more auxilliary ports	Chris Haywood
0119-US2	13/619,692	8,880,790	Issued	USA	Methods and Apparatus for Transferring Data Between Memory Modules	Chris Haywood

Inphi #	Application #	Patent #	Status	Country	Title	Inventor
0119-US3	14/228,673	8,990,488	Issued	USA	Memory Buffer With One or More Auxiliary Interfaces	Chris Haywood
0119-US4	14/665,968	9,323,458	Issued	USA	Memory Buffer With One or More Auxiliary Interfaces	Chris Haywood
0120-US	13/768,986	8,949,473	Issued	USA	Hybrid Memory Blade	Christopher Haywood, Chao Xu, Ford Tamer
0122-US	13/786,325	9,239,355	Issued	USA	Memory Test Sequencer	Andrew Burstein, Larry Kan, Chien-Hsin Lee, Satish Bamdhamravuri, David Wang
0123-US	13/787,282	9,069,717	Issued	USA	Memory Parametric Improvements (Interface)	David Wang, Andrew Burstein
0123-US2	13/787,350	9,230,635	Issued	USA	Memory Parametric Improvements (DRAM)	David Wang, Andrew Burstein
0127-US	13/445,143	8,694,857	Issued	USA	Error Correction Techniques Using Memory Buffer	David Wang, Christopher Haywood
0127-US2	14/228,847	9,015,558	Issued	USA	Systems and Methods For Error Detection And Correction In A Memory Module Which Includes A Memory Buffer	David Wang, Christopher Haywood
0128-US	13/460,307	8,711,647	Issued	USA	New Dram Refresh Scheme Proposal	David Wang
0130-US	13/783,155	9,230,620	Issued	USA	Distributed Hardware Tree Search Methods and Apparatus for	Chien-Hsin Lee

Inphi #	Application #	Patent #	Status	Country	Title	Inventor
					Memory Data Replacement	
0130-US2	13/791,792	9,099,165	Issued	USA	Single Chip Mixed Memory for Dynamic Replacement of DRAM BAD Cell	Chien-Hsin Lee
0132-US	13/791,161	9,195,607	Issued	USA	Content Matching Using a Multi-Hash Function for Replacement of a Faulty Memory Cell	Nirmal Saxena, Javier Villagomez
0135-US	13/797,623	8,966,327	Issued	USA	Protocol Checking Logic Circuit for Memory System Reliability	David Wang
0135-US2	14/593,257	9,317,366	Issued	USA	Protocol Checking Logic Circuit for Memory System Reliability	David Wang
0136-US	13/530,647	9,196,314	Issued	USA	Extended-Height Dimm	Victor Cai
0137-US	13/778,531	8,885,426	Issued	USA	Compression of Content Entries in Storage for Replacing Faulty Memory Cells	Andrew Burstein, Nirmal Saxena, Javier Villagomez
0138-US	13/797,814	8,854,908	Issued	USA	System and Method for Memory Access in Server Communications	Andrew Burstein, David Wang
0139-US	13/797,583	8,996,960	Issued	USA	Vertical Error Correction Code for DRAM Memory	Nirmal Saxena, David Wang, Hamid Rategh, Lawrence Tse

Inphi #	Application #	Patent #	Status	Country	Title	Inventor
0140-US	13/791,814	8,861,277	Issued	USA	Method of Using Non-Volatile Memories for On-Dimm Memory Address List Storage	Hamid Rategh, David Wang, Lawrence Tse
0140-US2	14/473,872	9,240,248	Issued	USA	Method of Using Non-Volatile Memories for On-Dimm Memory Address List Storage	Hamid Rategh, David Wang, Lawrence Tse
0144-US	13/791,124	9,170,878	Issued	USA	Memory Buffer with Data Scrambling and Error Correction	Christopher Haywood, David Wang
0162-US2	14/194,574	9,250,831	Issued	USA	Isolated Shared Memory Architecture (isMA)	Nirmal Saxena, Sreenivas Krishnan, David Wang
0169-US	13/909,489	8,990,491	Issued	USA	Eye Scan for Asymmetric Shaped Communication Signal	Chao Xu
0206-US	14/245,991	9,123,441	Issued	USA	A Backward Compatible Dynamic Random Access Memory Device and Method of Testing Therefor	David Wang
0128-US2	14/242,292	9,142,279	Issued	USA	DRAM Refresh Method and System	David Wang
0160-US	14/194,416	9,348,539	Issued	USA	Memory Centric Computing	Nirmal Saxena, David Wang, Christopher Haywood, Eric McDonald, Chao Xu
0171-US	14/175,857	9,349,433	Issued	USA	Hidden Refresh of Weak Memory Storage Cells In Semiconductor	David Wang

Inphi #	Application #	Patent #	Status	Country	Title	Inventor
0205-US	14/316,707	9,348,705	Issued	USA	Memory Memory Controller System with Non-Volatile Backup Storage	Shih-ho Wu, Chris Haywood

PENDING US PATENT APPLICATIONS

Inphi #	Application #	Status	Country	Title	Inventor
0119-US5	15/137,802	Pending	USA	Memory Buffer With One or More Auxiliary Interfaces	Chris Haywood
0136-US2	14/951,377	Pending	USA	Extended-Height Dimm	Victor Cai
0141-US	13/797,700	Pending	USA	System and Method for Memory Access in Server Communications	Christopher Haywood
0144-US2	14/923,345	Pending	USA	Memory Buffer with Data Scrambling and Error Correction	Christopher Haywood, David Wang
0158-US	14/181,422	Pending	USA	Alternate Access to DRAM Data Using Cycle Stealing	Christopher Haywood
0162-US3	14/975,273	Pending	USA	Isolated Shared Memory Architecture (isMA)	Nirmal Saxena, Sreenivas Krishnan, David Wang
0200-US	14/536,312	Pending	USA	Near-Memory Compute Module	David Wang, Nirmal Saxena
0205-US2	15/137,467	Pending	USA	Memory Controller System with Non-Volatile Backup Storage	Shih-ho Wu, Chris Haywood

Inphi #	Application #	Status	Country	Title	Inventor
0223-US	14/444,225	Pending	USA	Memory Controller Systems With Nonvolatile Memory For Storing Operating Parameters	Shih-ho Wu, Christopher Haywood
0380-US	14/798,340	Pending	USA	Dynamic Update Technique for the DB A0 Phase Interpolator (DB AO Phase Interpolator Update Circuit)	Cosmin Iorga
0382-US	14/861,079	Pending	USA	Method and Circuit for Ensuring Delay Adjustment Monotonicity in a Delay Line for DB Gen2 Product	Cosmin Iorga
0383-US	14/989,323	Pending	USA	Phase Interpolator Device Using Dynamic Stop and Phase Code Update and Method Therefor	Cosmin Iorga
0420-US	14/706,886	Pending	USA	Method and System using Memory Channel Load Sharing	Chris Haywood
0429-US	14/884,496	Pending	USA	Hybrid Memory Module with Improved Inter-Memory Data Transmission Path	Aws Shallal
0431-US	14/883,155	Pending	USA	High-Throughput Low Latency Hybrid Memory Module	Aws Shallal, Michael Miller, Stephen Horn
0431-US2	15/156,691	Pending	USA	High-Throughput Low Latency Hybrid Memory Module	Aws Shallal, Michael Miller, Stephen Horn
0440-US	14/885,031	Pending	USA	Buffering Device with Status Communication Method for Memory Controller	David Wang
0445-US	14/963,098	Pending	USA	Self-Describing Page Data Format (NAND Header)	Aws Shallal

ABANDONED US PATENT APPLICATIONS

Inphi #	Application #	Status	Country	Title	Inventor
0113-US	12/132,488	Abandoned	USA	Method and apparatus for Testing Write-only registers.	Chris Haywood
0117-US	13/620,288	Abandoned	USA	Replacement of Faulty Memory Cell with a Spare Cell for a Memory Circuit	David Wang
0131-US	13/797,708	Abandoned	USA	Memory Centric Computing	David Wang, Nirmal Saxena, Christopher Haywood, Eric McDonald