

PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
INTEGRATED DEVICE TECHNOLOGY INC.		10/05/2016
RECEIVING PARTY DATA		
Name:	SK HYNIX INC.	
Street Address:	2091, GYEONGCHUNG-DAERO, BUBAL-EUB, ICHEON-SI	
City:	GYEONGGI-DO	
State/Country:	KOREA, REPUBLIC OF	
PROPERTY NUMBERS Total: 14		
Property Type	Number	
Patent Number:	6775717	
Patent Number:	7587439	
Patent Number:	7061294	
Patent Number:	6867630	
Patent Number:	6865638	
Patent Number:	6664838	
Patent Number:	6222793	
Patent Number:	6944070	
Patent Number:	7203126	
Patent Number:	6856558	
Patent Number:	7359275	
Patent Number:	7386774	
Patent Number:	7710789	
Patent Number:	7363436	
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NAME OF SUBMITTER:	MYUNG SOO KIM
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DATE SIGNED:	10/24/2016
Total Attachments: 2 source=2016-10-05 Patent Assignment#page1.tif source=2016-10-05 Patent Assignment#page2.tif	

PATENT ASSIGNMENT

WHEREAS, **Integrated Device Technology, Inc.**, ("Seller") is the owner of certain United States and/or foreign patents and/or patent applications listed in Exhibit A annexed hereto (collectively referred to as the "**Patents**"); and

WHEREAS, **SK hynix Inc.**, ("Purchaser") is desirous of acquiring Seller's right, title and interest in, to and under the said Patents (and all foreign counterparts and related foreign patents).

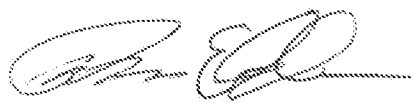
Now, Therefore,

For good and valuable consideration, the receipt of which is hereby acknowledged, Seller hereby sells, assigns, transfers and sets over to Purchaser the Patents aforesaid, and any inventions claimed in said Patents, any reissue or reissues of said Patents already granted and which may be granted, any certificates of reexamination already granted and which may be granted the same to be held and enjoyed by Purchaser as fully and entirely as the same would have been held and enjoyed by Seller, if this assignment had not been made; together with all claims for damages by reason of past, current, and future infringement and/or provisional rights under said Patents, with the right to sue for, and collect the same for its own use and behalf, and for the use and behalf of its successors, assigns or other legal representatives.

And, Seller, hereby authorizes and requests the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patents in the name of the Purchaser.

In Witness Whereof, Seller has executed this Assignment by its duly authorized representative.

Integrated Device Technology, Inc.

By: 

Name: Bruce Elder

Title: Director, IP and Licensing

Date: 5 Oct 2016

Exhibit A
Assigned Patents

Country	Patent No.	Title
US	6,775,717	Method and apparatus for reducing latency due to set up time between DMA transfers
US	7,587,439	Method and apparatus for generating a random bit stream in true random number generator fashion
US	7,061,294	Clock processing logic and method for determining clock signal characteristics in reference voltage and temperature varying environments
US	6,867,630	Clock processing logic and method for determining clock signal characteristics in reference voltage and temperature varying environments
US	6,865,638	Apparatus and method for transferring multi-byte words in a fly-by DMA operation
US	6,664,838	Apparatus and method for generating a compensated percent-of-clock period delay signal
US	6,222,793	Memory devices having a restore start address counter
US	6,944,070	Integrated circuit devices having high precision digital delay lines therein
US	7,203,126	Integrated circuit systems and devices having high precision digital delay lines therein
US	6,856,558	Integrated circuit devices having high precision digital delay lines therein
US	7,359,275	Reduced size dual-port SRAM cell
US	7,386,774	Memory unit with controller managing memory access through JTAG and CPU interfaces
US	7,710,789	Synchronous address and data multiplexed mode for SRAM
US	7,363,436	Collision detection in a multi-port memory system