PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4119633

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
MICRON TECHNOLOGY, INC.	09/08/2016

RECEIVING PARTY DATA

Name:	INTEL CORPORATION
Street Address:	2200 MISSION COLLEGE BLVD.
City:	SANTA CLARA
State/Country:	CALIFORNIA
Postal Code:	95054

PROPERTY NUMBERS Total: 6

Property Type	Number
Application Number:	11810550
Application Number:	12151265
Application Number:	11860949
Application Number:	12647317
Application Number:	12636896
Application Number:	12629992

CORRESPONDENCE DATA

Fax Number: (612)677-3572

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 6122369923
Email: jkathman@cpaglobal.com
Correspondent Name: JENNY KATHMAN
Address Line 1: C/O CPA GLOBAL
Address Line 2: 900 2ND AVENUE SOUTH, SUITE 600
Address Line 4: MINNEAPOLIS, MINNESOTA 55402

ATTORNEY DOCKET NUMBER:	MICRON-INTEL ASSIGNMENT
NAME OF SUBMITTER:	JENNY KATHMAN
SIGNATURE:	/JENNY KATHMAN/
DATE SIGNED:	10/28/2016

Total Attachments: 5
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Micron-Intel Assignment

Micron Technology, Inc., a Delaware corporation, with an office at 8000 S. Federal Way, Boise, ID 83707 (hereinafter "Micron") and Intel Corporation, a Delaware corporation, with an office at 2200 Mission College Blvd., Santa Clara, CA 95052 (hereinafter "Intel") executed an Amended and Restated Technology License Agreement on April 6, 2012 (hereinafter "the TLA"), and an Amended and Restated Product Designs Development Agreement on April 6, 2012 (hereinafter "the PDA"). Additionally, Micron and Intel executed an Amended and Restated Designated Technology Joint Development Program Agreement on May 8, 2012 (hereinafter "the DTJDPA").

In accordance with the TLA, the PDA, and the DTJDPA, Micron and Intel periodically meet to select Pooled Inventions according to a Draft (capitalized terms in this sentence and the remainder of this paragraph having, for each referenced agreement, the meaning ascribed to them in that agreement). In accordance with the TLA, the PDA, and the DTJDPA, the Patent Rights in the Pooled Inventions allocated to Intel as a result of each Draft that occurred under the applicable agreement are to be solely and exclusively owned by Intel.

Intel has filed the patent applications listed in Exhibit A (annexed hereto) (collectively referred to as the "Intel Applications") which are Patent Rights that have been allocated to Intel as a result of Drafts that have occurred.

For good and valuable consideration, the receipt of which is hereby acknowledged, to the extent not already assigned to Intel under the TLA, the PDA, the DTJDPA or another instrument or agreement, Micron hereby assigns to Intel all right, title and interest Micron owns or controls, in the Intel Applications and any and all divisionals, continuations, reissues, reexaminations, extensions, foreign counterparts or equivalents of any of the Intel Applications, wherever and whenever existing.

Micron and Intel agree that nothing in this Assignment shall in any way be interpreted to modify, replace or supersede, whether by implication, estoppel or otherwise, the TLA, the PDA or the DTJDPA.

In Witness Whereof, Micron, by its duly authorized representative, has executed this Micron-Intel Assignment.

Date: Sept. 8, 2016 By: Joel Popper
Printed/Typed Name

Title: Vice President, Legal Affairs, General Counsel and Corporate Secretary

Signature

STATE OF IDAHO)
) ss.
COUNTY OF Ada)

On this 8th day of Sept, 2016 personally appeared before me, Joel Popper, to me known and known to me to be the person aforesaid, who duly acknowledged the signing of the foregoing instrument to be his or her voluntary act and deed, and as _____ of _____ did execute the same for the uses and purposes therein set forth.

WITNESS my hand and official seal.
(Seal)

Notary Public in and for the state of Idaho

Kathlene R. Jones
Print Name

My appointment expires on: April 3, 2019

PATENT
REEL: 040163 FRAME: 0165

ACCEPTED:

Date: 7/30/16 By: Jeff Draeger
Printed/Typed Name

Title: Vice President, Intel Law and Policy Group

LEGAL OK

Signature

PATENT
REEL: 040163 FRAME: 0166

EXHIBIT A

First Filed Application Title	Disclosure Number	Intel Case Reference	Filing Date	Serial Number	Publication Number	Patent Number	Country	Inventors
Methods and Apparatuses for Refreshing Non-volatile Memory	55031	P25441	06/06/2007	11/810,550	US 2008-0304327 A1	7,535,787	US	Ruby, Paul D.; Elmhurst, Daniel R.; Moschiano, Violante
Method and Apparatuses for Programming Flash Memory Using Modulating Pulses	2006-1076	P25442	05/05/2008	12/151,265	US 2009-0273981 A1	7,848,158	US	Santin, Giovanni; Moschiano, Violante; Vali, Tommaso; Di Francesco, Walter
Device, System, and Method of Bit Line Selection of a Flash Memory	2007-0282	P26274	09/25/2007	11/860,949	US 2009-0080253 A1	7,639,534	US	Santin, Giovanni; Moschiano, Violante; Vali, Tommaso; Incarnati, Michele
Technique to Reduce FG-FG Interference in Multi-bit Flash NAND Memory in Case of Adjacent Pages not Fully Programmed	2009-0233	P32712	12/24/2009	12/647,317	US 2011-0157980 A1	8,194,448	US	Moschiano, Violante; Santin, Giovanni
Source Bias Shift for Multilevel Memories	2008-0590	P32715	12/14/2009	12/636,896	US 2011-0141822 A1	8,248,862	US	Di Iorio, Ercole Rosario; Marotta, Giulio Giuseppe; Tiburzi, Marco Domenico; Kalavade, Pranav
Flash Memory Having a Floating Gate in the Shape of a Curved Section	2008-0578	P32714	12/03/2009	12/629,992	US-2011-0133266-A1	n/a	US	Parat, Krishna K.; Tang, Sanh D.; Liu, Haitao

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RECORDED: 10/28/2016

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REEL: 040163 FRAME: 0168

First Filed Application Title	Disclosure Number	Intel Case Reference	Filing Date	Serial Number	Publication Number	Patent Number	Country	Inventors
Flash Memory Having a Floating Gate in the Shape of a Curved Section	2008-0578	P32714CN	09/29/2010	201010507045.X	102087972A	201010507045.X	CN	Parat, Krishna K.; Tang, Sanh D.; Liu, Haitao
Flash Memory Having a Floating Gate in the Shape of a Curved Section	2008-0578	P32714DE	09/24/2010	10 2010 046 506.2	102010046506A1		DE	Parat, Krishna K.; Tang, Sanh D.; Liu, Haitao
Flash Memory Having a Floating Gate in the Shape of a Curved Section	2008-0578	P32714TW	09/23/2010	099132163	201143033		TW	Parat, Krishna K.; Tang, Sanh D.; Liu, Haitao
Flash Memory Having a Floating Gate in the Shape of a Curved Section	2008-0578	P32714GB	09/22/2010	1015957.2	2475942 A	GB2475942	GB	Parat, Krishna K.; Tang, Sanh D.; Liu, Haitao