PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4136747

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
MICRON TECHNOLOGY, INC.	09/26/2008

RECEIVING PARTY DATA

Name:	APTINA IMAGING CORPORATION
Street Address:	C/O CITICO TRUSTEES (CAYMAN) LIMITED
Internal Address:	REGATTA OFFICE PARK, WEST BAY ROAD
City:	GRAND CAYMAN
State/Country:	CAYMAN ISLANDS
Postal Code:	Y1-1205

PROPERTY NUMBERS Total: 36

Property Type	Number
Patent Number:	6277673
Patent Number:	6830961
Patent Number:	7084490
Patent Number:	6445061
Patent Number:	6271580
Patent Number:	6130474
Patent Number:	6958528
Patent Number:	6562182
Patent Number:	6776871
Patent Number:	6517668
Patent Number:	6320246
Patent Number:	6344364
Patent Number:	6781365
Patent Number:	6870380
Patent Number:	7046029
Patent Number:	6646456
Patent Number:	6518181
Patent Number:	6765398
Patent Number:	6897512

Property Type	Number
Patent Number:	6972452
Patent Number:	7067861
Patent Number:	7094657
Patent Number:	7049191
Patent Number:	6720215
Patent Number:	6916699
Patent Number:	6479340
Patent Number:	6607975
Patent Number:	6489194
Patent Number:	6808976
Patent Number:	6468854
Patent Number:	6924188
Patent Number:	7041550
Patent Number:	6472264
Patent Number:	6852622
Patent Number:	6756301
Patent Number:	6602785

CORRESPONDENCE DATA

Fax Number: (602)244-3169

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 6022443574
Email: patents@onsemi.com
Correspondent Name: SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC
Address Line 1: 5005 E. MCDOWELL ROAD
Address Line 2: MAILDROP A700
Address Line 4: PHOENIX, ARIZONA 85008

ATTORNEY DOCKET NUMBER:	APT_MICRONAPTINA
NAME OF SUBMITTER:	SHARRON CASTILLO
SIGNATURE:	/Sharron Castillo/
DATE SIGNED:	11/10/2016

Total Attachments: 17
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source=APT_20161110_Assignment_MicronAptina#page3.tif
source=APT_20161110_Assignment_MicronAptina#page4.tif
source=APT_20161110_Assignment_MicronAptina#page5.tif
source=APT_20161110_Assignment_MicronAptina#page6.tif
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PATENT ASSIGNMENT AGREEMENT

1. Definitions

(a) "Agreement" shall mean this Patent Assignment Agreement.

(b) "Assignee" shall mean **Aptina Imaging Corporation**, a Cayman Islands corporation with offices at c/o Citco Trustees (Cayman) Limited, Regatta Office Park, West Bay Road, Grand Cayman, Y1-1205, Cayman Islands.

(c) "Assignor" shall mean **Micron Technology, Inc.**, a Delaware corporation with offices at 8000 South Federal Way, Boise, ID 83707.

(d) "Effective Date" shall mean October 3, 2008.

(e) [redacted]

(f) [redacted]

(g) "Imaging Patents" shall mean those patents identified in ATTACHMENT "A" hereto, including, without limitation, all divisions, continuations, continuations-in-part, reissues, reexaminations, and all foreign counterparts thereof, and which may issue thereon or in connection therewith after the Effective Date of this Agreement.

(h) "Imaging Patent Applications" shall mean those filed patent applications identified in ATTACHMENT "B" hereto, including, without limitation, all patents, divisions, continuations, continuations-in-part, reissues, reexaminations, and all foreign counterparts which may issue thereon or in connection therewith after the Effective Date of this Agreement.

(i) "Semiconductor Patents" shall mean those patents identified in ATTACHMENT "D" hereto, including, without limitation, all divisions, continuations, continuations-in-part, reissues, reexaminations, and all foreign counterparts thereof, and which may issue thereon or in connection therewith after the Effective Date of this Agreement.

(j) "Semiconductor Patent Applications" shall mean those filed patent applications identified in ATTACHMENT "E" hereto, including, without limitation, all patents, divisions, continuations, continuations-in-part, reissues, reexaminations, and all foreign counterparts which may issue thereon or in connection therewith after the Effective Date of this Agreement.

(k) [redacted].

2. [redacted]

(a) Subject to the terms and conditions of this Agreement, and subject to the rights of others existing as of the Effective Date of this Agreement if any, Assignor, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, hereby sells, assigns, and transfers to Assignee its entire right, title and interest in and to the Imaging Patents, including all rights to causes of action and remedies related thereto (including the right to sue for past, present or future infringement of rights related to the foregoing and the right to collect damages therefor). Assignor hereby authorizes and requests the Commissioner of Patents of the United States, and any other official of the United States and any country foreign to the United States whose duty it is to issue or record patents, to issue the Imaging Patents to Assignee and to record assignment of the Imaging Patents to Assignee.

(b) Subject to the terms and conditions of this Agreement, and subject to the rights of others existing as of the Effective Date of this Agreement if any, Assignor, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, hereby sells, assigns, and transfers to Assignee its entire right, title and interest in and to the Intellectual Property rights in the Imaging Patent Applications. Assignor hereby authorizes and requests the Commissioner of Patents of the United States, and any other official of the United States and any country foreign to the United States whose duty it is to issue or record patents, to record assignment of the Imaging Patent Applications to Assignee.

(c) [redacted].

(d) Subject to the terms and conditions of this Agreement, and subject to the rights of others existing as of the Effective Date of this Agreement if any, and subject further to the restrictions on the Semiconductor Patents set out below, Assignor, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, hereby sells, assigns, and transfers to Assignee its entire right, title and interest in and to the Semiconductor Patents, including all rights to causes of action and remedies related thereto (including the right to sue for past, present or future infringement of rights related to the foregoing and the right to collect damages therefor). Assignor hereby authorizes and requests the Commissioner of Patents of the United States, and any other official of the United States and any country foreign to the United States whose duty it is to issue or record patents, to issue the Semiconductor Patents to Assignee and to record assignment of the Semiconductor Patents to Assignee.

(e) Subject to the terms and conditions of this Agreement, and subject to the rights of others existing as of the Effective Date of this Agreement if any, [redacted], Assignor, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, hereby sells, assigns, and transfers to Assignee its entire right, title and interest in and to the Intellectual Property rights in the Semiconductor Patent Applications. Assignor hereby authorizes and requests the Commissioner of Patents of the United States, and any other official of the United States and any country foreign to the United States whose duty it is to issue or record patents, to record assignment of the Semiconductor Patent Applications to Assignee.

(f) [redacted]

[redacted]

[redacted]

3 [redacted]

[redacted]

4. [redacted]

[redacted]

5. [redacted]

[redacted]

[redacted]

6. [redacted]

[redacted]

7. General

This Agreement shall be effective as of the Effective Date hereof and shall be binding on the respective heirs, assigns, representatives, and successors of Assignor and of Assignee.

[the rest of this page intentionally left blank]

Agreed to by:

Micron Technology, Inc.

Signed: _____

Date: 9/26/08, 2008

Notarization
State of Idaho
County of Ada

On 9/26/08 (date), before me, Paula R. Spang (notary name), personally appeared the above-named Steven R. Appleton who executed this Assignment in my presence and acknowledged to me that he did so of his own free will and in his authorized capacity for the purposes set forth herein.

Signed: _____

My commission expires: 8/12/11

REVIEWED
MTI LEGAL
C.S

PAULA R. SPANG NOTARY PUBLIC STATE OF IDAHO

Agreed to by:

Aptina Imaging Corporation

Signed: _____

Date: 9/26/08, 2008

Notarization
State of Idaho
County of Ada

On 9/26/08 (date), before me, Paula R. Spang (notary name), personally appeared the above-named Thomas L. Laws, Jr. who executed this Assignment in my presence and acknowledged to me that he did so of his own free will and in his authorized capacity for the purposes set forth herein.

Signed: _____

My commission expires: 8/12/11

PAULA R. SPANG NOTARY PUBLIC STATE OF IDAHO

[Signature page to the Patent Assignment Agreement]

ATTACHMENT "A"

[redacted]

ATTACHMENT "B"

ATTACHMENT "C"

ATTACHMENT "D"

ATTACHMENT "E"

ATTACHMENT "D"

SEMICONDUCTOR PATENTS

Aptina Semiconductor Issued

Oct-03-2008

PATENT NUMBER	FILE NUMBER	TITLE	COUNTRY NAME	ISSUE DATE
0444811	1998-1290.00/KR	METHOD OF FORMING A CONDUCTIVE SILICIDE LAYER ON A SILICON COMPRISING SUBSTRATE AND METHOD OF FORMING A CONDUCTIVE SILICIDE CONTACT	Republic of Korea	Aug 9, 2004
100 84 994	1998-1290.00/DE	METHOD OF FORMING A CONDUCTIVE SILICIDE LAYER ON A SILICON COMPRISING SUBSTRATE AND METHOD OF FORMING A CONDUCTIVE SILICIDE CONTACT	Germany	Oct 19, 2006
2374980	1998-1290.00/GB	METHOD OF FORMING A CONDUCTIVE SILICIDE LAYER ON A SILICON COMPRISING SUBSTRATE AND METHOD OF FORMING A CONDUCTIVE SILICIDE CONTACT	United Kingdom	Apr 7, 2004
4068669	1998-1290.00/JP	METHOD OF FORMING A CONDUCTIVE SILICIDE LAYER ON A SILICON COMPRISING SUBSTRATE AND METHOD OF FORMING A CONDUCTIVE SILICIDE CONTACT	Japan	Dec 28, 2007
5472904	1994-0140.00/US	THERMAL TRENCH ISOLATION	United States of America	Dec 5, 1995
5578873	1993-0479.01/US	METHOD OF MAKING OHMIC CONTACT BETWEEN A THIN FILM POLYSILICON LAYER AND A SUBSEQUENTLY PROVIDED CONDUCTIVE LAYER AND INTEGRATED CIRCUITRY	United States of America	Nov 26, 1996
5681778	1992-0488.00/US	SEMICONDUCTOR PROCESSING METHOD OF FORMING A BURIED CONTACT AND CONDUCTIVE LINE (AS AMENDED)	United States of America	Oct 28, 1997
5729055	1993-0479.04/US	METHOD OF MAKING OHMIC CONTACT BETWEEN A THIN FILM POLYSILICON LAYER AND A SUBSEQUENTLY PROVIDED CONDUCTIVE LAYER AND INTEGRATED CIRCUITRY	United States of America	Mar 17, 1998
5773346	1992-0415.00/US	SEMICONDUCTOR PROCESSING METHOD OF FORMING A BURIED	United States of America	Jun 30, 1998

Aptina Semiconductor Issued

PATENT NUMBER	FILE NUMBER	TITLE	COUNTRY NAME	ISSUE DATE
		CONTACT		
5888881	1994-0140.01/US	METHOD OF TRENCH ISOLATION DURING THE FORMATION OF A SEMICONDUCTOR DEVICE	United States of America	Mar 30, 1999
5907769	1996-0243.00/US	LEADS UNDER CHIP/CONVENTIONAL IC PACKAGE ASSEMBLY	United States of America	May 25, 1999
5909631	1993-0479.03/US	METHOD OF MAKING OHMIC CONTACT BETWEEN A THIN FILM POLYSILICON LAYER AND A SUBSEQUENTLY PROVIDED CONDUCTIVE LAYER AND INTEGRATED CIRCUITRY	United States of America	Jun 1, 1999
5930662	1993-0479.02/US	METHOD OF MAKING OHMIC CONTACT BETWEEN A THIN FILM POLYSILICON LAYER AND A SUBSEQUENTLY PROVIDED CONDUCTIVE LAYER AND INTEGRATED CIRCUITRY	United States of America	Jul 27, 1999
5945348	1992-0680.00/US	METHOD FOR REDUCING THE HEIGHTS OF INTERCONNECTS ON A PROJECTING REGION WITH A SMALLER REDUCTION IN THE HEIGHTS OF OTHER INTERCONNECTS (AS AMENDED)	United States of America	Aug 31, 1999
6040221	1992-0488.01/US	SEMICONDUCTOR PROCESSING METHOD OF FORMING A BURIED CONTACT	United States of America	Mar 21, 2000
6057198	1992-0415.01/US	SEMICONDUCTOR PROCESSING METHOD OF FORMING A BURIED CONTACT	United States of America	May 2, 2000
6066549	1992-0488.02/US	SEMICONDUCTOR PROCESSING METHOD OF FORMING A BURIED CONTACT	United States of America	May 23, 2000
6090707	1998-1290.00/US	METHOD OF FORMING A CONDUCTIVE SILICIDE LAYER ON A SILICON COMPRISING SUBSTRATE AND METHOD OF FORMING A CONDUCTIVE SILICIDE CONTACT	United States of America	Jul 18, 2000
6130474	1996-0243.03/US	LEADS UNDER CHIP/CONVENTIONAL IC PACKAGE ASSEMBLY	United States of America	Oct 10, 2000

Aptina Semiconductor Issued

PATENT NUMBER	FILE NUMBER	TITLE	COUNTRY NAME	ISSUE DATE
6221763	1998-0673.00/US	METHOD OF FORMING A METAL SEED LAYER FOR SUBSEQUENT PLATING	United States of America	Apr 24, 2001
6271580	1996-0243.02/US	LEADS UNDER CHIP/CONVENTIONAL IC PACKAGE ASSEMBLY	United States of America	Aug 7, 2001
6274897	1992-0680.01/US	SEMICONDUCTOR STRUCTURE HAVING INTERCONNECTS ON A PROJECTING REGION AND SUBSTRATE	United States of America	Aug 14, 2001
6277673	1996-0243.01/US	LEADS UNDER CHIP IN CONVENTIONAL IC PACKAGE	United States of America	Aug 21, 2001
6284648	1992-0488.03/US	SEMICONDUCTOR PROCESSING METHOD OF FORMING A BURIED CONTACT	United States of America	Sep 4, 2001
6303972	1998-0616.00/US	DEVICE INCLUDING A CONDUCTIVE LAYER PROTECTED AGAINST OXIDATION	United States of America	Oct 16, 2001
6320246	1997-0826.01/US	SEMICONDUCTOR WAFER ASSEMBLIES	United States of America	Nov 20, 2001
6323046	1997-0800.00/US	METHOD AND APPARATUS FOR ENDPOINTING A CHEMICAL-MECHANICAL PLANARIZATION PROCESS	United States of America	Nov 27, 2001
6329670	1998-0210.00/US	CONDUCTIVE MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	United States of America	Dec 11, 2001
6344364	1997-0826.02/US	ETCHING METHODS	United States of America	Feb 5, 2002
6379981	1997-0826.00/US	METHODS INCORPORTATING DETECABLE ATOMS INTO ETCHING PROCESSES	United States of America	Apr 30, 2002
6445061	1996-0243.04/US	LEADS UNDER CHIP IN CONVENTIONAL IC PACKAGE	United States of America	Sep 3, 2002
6468854	1998-0616.10/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Oct 22, 2002
6472264	1998-0616.14/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Oct 29, 2002
6479340	1998-0616.06/US	DEVICE AND METHOD FOR	United States of America	Nov 12, 2002

Aptina Semiconductor Issued

PATENT NUMBER	FILE NUMBER	TITLE	COUNTRY NAME	ISSUE DATE
		PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE		
6489194	1998-0616.08/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Dec 3, 2002
6489235	1998-0673.01/US	METHOD OF FORMING A METAL SEED LAYER FOR SUBSEQUENT PLATING	United States of America	Dec 3, 2002
6517668	1997-0800.04/US	METHOD AND APPARATUS FOR ENDPOINTING A CHEMICAL-MECHANICAL PLANARIZATION PROCESS	United States of America	Feb 11, 2003
6518181	1998-0210.02/US	CONDUCTIVE MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	United States of America	Feb 11, 2003
6562182	1997-0800.02/US	METHOD AND APPARATUS FOR ENDPOINTING A CHEMICAL-MECHANICAL PLANARIZATION PROCESS	United States of America	May 13, 2003
6602785	1998-1200.01/US	METHOD OF FORMING A CONDUCTIVE CONTACT ON A SUBSTRATE AND METHOD OF PROCESSING A SEMICONDUCTOR SUBSTRATE USING AN OZONE TREATMENT	United States of America	Aug 5, 2003
6607975	1998-0616.07/US	DEVICE AND METHOD FOR PROTECTING OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Aug 19, 2003
6646456	1998-0210.01/US	CONDUCTIVE MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	United States of America	Nov 11, 2003
6699781	1998-0210.06/US	CONDUCTIVE MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	United States of America	Mar 2, 2004
6720215	1998-0616.04/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Apr 13, 2004
6756301	1998-0673.02/US	METHOD OF FORMING A METAL SEED LAYER FOR SUBSEQUENT	United States of America	Jun 29, 2004

Aptina Semiconductor Issued

PATENT NUMBER	FILE NUMBER	TITLE	COUNTRY NAME	ISSUE DATE
		PLATING		
6765398	1998-0210.05/US	CONDUCTIVE MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	United States of America	Jul 20, 2004
6776871	1997-0800.03/US	METHOD AND APPARATUS FOR ENDPOINTING A CHEMICAL-MECHANICAL PLANARIZATION PROCESS	United States of America	Aug 17, 2004
6781365	1998-0210.04/US	CONDUCTIVE MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	United States of America	Aug 24, 2004
6808976	1998-0616.09/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Oct 26, 2004
6830961	1996-0243.05/US	LEADS UNDER CHIP IN CONVENTIONAL IC PACKAGE	United States of America	Dec 14, 2004
6852622	1998-0616.15/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Feb 8, 2005
6870380	1998-0210.03/US	CONDUCTIVE MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	United States of America	Mar 22, 2005
6897512	1998-0616.16/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	May 24, 2005
6906547	1998-0210.07/US	CONDUCTIVE MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	United States of America	Jun 14, 2005
6916699	1998-0616.05/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Jul 12, 2005
6924188	1998-0616.12/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Aug 2, 2005
6958528	1996-0243.07/US	LEADS UNDER CHIP IN CONVENTIONAL IC PACKAGE	United States of America	Oct 25, 2005
6972452	1998-0616.17/US	DEVICE AND METHOD FOR	United States of America	Dec 6, 2005

Aptina Semiconductor Issued

PATENT NUMBER	FILE NUMBER	TITLE	COUNTRY NAME	ISSUE DATE
		PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE		
7041550	1998-0616.13/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	May 9, 2006
7046029	1998-0210.08/US	CONDUCTIVE MATERIAL FOR INTEGRATED CIRCUIT FABRICATION	United States of America	May 16, 2006
7049191	1998-0616.03/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	May 23, 2006
7067861	1998-0616.01/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Jun 27, 2006
7084490	1996-0243.08/US	LEADS UNDER CHIP IC PACKAGE	United States of America	Aug 1, 2006
7094657	1998-0616.02/US	DEVICE AND METHOD FOR PROTECTING AGAINST OXIDATION OF A CONDUCTIVE LAYER IN SAID DEVICE	United States of America	Aug 22, 2006
Total number of records: 64				