PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4141825

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SOFT MACHINES, INC.	11/07/2016

RECEIVING PARTY DATA

Name:	INTEL CORPORATION
Street Address:	2200 MISSION COLLEGE BOULEVARD
City:	SANTA CLARA
State/Country:	CALIFORNIA
Postal Code:	95054

PROPERTY NUMBERS Total: 217

Property Type	Number
Application Number:	61384198
Application Number:	13824013
Application Number:	61392391
Application Number:	13879365
Application Number:	61392392
Application Number:	13879374
Application Number:	61436962
Application Number:	13359767
PCT Number:	US2012022538
Application Number:	61436975
Application Number:	13359817
Application Number:	15176079
PCT Number:	US2012022589
Application Number:	61436973
Application Number:	13359961
Application Number:	14961464
PCT Number:	US2012022598
Application Number:	61436966
Application Number:	13360024
Application Number:	15042005

Property Type	Number
PCT Number:	US2012022760
Application Number:	61436957
Application Number:	13359832
Application Number:	15208404
PCT Number:	US2012022773
Application Number:	61436959
Application Number:	13359939
Application Number:	15009684
PCT Number:	US2012022780
Application Number:	14360282
Application Number:	15283836
Application Number:	14360284
Application Number:	14360280
Application Number:	61660538
PCT Number:	US2013045730
Application Number:	14567699
Application Number:	61660610
PCT Number:	US2013045722
Application Number:	14567731
PCT Number:	US2013045734
Application Number:	14567797
Application Number:	61660548
Application Number:	14559740
PCT Number:	US2013045261
Application Number:	61660553
PCT Number:	US2013045193
Application Number:	14560974
Application Number:	61660592
PCT Number:	US2013045470
Application Number:	14569537
Application Number:	61660521
PCT Number:	US2013045497
Application Number:	14563583
Application Number:	61660526
PCT Number:	US2013045020
Application Number:	14569554
Application Number:	61660528
PCT Number:	US2013045863

Property Type	Number
Application Number:	14569543
Application Number:	61660539
PCT Number:	US2013045008
Application Number:	14569551
Application Number:	61488683
Application Number:	13475739
Application Number:	15219063
PCT Number:	US2012038713
Application Number:	61488662
Application Number:	13475708
PCT Number:	US2012038711
Application Number:	61467944
Application Number:	13428440
Application Number:	15082359
PCT Number:	US2012030360
Application Number:	61467939
Application Number:	13428438
Application Number:	15082867
PCT Number:	US2012030383
Application Number:	61467940
Application Number:	13428452
Application Number:	15019920
PCT Number:	US2012030409
Application Number:	14376825
Application Number:	14385968
PCT Number:	US2011056757
Application Number:	14825502
Application Number:	13414456
Application Number:	14590902
Application Number:	15276664
PCT Number:	US2013029199
Application Number:	13561528
Application Number:	14922053
PCT Number:	US2013051128
Application Number:	13561570
Application Number:	14922035
Application Number:	13561441
Application Number:	14922042

Property Type	Number
Application Number:	13561491
Application Number:	13649505
Application Number:	15244873
Application Number:	13649469
Application Number:	15145615
Application Number:	13649532
Application Number:	15003486
Application Number:	61800885
Application Number:	14216855
Application Number:	15157158
Application Number:	61799902
Application Number:	14212203
Application Number:	14212533
PCT Number:	US2014024608
Application Number:	61798988
Application Number:	14213115
Application Number:	61799006
Application Number:	14213854
PCT Number:	US2014024276
Application Number:	61799299
Application Number:	14214045
Application Number:	61799530
Application Number:	14216859
PCT Number:	US2014024677
Application Number:	61799407
Application Number:	14213135
Application Number:	61799736
Application Number:	14213692
PCT Number:	US2014024722
Application Number:	61799892
Application Number:	14214176
Application Number:	61800123
Application Number:	14214280
PCT Number:	US2014024775
Application Number:	61800179
Application Number:	14213218
Application Number:	61800487
Application Number:	14213730

Property Type	Number
PCT Number:	US2014024828
Application Number:	61793466
Application Number:	14063173
Application Number:	14063409
Application Number:	61793042
Application Number:	14182618
Application Number:	61792676
Application Number:	14211476
PCT Number:	US2014026176
Application Number:	61792885
Application Number:	14209736
Application Number:	61793174
Application Number:	14211655
PCT Number:	US2014026252
Application Number:	61793541
Application Number:	14101615
Application Number:	15219119
PCT Number:	US2014027200
Application Number:	61799062
Application Number:	14107116
PCT Number:	US2014027252
Application Number:	61799717
Application Number:	14216493
Application Number:	61793703
Application Number:	14215633
Application Number:	15257593
Application Number:	61799116
Application Number:	14211878
Application Number:	14281663
Application Number:	61793752
Application Number:	14052571
Application Number:	15215004
PCT Number:	US2014026312
Application Number:	61800498
Application Number:	14173602
Application Number:	61852389
Application Number:	14213909
PCT Number:	US2014026427

Property Type	Number
Application Number:	61852057
Application Number:	14216683
Application Number:	61852338
Application Number:	14214049
Application Number:	13970277
Application Number:	14015086
Application Number:	14819255
Application Number:	13970311
Application Number:	13970344
Application Number:	61991951
Application Number:	14710372
Application Number:	62029383
Application Number:	14806169
PCT Number:	US2015041847
Application Number:	14807141
PCT Number:	US2015042002
Application Number:	14807271
PCT Number:	US2015041850
Application Number:	14807308
PCT Number:	US2015042019
Application Number:	14807313
PCT Number:	US2015041851
Application Number:	14807343
PCT Number:	US2015042010
Application Number:	14807353
PCT Number:	US2015042032
Application Number:	14515333
Application Number:	14515379
Application Number:	14515345
Application Number:	62367537
Application Number:	62367553
Application Number:	62367558
Application Number:	60791782
Application Number:	60791649
Application Number:	12296919
Application Number:	13691609
Application Number:	14733827
Application Number:	60792219

Property Type	Number
Application Number:	60865813
Application Number:	60865816
Application Number:	60865818
Application Number:	60865820
Application Number:	12514303
Application Number:	14194589
Application Number:	61660544

CORRESPONDENCE DATA

Fax Number: (612)677-3572

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 612-236-9942
Email: amiller1@cpaglobal.com
Correspondent Name: ANGELA MILLER
Address Line 1: C/O CPA GLOBAL
Address Line 2: 900 SECOND AVENUE SOUTH, SUITE 600
Address Line 4: MINNEAPOLIS, MINNESOTA 55402

ATTORNEY DOCKET NUMBER:	SOFT MACHINES
NAME OF SUBMITTER:	ANGELA MILLER
SIGNATURE:	/Angela Miller/
DATE SIGNED:	11/14/2016

Total Attachments: 53
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Patent Assignment

Soft Machines, Inc., a Delaware corporation, with an office at 3920 Freedom Circle, Santa Clara, CA 95054 ("Assignor") is the sole owner of the patents and patent applications listed in Schedule 1 hereto (collectively the "Patents"); and Intel Corporation, a Delaware corporation with its principal place of business at 2200 Mission College Boulevard, Santa Clara, California 95054 ("Buyer") desires to acquire all right, title and interest in the Patents and the related rights described below.

For good and valuable consideration, the receipt of which is hereby acknowledged, Assignor does hereby sell, assign, transfer and convey to Buyer and its successors and assigns all right, title and interest that may exist today and in the future to any and all:

(1) Patents;

(2) patents and patent applications to which any of the patents or patent applications listed in Schedule 1 directly or indirectly claims, or forms the basis for, priority anywhere in the world;

(3) reissues, reexaminations, extensions, continuations, continuations-in-part, continuing prosecution applications and divisions of any of the items listed in (1) or (2) of this Assignment;

(4) foreign counterparts to any of the items listed in (1), (2) or (3) of this Assignment, including utility models, inventors' certificates, industrial design protection and any other form of governmental grants or issuances for the protection of inventions, designs or discoveries;

(5) inventions, invention disclosures, designs and discoveries described in the items listed in (1) through (4) of this Assignment;

(6) patents that issue from any of the items listed in (1) through (5) of this Assignment;

(7) claims, causes of action and enforcement rights of any kind, whether currently pending, filed or otherwise, and whether known or unknown, under or arising from any of the items listed in (1) through (6) of this Assignment, including all rights to pursue and collect damages, costs, injunctive relief and other remedies for past, current or future infringement of the Patents and including rights afforded under 35 U.S.C. § 154(d);

(8) royalties, income and other payments due as of the date hereof or hereafter under or arising from any of the items listed in (1) through (7) of this Assignment; and

(9) rights to apply for, file, register, maintain, extend and renew in any or all countries of the world patents, certificates of invention, utility models, industrial design protection, design patent protection and other governmental grants or issuances of any kind related to any of the items listed in (1) through (9) of this Assignment.

Assignor shall execute and deliver any instruments, and do and perform any other acts and things as may be reasonably necessary or desirable for effecting and evidencing the assignments contemplated hereby, including the execution, acknowledgment and recordation of any instruments.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks and any other patent office to issue any and all patents, utility models or other governmental grants or issuances pertaining to any of the items assigned hereunder in the name of Buyer.

This Assignment will inure to the benefit of Buyer and its successors, assigns and other legal representatives and is binding upon Assignor and its successors, assigns, heirs and legal representatives.

Assignor, by its duly authorized representative, has executed this Assignment on the date set forth below.

DATE: November 7, 2016

By: Tiffany Dos Silva
Printed/Typed Name

Title: Assistant Secretary

C Henry Legal 11/7/16

Signature

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document

STATE OF CALIFORNIA)
) ss.
COUNTY OF SANTA CLARA)

On this 7th day of November 2016, before me, J. Argabright notary public personally appeared Tiffany D. Silva, who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct

WITNESS my hand and official seal.

J. ARGABRIGHT
Notary Public - California
Santa Clara County
Commission # 2157751
My Comm. Expires Jul 21, 2020

Signature of Notary Public

ACCEPTED:

DATE: November 7, 2016

Intel Corporation

By: Jenny J. Kim
Printed/Typed Name

Title: VP, Law & Policy Group

Signature

Patent Assignment
Schedule 1

Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	US	61/384,198	9/17/2010	N/A	N/A	Expired 9/17/2011
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	TW	100133656	9/19/2011	TW201227504	7/1/2012	Granted
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	PCT	PCT/US2011/051992	9/16/2011	WO/2012/037491	3/22/2012	Expired 3/17/2013
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	CN	201180053524.1	9/16/2011 Entry Date 5/6/2013	CN103250131	8/14/2013	Granted
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	KR	10-20137009758	9/16/2011 Entry Date 4/17/2013	10-20140014070 Unexamined	2/5/2014	Pending
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	US	13/824,013	9/16/2011	N/A	N/A	Pending (revived)
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	IN	2195/CHENP/2013	9/16/2011 Entry Date 3/19/2013	N/A	N/A	Pending
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	EP	11826042.1	9/16/2011 Entry Date 4/11/2013	EP2616928	7/24/2013	Expected to Grant on 11/2/2016
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	DE	11826042.1	9/16/2011	EP2616928	7/24/2013	Granted
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	FR	11826042.1	9/16/2011	EP2616928	7/24/2013	Granted
SINGLE CYCLE MULTI-BRANCH PREDICTION INCLUDING SHADOW CACHE FOR EARLY FAR BRANCH PREDICTION	GB	11826042.1	9/16/2011	EP2616928	7/24/2013	Granted

Patent Assignment
Schedule 1

Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
AN INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	US	61/392,391	10/12/2010	N/A	N/A	Expired 10/12/2011
INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	TW	100136923	10/12/2011	TW201237751	9/16/2012	Granted
AN INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	PCT	PCT/US2011/055917	10/12/2011	WO/2012/051262	4/19/2012	Expired 4/12/2013
INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	CN	201180057070.5	10/12/2011 Entry Date 5/30/2013	CN103282874	9/4/2013	Published
INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	IN	2785/CHENP/2013	10/12/2011 Entry Date 4/10/2013	N/A	N/A	Pending
INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	US	13/879,365	10/12/2011 Entry Date 8/12/2013	US 2013-0311759 A1	11/21/2013	Published
INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	EP	11833310.3	10/12/2011 Entry Date 4/11/2013	EP2628072	8/21/2013	Granted
INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	DE	11833310.3	10/12/2011	EP2628072	8/21/2013	Granted
INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	FR	11833310.3	10/12/2011	EP2628072	8/21/2013	Granted
INSTRUCTION SEQUENCE BUFFER TO ENHANCE BRANCH PREDICTION EFFICIENCY	GB	11833310.3	10/12/2011	EP2628072	8/21/2013	Granted
INSTRUCTION SEQUENCE BUFFER TO STORE BRANCHES HAVING RELIABLY PREDICTABLE INSTRUCTION SEQUENCES	US	61/392,392	10/12/2010	N/A	N/A	Expired 10/12/2011

Patent Assignment
Schedule 1

Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
INSTRUCTION SEQUENCE BUFFER TO STORE BRANCHES HAVING RELIABLY PREDICTABLE INSTRUCTION SEQUENCE	TW	100136924	10/12/2011	TW201235939	9/1/2012	Granted
AN INSTRUCTION SEQUENCE BUFFER TO STORE BRANCHES HAVING RELIABLY PREDICTABLE INSTRUCTION SEQUENCES	PCT	PCT/US2011/055943	10/12/2011	WO/2012/051281	4/19/2012	Expired 4/12/2013
SEQUENCE BUFFER FOR OPTIMIZING EXECUTION OF FREQUENTLY EXECUTED BRANCHES THAT ARE OFTEN PREDICTED ACCURATELY	CN	201180057525.3	10/12/2011 Entry Date 5/29/2013	CN103262027	8/21/2013	Granted
AN INSTRUCTION SEQUENCE BUFFER TO STORE BRANCHES HAVING RELIABLY PREDICTABLE INSTRUCTION SEQUENCES	EP	11833322.8	10/12/2011 Entry Date 4/11/2013	EP2628076	8/21/2013	Published
INSTRUCTION SEQUENCE BUFFER TO STORE BRANCHES HAVING RELIABLY PREDICTABLE INSTRUCTION SEQUENCES	US	13/879,374	10/12/2011 Entry Date 11/27/2013	US 2014-0075168 A1	3/13/2014	Published
AN INSTRUCTION SEQUENCE BUFFER TO STORE BRANCHES HAVING RELIABLY PREDICTABLE INSTRUCTION SEQUENCES	IN	2786/CHENP/2013	10/12/2011 Entry Date 4/10/2013	N/A	N/A	Pending
GUEST INSTRUCTION TO NATIVE INSTRUCTION RANGE BASED MAPPING USING A CONVERSION LOOK ASIDE BUFFER OF A PROCESSOR	US	61/436,962	1/27/2011	N/A	N/A	Expired 1/27/2012
GUEST INSTRUCTION TO NATIVE INSTRUCTION RANGE BASED MAPPING USING A CONVERSION LOOK ASIDE BUFFER OF A PROCESSOR	US	13/359,767	1/27/2012	US 2012-0198157 A1	8/2/2012	Allowed

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
GUEST INSTRUCTION TO NATIVE INSTRUCTION RANGE BASED MAPPING USING A CONVERSION LOOK ASIDE BUFFER OF A PROCESSOR	TW	101102834	1/30/2012	TW201250583	12/16/2012	Granted
GUEST INSTRUCTION TO NATIVE INSTRUCTION RANGE BASED MAPPING USING A CONVERSION LOOK ASIDE BUFFER OF A PROCESSOR	PCT	PCT/US2012/022538	1/25/2012	WO/2012/103209	8/2/2012	Expired 7/27/2013
GUEST INSTRUCTION TO NATIVE INSTRUCTION RANGE BASED MAPPING USING A CONVERSION LOOK ASIDE BUFFER OF A PROCESSOR	CN	201280012962.8	1/25/2012 Entry Date 9/11/2013	CN103620547	3/5/2014	Published
GUEST INSTRUCTION TO NATIVE INSTRUCTION RANGE BASED MAPPING USING A CONVERSION LOOK ASIDE BUFFER OF A PROCESSOR	EP	12739955.8	1/25/2012 Entry Date 8/27/2013	EP2668565	12/4/2013	Published
GUEST INSTRUCTION TO NATIVE INSTRUCTION RANGE BASED MAPPING USING A CONVERSION LOOK ASIDE BUFFER OF A PROCESSOR	KR	10-20137022671	1/25/2012 Entry Date 8/27/2013	10-20140006926	1/16/2014	Granted
GUEST INSTRUCTION TO NATIVE INSTRUCTION RANGE BASED MAPPING USING A CONVERSION LOOK ASIDE BUFFER OF A PROCESSOR	IN	5852/CHENP/2013	1/25/2012 Entry Date 7/22/2013	45/2014	11/7/2014	Pending
GUEST INSTRUCTION BLOCK WITH NEAR BRANCHING AND FAR BRANCHING SEQUENCE CONSTRUCTION TO NATIVE INSTRUCTION BLOCK	US	61/436,975	1/27/2011	N/A	N/A	Expired 1/27/2012
GUEST INSTRUCTION BLOCK WITH NEAR BRANCHING AND FAR BRANCHING SEQUENCE CONSTRUCTION TO NATIVE INSTRUCTION BLOCK	US	13/359,817	1/27/2012	US 2012-0198209 A1	8/2/2012	Allowed

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
GUEST INSTRUCTION BLOCK WITH NEAR BRANCHING AND FAR BRANCHING SEQUENCE CONSTRUCTION TO NATIVE INSTRUCTION BLOCK	US	15/176,079	6/7/2016	US 2016-0283239 A1	9/29/2016	Published
GUEST INSTRUCTION BLOCK WITH NEAR BRANCHING AND FAR BRANCHING SEQUENCE CONSTRUCTION TO NATIVE INSTRUCTION BLOCK	TW	101102831	1/30/2012	TW201246066	11/16/2012	Granted
GUEST INSTRUCTION BLOCK WITH NEAR BRANCHING AND FAR BRANCHING SEQUENCE CONSTRUCTION TO NATIVE INSTRUCTION BLOCK	PCT	PCT/US2012/022589	1/25/2012	WO/2012/103245	8/2/2012	Expired 7/27/2013
MULTILEVEL CONVERSION TABLE CACHE FOR TRANSLATING GUEST INSTRUCTIONS TO NATIVE INSTRUCTIONS	US	61/436,973	1/27/2011	N/A	N/A	Expired 1/27/2012
MULTILEVEL CONVERSION TABLE CACHE FOR TRANSLATING GUEST INSTRUCTIONS TO NATIVE INSTRUCTIONS	US	13/359,961	1/27/2012	US 2013-0024619 A1	1/24/2013	Granted
MULTILEVEL CONVERSION TABLE CACHE FOR TRANSLATING GUEST INSTRUCTIONS TO NATIVE INSTRUCTIONS	US	14/961,464	12/7/2015	N/A	N/A	Pending
MULTILEVEL CONVERSION TABLE CACHE FOR TRANSLATING GUEST INSTRUCTIONS TO NATIVE INSTRUCTIONS	TW	101102832	1/30/2012	TW201246064	11/16/2012	Pending
MULTILEVEL CONVERSION TABLE CACHE FOR TRANSLATING GUEST INSTRUCTIONS TO NATIVE INSTRUCTIONS	PCT	PCT/US2012/022598	1/25/2012	WO/2012/103253	8/2/2012	Expired 7/27/2013

Patent Assignment
Schedule 1

Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
HARDWARE ACCELERATION COMPONENTS FOR TRANSLATING GUEST INSTRUCTIONS TO NATIVE INSTRUCTIONS	US	61/436,966	1/27/2011	N/A	N/A	Expired 1/27/2012
MAPPING OF GUEST INSTRUCTION BLOCK ASSEMBLED ACCORDING TO BRANCH PREDICTION TO TRANSLATED NATIVE CONVERSION BLOCK	US	13/360,024	1/27/2012	US 2013-0024661 A1	1/24/2013	Published
HARDWARE ACCELERATION COMPONENT FOR TRANSLATION GUEST INSTRUCTIONS TO NATIVE INSTRUCTIONS	US	15/042,005	2/11/2016	N/A	N/A	Pending
HARDWARE ACCELERATION COMPONENTS FOR TRANSLATING GUEST INSTRUCTIONS TO NATIVE INSTRUCTIONS	TW	101102835	1/30/2012	TW201245976	11/16/2012	Granted
HARDWARE ACCELERATION COMPONENTS FOR TRANSLATING GUEST INSTRUCTIONS TO NATIVE INSTRUCTIONS	PCT	PCT/US2012/022760	1/26/2012	WO/2012/103359	8/2/2012	Expired 7/27/2013
GUEST TO NATIVE BLOCK ADDRESS MAPPINGS AND MANAGEMENT OF NATIVE CODE STORAGE	US	61/436,957	1/27/2011	N/A	N/A	Expired 1/27/2012
GUEST TO NATIVE BLOCK ADDRESS MAPPINGS AND MANAGEMENT OF NATIVE CODE STORAGE	US	13/359,832	1/27/2012	US 2012-0198122 A1	8/2/2012	Allowed
GUEST TO NATIVE BLOCK ADDRESS MAPPINGS AND MANAGEMENT OF NATIVE CODE STORAGE	US	15/208,404	7/12/2016	N/A	N/A	Pending
GUEST TO NATIVE BLOCK ADDRESS MAPPINGS AND MANAGEMENT OF NATIVE CODE STORAGE	TW	101102838	1/30/2012	TW201303593	1/16/2013	Granted

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GUEST TO NATIVE BLOCK ADDRESS MAPPINGS AND MANAGEMENT OF NATIVE CODE STORAGE	PCT	PCT/US2012/022773	1/26/2012	WO/2012/103367	8/2/2012	Expired 7/27/2013
VARIABLE CACHING STRUCTURE FOR MANAGING PHYSICAL STORAGE	US	61/436,959	1/27/2011	N/A	N/A	Expired 1/27/2012
VARIABLE CACHING STRUCTURE FOR MANAGING PHYSICAL STORAGE	US	13/359,939	1/27/2012	US 2012-0198168 A1	8/2/2012	Allowed
VARIABLE CACHING STRUCTURE FOR MANAGING PHYSICAL STORAGE	US	15/009,684	1/28/2016	US 2016-0224472 A1	8/4/2016	Published
VARIABLE CACHING STRUCTURE FOR MANAGING PHYSICAL STORAGE	PCT	PCT/US2012/022780	1/26/2012	WO/2012/103373	8/2/2012	Expired 7/27/2013
VARIABLE CACHING STRUCTURE FOR MANAGING PHYSICAL STORAGE	TW	101102840	1/30/2012	TW201246069	11/16/2012	Granted
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER	TW	100142885	11/23/2011	TW201322122	6/1/2013	Pending
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER	PCT	PCT/US2011/061957	11/22/2011	WO/2013/077876	5/30/2013	Expired 5/22/2014
MICROPROCESSOR ACCELERATED CODE OPTIMIZER	US	14/360,282	11/22/2011 Entry Date 9/15/2014	US 2015-0039859 A1	2/5/2015	Published
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER	US	15/283,836	10/3/2016	N/A	N/A	Pending
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER	CN	201180076248.0	11/22/2011 Entry Date 7/14/2014	CN104040491	9/10/2014	Published
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER	EP	11876314.3	11/22/2011 Entry Date 5/22/2014	EP2783281	10/1/2014	Published
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER	IN	3611/CHENP/2014	11/22/2011 Entry Date 5/13/2014	N/A	N/A	Pending
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER	KR	10-20147016763	11/22/2011 Entry Date 6/18/2014	10-20140093721 Unexamined	7/28/2014	Pending
AN ACCELERATED CODE OPTIMIZER FOR A MULTIENGINE MICROPROCESSOR	TW	100142887	11/23/2011	TW201322120	6/1/2013	Granted
AN ACCELERATED CODE OPTIMIZER FOR A MULTIENGINE MICROPROCESSOR	PCT	PCT/US2011/061953	11/22/2011	WO/2013/077875	5/30/2013	Expired 5/22/2014

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ACCELERATED CODE OPTIMIZER FOR A MULTIENGINE MICROPROCESSOR	US	14/360,284	11/22/2011 Entry Date 10/06/2014	US 2015-0186144 A1	7/2/2015	Published
AN ACCELERATED CODE OPTIMIZER FOR A MULTIENGINE MICROPROCESSOR	CN	201180076244.2	11/22/2011 Entry Date 7/14/2014	CN104040490	9/10/2014	Published
AN ACCELERATED CODE OPTIMIZER FOR A MULTIENGINE MICROPROCESSOR	EP	11876128.7	11/22/2011 Entry Date 5/22/2014	EP2783280	10/1/2014	Published
AN ACCELERATED CODE OPTIMIZER FOR A MULTIENGINE MICROPROCESSOR	IN	3678/CHENP/2014	11/22/2011 Entry Date 5/14/2014	39/2015	9/25/2015	Pending
AN ACCELERATED CODE OPTIMIZER FOR A MULTIENGINE MICROPROCESSOR	KR	10-20147016764	11/22/2011 Entry Date 6/18/2014	10-20140094014	7/29/2014	Pending
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER AND DEPENDENCY REORDERING METHOD	TW	100142888	11/23/2011	TW201322123	6/1/2013	Granted
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER AND DEPENDENCY REORDERING METHOD	PCT	PCT/US2011/061940	11/22/2011	WO/2013/077872	5/30/2013	Expired 5/22/2014
MICROPROCESSOR ACCELERATED CODE OPTIMIZER AND DEPENDENCY REORDERING METHOD	US	14/360,280	11/22/2011 Entry Date 7/29/2014	US 2014-0344554 A1	11/20/2014	Published
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER AND DEPENDENCY REORDERING METHOD	CN	201180076245.7	11/22/2011 Entry Date 7/14/2014	CN104040492	9/10/2014	Published
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER AND DEPENDENCY REORDERING METHOD	EP	11876130.3	11/22/2011 Entry Date 5/22/2014	EP2783282	10/1/2014	Published
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER AND DEPENDENCY REORDERING METHOD	IN	3703/CHENP/2014	11/22/2011 Entry Date 5/16/2014	41/2015	10/9/2015	Pending
A MICROPROCESSOR ACCELERATED CODE OPTIMIZER AND DEPENDENCY REORDERING METHOD	KR	10-20147016774	11/22/2011 Entry Date 6/18/2014	10-20140094015	7/29/2014	Granted

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A METHOD AND SYSTEM FOR IMPLEMENTING RECOVERY FROM SPECULATIVE FORWARDING MISS-PREDICTIONS/ERRORS RESULTING FROM LOAD STORE REORDERING AND OPTIMIZATION	US	61/660,538	6/15/2012	N/A	N/A	Expired 6/15/2103
A METHOD AND SYSTEM FOR IMPLEMENTING RECOVERY FROM SPECULATIVE FORWARDING MISS-PREDICTIONS/ERRORS RESULTING FROM LOAD STORE REORDERING AND OPTIMIZATION	TW	102121098	6/14/2013	TW201428620	7/16/2014	Pending
A METHOD AND SYSTEM FOR IMPLEMENTING RECOVERY FROM SPECULATIVE FORWARDING MISS-PREDICTIONS/ERRORS RESULTING FROM LOAD STORE REORDERING AND OPTIMIZATION	PCT	PCT/US2013/045730	6/13/2013	WO/2013/188701	12/19/2013	Expired 12/15/2014
A METHOD AND SYSTEM FOR IMPLEMENTING RECOVERY FROM SPECULATIVE FORWARDING MISS-PREDICTIONS/ERRORS RESULTING FROM LOAD STORE REORDERING AND OPTIMIZATION	US	14/567,699	6/13/2013 Entry Date 12/11/2014	US 2015-0095629 A1	4/2/2015	Published
A METHOD AND SYSTEM FOR IMPLEMENTING RECOVERY FROM SPECULATIVE FORWARDING MISS-PREDICTIONS/ERRORS RESULTING FROM LOAD STORE REORDERING AND OPTIMIZATION	CN	201380042999.X	6/13/2013 Entry Date 2/12/2015	CN104823168	8/5/2015	Published

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A METHOD AND SYSTEM FOR IMPLEMENTING RECOVERY FROM SPECULATIVE FORWARDING MISS-PREDICTIONS/ERRORS RESULTING FROM LOAD STORE REORDERING AND OPTIMIZATION	EP	13803753.6	6/13/2013 Entry Date 12/15/2104	EP2862084	4/22/2015	Published
A METHOD AND SYSTEM FOR IMPLEMENTING RECOVERY FROM SPECULATIVE FORWARDING MISS-PREDICTIONS/ERRORS RESULTING FROM LOAD STORE REORDERING AND OPTIMIZATION	IN	8939/CHENP/2014	6/13/2013 Entry Date 12/10/2104	27/2016	7/1/2016	Pending
A METHOD AND SYSTEM FOR IMPLEMENTING RECOVERY FROM SPECULATIVE FORWARDING MISS-PREDICTIONS/ERRORS RESULTING FROM LOAD STORE REORDERING AND OPTIMIZATION	KR	10-20157000752	6/13/2013 Entry Date 1/12/2015	10-20150020246	2/25/2015	Granted
AN INSTRUCTION DEFINITION TO IMPLEMENT LOAD STORE REORDERING AND OPTIMIZATION	US	61/660,610	6/15/2012	N/A	N/A	Expired 6/15/2013
AN INSTRUCTION DEFINITION TO IMPLEMENT LOAD STORE REORDERING AND OPTIMIZATION	TW	102121100	6/14/2013	TW201428621	7/16/2014	Published
AN INSTRUCTION DEFINITION TO IMPLEMENT LOAD STORE REORDERING AND OPTIMIZATION	PCT	PCT/US2013/045722	6/13/2013	WO/2013/188696	12/19/2013	Expired 12/15/2014
INSTRUCTION DEFINITION TO IMPLEMENT LOAD STORE REORDERING AND OPTIMIZATION	US	14/567,731	6/13/2013 Entry date 12/11/2014	US 2015-0095615 A1	4/2/2015	Published
AN INSTRUCTION DEFINITION TO IMPLEMENT LOAD STORE REORDERING AND OPTIMIZATION	CN	201380042998.5	6/13/2013 Entry Date 2/12/2015	CN104583956	4/29/2015	Published

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AN INSTRUCTION DEFINITION TO IMPLEMENT LOAD STORE REORDERING AND OPTIMIZATION	EP	13804462.3	6/13/2013 Entry Date 12/15/2014	EP2862069	4/22/2015	Published
AN INSTRUCTION DEFINITION TO IMPLEMENT LOAD STORE REORDERING AND OPTIMIZATION	IN	8940/CHENP/2014	6/13/2013 Entry Date 12/10/2014	27/2016	7/1/2016	Pending
AN INSTRUCTION DEFINITION TO IMPLEMENT LOAD STORE REORDERING AND OPTIMIZATION	KR	10-20157000708	6/13/2013 Entry Date 1/12/2015	10-20150027213 Unexamined	3/11/2015	Pending
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A UNIFIED STRUCTURE	US	61/660,544	6/15/2012	N/A	N/A	Expired 6/15/2013
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A UNIFIED STRUCTURE	TW	102121102	6/14/2013	TW201423580	6/16/2014	Pending
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A UNIFIED STRUCTURE	PCT	PCT/US2013/045734	6/13/2013	WO/2013/188705	12/19/2013	Expired 12/15/2014
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A UNIFIED STRUCTURE	US	14/567,797	6/13/2013 Entry Date 12/11/2014	US 2015-0095618 A1	4/2/2015	Published
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A UNIFIED STRUCTURE	CN	201380043000.3	6/13/2013 Entry Date 2/12/2015	CN104823154	8/5/2015	Published
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A UNIFIED STRUCTURE	EP	13803692.6	6/13/2013 Entry Date 12/15/2014	EP2862061	4/22/2015	Published
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A UNIFIED STRUCTURE	IN	8942/CHENP/2014	6/13/2013 Entry Date 12/10/2014	27/2016	7/1/2016	Pending
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A UNIFIED STRUCTURE	KR	10-20157000653	6/13/2013 Entry Date 1/12/15	10-20150027209 Unexamined	3/11/2015	Pending

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A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A DISTRIBUTED STRUCTURE	US	61/660,548	6/15/2012	N/A	N/A	Expired 6/15/2013
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A DISTRIBUTED STRUCTURE	TW	102121092	6/14/2013	TW201428617	7/16/2014	Pending
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A DISTRIBUTED STRUCTURE	US	14/559,740	6/11/2013 Entry Date 12/03/2014	US 2015-0134934 A1	5/14/2015	Published
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A DISTRIBUTED STRUCTURE	PCT	PCT/US2013/045261	6/11/2013	WO/2013/188460	12/19/2013	Expired 12/14/2014
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A DISTRIBUTED STRUCTURE	CN	201380043001.8	6/11/2013 Entry Date 2/12/2015	CN104583943	4/29/2015	Published
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A DISTRIBUTED STRUCTURE	EP	13804852.5	6/11/2013 Entry Date 12/15/2014	EP2862062	4/22/2015	Published
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A DISTRIBUTED STRUCTURE	IN	8964/CHENP/2014	6/11/2013 Entry Date 12/12/2014	27/2016	7/1/2016	Published
A VIRTUAL LOAD STORE QUEUE HAVING A DYNAMIC DISPATCH WINDOW WITH A DISTRIBUTED STRUCTURE	KR	10-20157000695	6/11/2013 Entry Date 1/12/2015	10-20150027212 Unexamined	3/11/2015	Pending
A METHOD AND SYSTEM FOR FILTERING THE STORES TO PREVENT ALL STORES FROM HAVING TO SNOOP CHECK AGAINST ALL WORDS OF A CACHE	US	61/660,553	6/15/2012	N/A	N/A	Expired 6/15/2013

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A METHOD AND SYSTEM FOR FILTERING THE STORES TO PREVENT ALL STORES FROM HAVING TO SNOOP CHECK AGAINST ALL WORDS OF A CACHE	PCT	PCT/US2013/045193	6/11/2013	WO/2013/188414	12/19/2013	Expired 12/14/2014
A METHOD AND SYSTEM FOR FILTERING THE STORES TO PREVENT ALL STORES FROM HAVING TO SNOOP CHECK AGAINST ALL WORDS OF A CACHE	TW	102121087	6/14/2013	TW201428615	7/16/2014	Published
METHOD AND SYSTEM FOR FILTERING THE STORES TO PREVENT ALL STORES FROM HAVING TO SNOOP CHECK AGAINST ALL WORDS OF A CACHE	US	14/560,974	6/11/2013 Entry Date 12/04/2014	US 2015-0095591 A1	4/2/2015	Published
A METHOD AND SYSTEM FOR FILTERING THE STORES TO PREVENT ALL STORES FROM HAVING TO SNOOP CHECK AGAINST ALL WORDS OF A CACHE	CN	201380043002.2	6/11/2013 Entry Date 2/12/2015	CN104583939	4/29/2015	Published
A METHOD AND SYSTEM FOR FILTERING THE STORES TO PREVENT ALL STORES FROM HAVING TO SNOOP CHECK AGAINST ALL WORDS OF A CACHE	EP	13804226.2	6/11/2013 Entry Date 12/15/2014	EP2862060	4/22/2015	Published
A METHOD AND SYSTEM FOR FILTERING THE STORES TO PREVENT ALL STORES FROM HAVING TO SNOOP CHECK AGAINST ALL WORDS OF A CACHE	IN	8941/CHENP/2014	6/11/2013 Entry Date 12/10/2014	27/2016	7/1/2016	Published
A METHOD AND SYSTEM FOR FILTERING THE STORES TO PREVENT ALL STORES FROM HAVING TO SNOOP CHECK AGAINST ALL WORDS OF A CACHE	KR	10-20157000693	6/11/2013 Entry Date 1/12/2015	10-20150027211 Unexamined	3/11/2015	Pending

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A SEMAPHORE METHOD AND SYSTEM WITH OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL THAT CONSTITUTES LOADS READING FROM MEMORY IN ORDER	US	61/660,592	6/15/2012	N/A	N/A	Expired 6/15/2013
A SEMAPHORE METHOD AND SYSTEM WITH OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL THAT CONSTITUTES LOADS READING FROM MEMORY IN ORDER	TW	102121094	6/14/2013	TW201428618	7/16/2014	Published
A SEMAPHORE METHOD AND SYSTEM WITH OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL THAT CONSTITUTES LOADS READING FROM MEMORY IN ORDER	PCT	PCT/US2013/045470	6/12/2013	WO/2013/188565	12/19/2013	Expired 12/15/2014
A SEMAPHORE METHOD AND SYSTEM WITH OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL THAT CONSTITUTES LOADS READING FROM MEMORY IN ORDER	US	14/569,537	6/12/2013 Entry Date 12/12/2014	US 2015-0100734 A1	4/9/2015	Published
A SEMAPHORE METHOD AND SYSTEM WITH OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL THAT CONSTITUTES LOADS READING FROM MEMORY IN ORDER	CN	201380043005.6	6/12/2013 Entry Date 2/12/2015	CN104583936	4/29/2015	Published
A SEMAPHORE METHOD AND SYSTEM WITH OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL THAT CONSTITUTES LOADS READING FROM MEMORY IN ORDER	EP	13803443.4	6/12/2013 Entry Date 12/15/2014	EP2862058	4/22/2015	Published
A SEMAPHORE METHOD AND SYSTEM WITH OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL THAT CONSTITUTES LOADS READING FROM MEMORY	IN	8965/CHENP/2014	6/12/2013 Entry Date 12/12/2014	27/2016	7/1/2016	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
A SEMAPHORE METHOD AND SYSTEM WITH OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL THAT CONSTITUTES LOADS READING FROM MEMORY	KR	10-20157000751	6/12/2013 Entry Date 1/12/2015	10-20150020245 Unexamined	2/25/2015	Published
A LOCK-BASED AND SYNCH-BASED METHOD FOR OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL USING SHARED MEMORY RESOURCES	US	61/660,521	6/15/2012	N/A	N/A	Expired 6/15/2013
A LOCK-BASED AND SYNCH-BASED METHOD FOR OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL USING SHARED MEMORY RESOURCES	TW	102121095	6/14/2013	TW201428619	7/16/2014	Published
LOCK-BASED AND SYNCH-BASED METHOD FOR OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL USING SHARED MEMORY RESOURCES	PCT	PCT/US2013/045497	6/12/2013	WO/2013/188588	12/19/2013	Expired 12/15/2014
LOCK-BASED AND SYNCH-BASED METHOD FOR OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL USING SHARED MEMORY RESOURCES	US	14/563,583	6/12/2013 Entry Date 12/08/2014	US 2015-0095588 A1	4/2/2015	Published
A LOCK-BASED AND SYNCH-BASED METHOD FOR OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL USING SHARED MEMORY RESOURCES	CN	201380042996.6	6/12/2013 Entry Date 2/12/2015	CN104583942	4/29/2015	Published
A LOCK-BASED AND SYNCH-BASED METHOD FOR OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL USING SHARED MEMORY RESOURCES	EP	13804863.2	6/12/2013 Entry Date 12/15/2014	EP2862063	4/22/2015	Published

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A LOCK-BASED AND SYNCH-BASED METHOD FOR OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL USING SHARED MEMORY RESOURCES	IN	8966/CHENP/2014	6/12/2013 Entry Date 12/12/2014	27/2016	7/1/2016	Published
A LOCK-BASED AND SYNCH-BASED METHOD FOR OUT OF ORDER LOADS IN A MEMORY CONSISTENCY MODEL USING SHARED MEMORY RESOURCES	KR	10-20157000652	6/12/2013 Entry Date 1/12/2015	10-20150020244	2/25/2015	Published
A LOAD STORE BUFFER AGNOSTIC TO THREADS IMPLEMENTING FORWARDING FROM DIFFERENT THREADS BASED ON STORE SENIORITY	US	61/660,526	6/15/2012	N/A	N/A	Expired 6/15/2013
A LOAD STORE BUFFER AGNOSTIC TO THREADS IMPLEMENTING FORWARDING FROM DIFFERENT THREADS BASED ON STORE SENIORITY	TW	102121096	6/14/2013	TW201426542	7/1/2014	Published
A LOAD STORE BUFFER AGNOSTIC TO THREADS IMPLEMENTING FORWARDING FROM DIFFERENT THREADS BASED ON STORE SENIORITY	PCT	PCT/US2013/045020	6/10/2013	WO/2013/188311	12/19/2013	Expired 12/15/2014
LOAD STORE BUFFER AGNOSTIC TO THREADS IMPLEMENTING FORWARDING FROM DIFFERENT THREADS BASED ON STORE SENIORITY	US	14/569,554	6/10/2013 Entry Date 12/12/2014	US 2015-0205605 A1	7/23/2015	Published
A LOAD STORE BUFFER AGNOSTIC TO THREADS IMPLEMENTING FORWARDING FROM DIFFERENT THREADS BASED ON STORE SENIORITY	CN	201380043004.1	6/10/2013 Entry Date 2/12/2015	CN104620223	5/13/2015	Published

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A LOAD STORE BUFFER AGNOSTIC TO THREADS IMPLEMENTING FORWARDING FROM DIFFERENT THREADS BASED ON STORE SENIORITY	EP	13805130.5	6/10/2013 Entry Date 12/15/2015	EP2862072	4/22/2015	Published
A LOAD STORE BUFFER AGNOSTIC TO THREADS IMPLEMENTING FORWARDING FROM DIFFERENT THREADS BASED ON STORE SENIORITY	IN	9000/CHENP/2014	6/10/2013 Entry Date 12/12/2014	27/2016	7/1/2016	Published
A LOAD STORE BUFFER AGNOSTIC TO THREADS IMPLEMENTING FORWARDING FROM DIFFERENT THREADS BASED ON STORE SENIORITY	KR	10-20157000654	6/10/2013 Entry Date 1/12/2015	10-20150023706 Unexamined	3/5/2015	Published
A DISAMBIGUATION FREE OUT OF ORDER LOAD STORE QUEUE	US	61/660,528	6/15/2012	N/A	N/A	Expired 6/15/2013
A DISAMBIGUATION FREE OUT OF ORDER LOAD STORE QUEUE	TW	102121088	6/14/2013	TW201421239	6/1/2014	Published
A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	PCT	PCT/US2013/045863	6/14/2013	WO/2013/188754	12/19/2013	Expired 12/15/2014
DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	US	14/569,543	6/14/2013 Entry Date 12/12/2014	US 2015-0100765 A1	4/9/2015	Published
A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	CN	201380043007.5	6/14/2013 Entry Date 2/12/2015	CN104583975	4/29/2015	Published
DISAMBIGUATION FREE OUT OF ORDER LOAD STORE QUEUE	EP	13805015.8	6/14/2013 Entry Date 12/15/2014	EP2862087	4/22/2015	Published
A DISAMBIGUATION FREE OUT OF ORDER LOAD STORE QUEUE	IN	8967/CHENP/2014	6/14/2013 Entry Date 12/12/2014	27/2016	7/1/2016	Published
A DISAMBIGUATION FREE OUT OF ORDER LOAD STORE QUEUE	KR	10-20157000678	6/14/2013 Entry Date 1/12/2015	10-20150027210 Unexamined	3/11/2015	Published
REORDERED SPECULATIVE INSTRUCTION SEQUENCES WITH A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	US	61/660,539	6/15/2012	N/A	N/A	Expired 6/15/2013

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REORDERED SPECULATIVE INSTRUCTION SEQUENCES WITH A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	TW	102121090	6/14/2013	TW201428616	7/16/2014	Published
REORDERED SPECULATIVE INSTRUCTION SEQUENCES WITH A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	PCT	PCT/US2013/045008	6/10/2013	WO/2013/188306	12/19/2013	Expired 12/15/2014
REORDERED SPECULATIVE INSTRUCTION SEQUENCES WITH A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	US	14/569,551	6/10/2013 Entry Date 12/12/2014	US 2015-0100766 A1	4/9/2015	Published
REORDERED SPECULATIVE INSTRUCTION SEQUENCES WITH A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	CN	201380043003.7	6/10/2013 Entry Date 2/12/2015	CN104583957	4/29/2015	Published
REORDERED SPECULATIVE INSTRUCTION SEQUENCES WITH A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	EP	13803665.2	6/10/2013 Entry Date 12/15/2014	EP2862068	4/22/2015	Published
REORDERED SPECULATIVE INSTRUCTION SEQUENCES WITH A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	IN	8968/CHENP/2014	6/10/2013 Entry Date 12/12/2014	27/2016	7/1/2016	Published
REORDERED SPECULATIVE INSTRUCTION SEQUENCES WITH A DISAMBIGUATION-FREE OUT OF ORDER LOAD STORE QUEUE	KR	10-20157000647	6/10/2013 Entry Date 1/12/2015	10-20150027208	3/11/2015	Published
INTERCONNECT STRUCTURE TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	US	61/488,683	5/20/2011	N/A	N/A	Expired 5/20/2012

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
GLOBAL AND LOCAL INTERCONNECT STRUCTURE COMPRISING ROUTING MATRIX TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	US	13/475,739	5/18/2012	US 2012-0297396 A1	11/22/2012	Granted
INTERCONNECT STRUCTURE TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	US	15/219,063	7/25/2016	N/A	N/A	Pending
AN INTERCONNECT STRUCTURE TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	TW	101117850	5/18/2012	TW201314462	4/1/2013	Granted
AN INTERCONNECT STRUCTURE TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	PCT	PCT/US2012/038713	5/18/2012	WO/2012/162189	11/29/2012	Expired 11/20/2013
AN INTERCONNECT STRUCTURE TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	CN	201280034725.1	5/18/2012 Entry Date 1/13/2014	CN103649931	3/19/2014	Granted
AN INTERCONNECT STRUCTURE TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	EP	12788989.7	5/18/2012 Entry Date 12/19/2013	EP2710480	3/26/2014	Published
AN INTERCONNECT STRUCTURE TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	IN	9176/CHENP/2013	5/18/2012 Entry Date 11/15/2013	50/2014	12/12/2014	Published

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AN INTERCONNECT STRUCTURE TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	KR	10-20137033566	5/18/2012 Entry Date 12/17/2013	10-20140030261 Unexamined	3/11/2014	Granted
DECENTRALLIZED ALLOCATION OF RESOURCES AND INTERCONNECT STRUCTURES TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	US	61/488,662	5/20/2011	N/A	N/A	Expired 5/20/2012
DECENTRALLIZED ALLOCATION OF RESOURCES AND INTERCONNECT STRUCTURES TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	TW	101117854	5/18/2012	TW201314463	4/1/2013	Published
DECENTRALLIZED ALLOCATION OF RESOURCES AND INTERCONNECT STRUCTURES TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	US	13/475,708	5/18/2012	US 2012-0297170 A1	11/22/2012	Allowed
DECENTRALLIZED ALLOCATION OF RESOURCES AND INTERCONNECT STRUCTURES TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	PCT	PCT/US2012/038711	5/18/2012	WO/2012/162188	11/29/2012	Expired 11/20/2013

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DECENTRALLIZED ALLOCATION OF RESOURCES AND INTERCONNECT STRUCTURES TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	CN	201280034739.3	5/18/2012 Entry Date 1/13/2014	CN103649932	3/19/2014	Published
DECENTRALLIZED ALLOCATION OF RESOURCES AND INTERCONNECT STRUCTURES TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	EP	12789667.8	5/18/2012 Entry Date 12/19/2013	EP2710481	3/26/2014	Published
DECENTRALLIZED ALLOCATION OF RESOURCES AND INTERCONNECT STRUCTURES TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	IN	9177/CHENP/2013	5/18/2012 Entry Date 11/15/2013	50/2014	12/12/2014	Published
DECENTRALLIZED ALLOCATION OF RESOURCES AND INTERCONNECT STRUCTURES TO SUPPORT THE EXECUTION OF INSTRUCTION SEQUENCES BY A PLURALITY OF ENGINES	KR	10-20137033565	5/18/2012 Entry Date 12/17/2013	10-20140030260 Unexamined	3/11/2014	Granted
EXECUTING INSTRUCTION SEQUENCE CODE BLOCKS BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	US	61/467,944	3/25/2011	N/A	N/A	Expired 3/25/2012

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EXECUTING INSTRUCTION SEQUENCE CODE BLOCKS BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	TW	101110082	3/23/2012	TW201305819	2/1/2013	Granted
EXECUTING INSTRUCTION SEQUENCE CODE BLOCKS BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	US	13/428,440	3/23/2012	US 2012-0246657 A1	9/27/2012	Published
EXECUTING INSTRUCTION SEQUENCE CODE BLOCKS BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	US	15/082,359	3/28/2016	US 2016-0210145 A1	7/21/2016	Published
EXECUTING INSTRUCTION SEQUENCE CODE BLOCKS BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	PCT	PCT/US2012/030360	3/23/2012	WO/2012/135031	10/4/2012	Expired 9/25/2013
EXECUTING INSTRUCTION SEQUENCE CODE BLOCKS BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	CN	201280024012.7	3/23/2012 Entry Date 11/18/2013	CN103547993	1/29/2014	Published
EXECUTING INSTRUCTION SEQUENCE CODE BLOCKS BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	EP	12764627.1	3/23/2012 Entry Date 9/19/2013	EP2689327	1/29/2014	Published
EXECUTING INSTRUCTION SEQUENCE CODE BLOCKS BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	IN	7380/CHENP/2013	3/23/2012 Entry Date 9/13/2013	25/2016	6/17/2016	Published

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EXECUTING INSTRUCTION SEQUENCE CODE BLOCKS BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	KR	10-20137027843	3/23/2012 Entry Date 10/22/2013	10-20140018947	2/13/2014	Granted
REGISTER FILE SEGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	US	61/467,939	3/25/2011	N/A	N/A	Expired 3/25/2012
REGISTER FILE SEGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	TW	101110086	3/21/2012	TW201305820	2/1/2013	Granted
REGISTER FILE SEGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	US	13/428,438	3/23/2012	US 2012-0246450 A1	9/27/2012	Published
REGISTER FILE SEGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	US	15/082,867	3/28/2016	US 2016-0210176 A1	7/21/2016	Published
REGISTER FILE SEGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	PCT	PCT/US2012/030383	3/23/2012	WO/2012/135041	10/4/2012	Expired 9/25/2013
REGISTER FILE SEGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	CN	201280024054.0	3/23/2012 Entry Date 11/18/2013	CN103562866	2/5/2014	Published

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REGISTER FILE SEGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	EP	12764838.4	3/23/2012 Entry Date 9/19/2013	EP2689330	1/29/2014	Published
REGISTER FILE SEGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	IN	7383/CHENP/2013	3/23/2012 Entry Date 9/13/2013	25/2016	6/17/2016	Published
REGISTER FILE SEGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	KR	10-20137027842	3/23/2012 Entry Date 10/22/2013	10-20140018946	2/13/2014	Granted
MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	US	61/467,940	03/25/2011	N/A	N/A	Expired 3/25/2012
MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	TW	101110092	3/23/2012	TW201303736	1/16/2013	Granted
MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	US	13/428,452	3/23/2012	US 2012-0246448 A1	9/27/2012	Granted
MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	US	15/019,920	2/9/2016	US 2016-0154653 A1	6/2/2016	Published

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MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	PCT	PCT/US2012/030409	3/23/2012	WO/2012/135050	10/4/2012	Expired 9/25/2013
MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	CN	201280024095.X	3/23/2012 Entry Date 11/18/2013	CN103635875	3/12/2014	Published
MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	EP	12763717.1	3/23/2012 Entry Date 10/25/2013	EP2689326	1/29/2014	Published
MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	IN	7466/CHENP/2013	3/23/2012 Entry Date 9/17/2013	45/2014	11/7/2014	Published
MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	KR	10-20137027841	3/23/2012 Entry Date 10/22/2013	10-20140018945	2/13/2014	Granted
MEMORY FRAGMENTS FOR SUPPORTING CODE BLOCK EXECUTION BY USING VIRTUAL CORES INSTANTIATED BY PARTITIONABLE ENGINES	KR	10-20167017150	3/23/2012 Entry Date 6/27/2016	10-20160084471 Unexamined	7/13/2016	Published
FAST UNALIGNED MEMORY ACCESS	PCT	PCT/US2011/057380	10/21/2011	WO/2013/058775	4/25/2013	Expired 4/21/2014
FAST UNALIGNED MEMORY ACCESS	US	14/376,825	10/21/2011 Entry Date 5/19/2015	US 2015-0248294 A1	9/3/2015	Published
FAST UNALIGNED MEMORY ACCESS	TW	100138451	10/24/2011	TW201317778	5/1/2013	Granted
CACHE REPLACEMENT POLICY	PCT	PCT/US2011/065584	12/16/2011	WO/2013/089786	6/20/2013	Expired 6/16/2014

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
CACHE REPLACEMENT POLICY	US	14/385,968	12/16/2011 Entry Date 5/7/2015	US 2015-0286576 A1	10/8/2015	Published
CACHE REPLACEMENT POLICY	TW	100147087	12/19/2011	TW201327159	7/1/2013	Published
METHODS AND SYSTEMS FOR MANAGING SYNONYMS IN VIRTUALLY INDEXED PHYSICALLY TAGGED CACHES	PCT	PCT/US2011/056757	10/18/2011	WO/2013/058745	4/25/2013	Expired 4/18/2014
METHODS AND SYSTEMS FOR MANAGING SYNONYMS IN VIRTUALLY INDEXED PHYSICALLY TAGGED CACHES	US	14/825,502	10/18/2011 Entry Date 8/13/2015	US 2016-0224471 A1	8/4/2016	Published
METHODS AND SYSTEMS FOR MANAGING SYNONYMS IN VIRTUALLY INDEXED PHYSICALLY TAGGED CACHES	TW	100138450	10/24/2011	TW201317782	5/1/2013	Granted
SYSTEMS AND METHODS FOR ACCESSING A UNIFIED TRANSLATION LOOKASIDE BUFFER	US	13/414,456	3/7/2012	US 2013-0238874 A1	9/12/2013	Granted
SYSTEMS AND METHODS FOR ACCESSING A UNIFIED TRANSLATION LOOKASIDE BUFFER	US	14/590,902	1/6/2015	US 2015-0301954 A1	10/22/2015	Granted
SYSTEMS AND METHODS FOR ACCESSING A UNIFIED TRANSLATION LOOKASIDE BUFFER	US	15/276,664	9/26/2016	N/A	N/A	Pending
SYSTEMS AND METHODS FOR ACCESSING A UNIFIED TRANSLATION LOOKASIDE BUFFER	PCT	PCT/US2013/029199	3/5/2013	WO/2013/134314	9/12/2013	Expired 9/7/2014
SYSTEMS AND METHODS FOR ACCESSING A UNIFIED TRANSLATION LOOKASIDE BUFFER	TW	102108112	3/7/2013	TW201403320	1/16/2014	Granted
SYSTEMS AND METHODS FOR SUPPORTING A PLURALITY OF LOAD ACCESSES OF A CACHE IN A SINGLE CYCLE	US	13/561,528	7/30/2012	US 2014-0032845 A1	1/30/2014	Granted

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
SYSTEMS AND METHODS FOR SUPPORTING A PLURALITY OF LOAD ACCESSES OF A CACHE IN A SINGLE CYCLE	US	14/922,053	10/23/2015	US 2016-0041930 A1	2/11/2016	Published
SYSTEMS AND METHODS FOR SUPPORTING A PLURALITY OF LOAD ACCESSES OF A CACHE IN A SINGLE CYCLE	TW	102127066	7/29/2013	TW201428494	7/16/2014	Granted
SYSTEMS AND METHODS FOR SUPPORTING A PLURALITY OF LOAD ACCESSES OF A CACHE IN A SINGLE CYCLE	PCT	PCT/US2013/051128	7/18/2013	WO/2014/022115	2/6/2014	Expired 1/30/2015
SYSTEMS AND METHODS FOR SUPPORTING A PLURALITY OF LOAD AND STORE ACCESSES OF A CACHE	US	13/561,570	7/30/2012	US 2014-0032846 A1	1/30/2014	Granted
SYSTEMS AND METHODS FOR SUPPORTING A PLURALITY OF LOAD AND STORE ACCESSES OF A CACHE	US	14/922,035	10/23/2015	US 2016-0041913 A1	2/11/2016	Published
SYSTEMS AND METHODS FOR MAINTAINING THE COHERENCY OF A STORE COALESCING CACHE AND A LOAD CACHE	US	13/561,441	7/30/2012	US 2014-0032856 A1	1/30/2014	Published
SYSTEMS AND METHODS FOR MAINTAINING THE COHERENCY OF A STORE COALESCING CACHE AND A LOAD CACHE	US	14/922,042	10/23/2015	US 2016-0041908 A1	2/11/2016	Published
SYSTEMS AND METHODS FOR FLUSHING A CACHE WITH MODIFIED DATA	US	13/561,491	7/30/2012	US 2014-0032844 A1	1/30/2014	Allowed
SYSTEMS AND METHODS FOR LOAD CANCELING IN A PROCESSOR THAT IS CONNECTED TO AN EXTERNAL INTERCONNECT FABRIC	US	13/649,505	10/11/2012	US 2014-0108729 A1	4/17/2014	Granted

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SYSTEMS AND METHODS FOR LOAD CANCELING IN A PROCESSOR THAT IS CONNECTED TO AN EXTERNAL INTERCONNECT FABRIC	US	15/244,873	8/23/2016	N/A	N/A	Pending
SYSTEMS AND METHODS FOR IMPLEMENTING WEAK STREAM SOFTWARE DATA AND INSTRUCTION PREFETCHING USING A HARDWARE DATA PREFETCHER	US	13/649,469	10/11/2012	US 2014-0108739 A1	4/17/2016	Granted
SYSTEMS AND METHODS FOR IMPLEMENTING WEAK STREAM SOFTWARE DATA AND INSTRUCTION PREFETCHING USING A HARDWARE DATA PREFETCHER	US	15/145,615	5/3/2016	US 2016-0246727 A1	8/25/2016	Published
SYSTEMS AND METHODS FOR NON-BLOCKING IMPLEMENTATION OF CACHE FLUSH INSTRUCTIONS	US	13/649,532	10/11/2012	US 2014-0108730 A1	4/17/2014	Allowed
SYSTEMS AND METHODS FOR NON-BLOCKING IMPLEMENTATION OF CACHE FLUSH INSTRUCTIONS	US	15/003,486	1/21/2016	US 2016-0140044 A1	5/19/2016	Published
MULTIPORT MEMORY CELL HAVING IMPROVED DENSITY AREA	US	61/800,885	3/15/2013	N/A	N/A	Expired 3/15/2014
MULTIPORT MEMORY CELL HAVING IMPROVED DENSITY AREA	US	14/216,855	3/17/2014	US 2015-0023086 A1	1/22/2015	Published
MULTIPORT MEMORY CELL HAVING IMPROVED DENSITY AREA	US	15/157,158	5/17/2016	US 2016-0260475 A1	9/8/2016	Published

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METHOD FOR EXECUTING BLOCKS OF INSTRUCTIONS USING A MICROPROCESSOR ARCHITECTURE HAVING A REGISTER VIEW, SOURCE VIEW, INSTRUCTION VIEW, AND A PLURALITY OF REGISTER TEMPLATES	US	61/799,902	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR USING REGISTER TEMPLATES TO TRACK INTERDEPENDENCIES AMONG BLOCKS OF INSTRUCTIONS	US	14/212,203	3/14/2014	US 2015-0046683 A1	2/12/2015	Published
METHOD FOR EXECUTING BLOCKS OF INSTRUCTIONS USING A MICROPROCESSOR ARCHITECTURE HAVING A REGISTER VIEW, SOURCE VIEW, INSTRUCTION VIEW, AND A PLURALITY OF REGISTER TEMPLATES	US	14/212,533	3/14/2014	US 2015-0046686 A1	2/12/2015	Published
METHOD FOR EXECUTING BLOCKS OF INSTRUCTIONS USING A MICROPROCESSOR ARCHITECTURE HAVING A REGISTER VIEW, SOURCE VIEW, INSTRUCTION VIEW, AND A PLURALITY OF REGISTER TEMPLATES	TW	103109504	3/14/2014	TW201504939	2/1/2015	Granted
A METHOD FOR EXECUTING BLOCKS OF INSTRUCTIONS USING A MICROPROCESSOR ARCHITECTURE HAVING A REGISTER VIEW, SOURCE VIEW, INSTRUCTION VIEW, AND A PLURALITY OF REGISTER TEMPLATES	PCT	PCT/US2014/024608	3/12/2014	WO/2014/150941	9/25/2014	Expired 9/15/2015

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A METHOD FOR EXECUTING BLOCKS OF INSTRUCTIONS USING A MICROPROCESSOR ARCHITECTURE HAVING A REGISTER VIEW, SOURCE VIEW, INSTRUCTION VIEW, AND A PLURALITY OF REGISTER TEMPLATES	CN	201480024463.X	3/12/2014 Entry Date 10/30/2015	CN105190541	12/23/2015	Published
A METHOD FOR EXECUTING BLOCKS OF INSTRUCTIONS USING A MICROPROCESSOR ARCHITECTURE HAVING A REGISTER VIEW, SOURCE VIEW, INSTRUCTION VIEW, AND A PLURALITY OF REGISTER TEMPLATES	EP	14769411.1	3/12/2014 Entry Date 9/15/2015	EP2972794	1/20/2016	Published
METHOD FOR EXECUTING BLOCKS OF INSTRUCTIONS USING A MICROPROCESSOR ARCHITECTURE HAVING A REGISTER VIEW, SOURCE VIEW, INSTRUCTION VIEW, AND A PLURALITY OF REGISTER TEMPLATES	IN	5500/CHENP/2015	3/12/2014 Entry Date 9/10/2015	27/2016	7/1/2016	Published
METHOD FOR EXECUTING BLOCKS OF INSTRUCTIONS USING A MICROPROCESSOR ARCHITECTURE HAVING A REGISTER VIEW, SOURCE VIEW, INSTRUCTION VIEW, AND A PLURALITY OF REGISTER TEMPLATES	KR	10-20157029262	3/12/2014 Entry Date 10/14/2015	10-20150132419	11/24/2015	Published
METHOD FOR POPULATING A SOURCE VIEW DATA STRUCTURE BY USING REGISTER TEMPLATE SNAPSHOTS	US	61/798,988	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR POPULATING A SOURCE VIEW DATA STRUCTURE BY USING REGISTER TEMPLATE SNAPSHOTS	US	14/213,115	3/14/2014	US 2014-0281426 A1	9/18/2014	Published

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METHOD FOR POPULATING REGISTER VIEW DATA STRUCTURE BY USING REGISTER TEMPLATE SNAPSHOTS	US	61/799,006	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR POPULATING REGISTER VIEW DATA STRUCTURE BY USING REGISTER TEMPLATE SNAPSHOTS	US	14/213,854	3/14/2014	US 2014-0281428 A1	9/18/2014	Allowed
A METHOD FOR POPULATING REGISTER VIEW DATA STRUCTURE BY USING REGISTER TEMPLATE SNAPSHOTS	TW	103109509	3/14/2014	TW201504940	2/1/2015	Granted
A METHOD FOR POPULATING REGISTER VIEW DATA STRUCTURE BY USING REGISTER TEMPLATE SNAPSHOTS	PCT	PCT/US2014/024276	3/12/2014	WO/2014/150806	9/25/2014	Expired 9/15/2015
METHOD FOR POPULATING AND INSTRUCTION VIEW DATA STRUCTURE BY USING REGISTER TEMPLATE SNAPSHOTS	US	61/799,299	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR POPULATING AND INSTRUCTION VIEW DATA STRUCTURE BY USING REGISTER TEMPLATE SNAPSHOTS	US	14/214,045	3/14/2014	US 2014-0281412 A1	9/18/2014	Published
METHOD FOR DEPENDENCY BROADCASTING THROUGH A BLOCK ORGANIZED SOURCE VIEW DATA STRUCTURE	US	61/799,530	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR DEPENDENCY BROADCASTING THROUGH A BLOCK ORGANIZED SOURCE VIEW DATA STRUCTURE	US	14/216,859	3/17/2014	US 2014-0282601 A1	9/18/2014	Published
A METHOD FOR DEPENDENCY BROADCASTING THROUGH A BLOCK ORGANIZED SOURCE VIEW DATA STRUCTURE	TW	103109519	3/14/2014	TW201510870	3/16/2015	Granted

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A METHOD FOR DEPENDENCY BROADCASTING THROUGH A BLOCK ORGANIZED SOURCE VIEW DATA STRUCTURE	PCT	PCT/US2014/024677	3/12/2014	WO/2014/150971	9/25/2014	Expired 9/15/2015
METHOD FOR DEPENDENCY BROADCASTING THROUGH A SOURCE ORGANIZED SOURCE VIEW DATA STRUCTURE	US	61/799,407	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR DEPENDENCY BROADCASTING THROUGH A SOURCE ORGANIZED SOURCE VIEW DATA STRUCTURE	US	14/213,135	3/14/2014	US 2014-0282601 A1	9/18/2014	Allowed
METHOD FOR IMPLEMENTING A REDUCED SIZE REGISTER VIEW DATA STRUCTURE IN A MICROPROCESSOR	US	61/799,736	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR IMPLEMENTING A REDUCED SIZE REGISTER VIEW DATA STRUCTURE IN A MICROPROCESSOR	US	14/213,692	3/14/2014	US 2014-0281427 A1	9/18/2014	Published
A METHOD FOR IMPLEMENTING A REDUCED SIZE REGISTER VIEW DATA STRUCTURE IN A MICROPROCESSOR	TW	103109513	3/14/2014	TW201504943	2/1/2015	Granted
A METHOD FOR IMPLEMENTING A REDUCED SIZE REGISTER VIEW DATA STRUCTURE IN A MICROPROCESSOR	PCT	PCT/US2014/024722	3/12/2014	WO/2014/150991	9/25/2014	Expired 9/15/2015
METHOD FOR IMPLEMENTING A REDUCED SIZE REGISTER VIEW DATA STRUCTURE IN A MICROPROCESSOR	US	61/799,892	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR IMPLEMENTING A REDUCED SIZE REGISTER VIEW DATA STRUCTURE IN A MICROPROCESSOR	US	14/214,176	3/14/2014	US 2014-0281416 A1	9/18/2014	Published

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METHOD FOR EXECUTING MULTITHREADED INSTRUCTIONS GROUPED INTO BLOCKS	US	61/800,123	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR EXECUTING MULTITHREADED INSTRUCTIONS GROUPED INTO BLOCKS	US	14/214,280	3/14/2014	US 2014-0282592 A1	9/18/2014	Published
METHOD FOR EXECUTING MULTITHREADED INSTRUCTIONS GROUPED INTO BLOCKS	TW	103109479	3/14/2014	TW201504948	2/1/2015	Pending
A METHOD FOR EXECUTING MULTITHREADED INSTRUCTIONS GROUPED INTO BLOCKS	PCT	PCT/US2014/024775	3/12/2014	WO/2014/151018	9/25/2014	Expired 9/15/2015
A METHOD FOR EXECUTING MULTITHREADED INSTRUCTIONS GROUPED INTO BLOCKS	CN	20148002452.8	3/15/2013 Entry Date 10/30/2015	CN105210040	12/30/2015	Published
METHOD FOR EXECUTING MULTITHREADED INSTRUCTIONS GROUPED INTO BLOCKS	EP	14769450.9	3/12/2014 Entry Date 10/13/2015	EP2972845	1/20/2016	Published
METHOD FOR EXECUTING MULTITHREADED INSTRUCTIONS GROUPED INTO BLOCKS	IN	5509/CHENP/2015	3/12/2014 Entry Date 9/11/2015	27/2016	7/1/2016	Published
METHOD FOR EXECUTING MULTITHREADED INSTRUCTIONS GROUPED INTO BLOCKS	KR	10-20157028745	3/12/2014 Entry Date 10/12/2015	10-20150128968 Unexamined	11/18/2015	Published
METHOD FOR PERFORMING DUAL DISPATCH OF BLOCKS AND HALF BLOCKS	US	61/800,179	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR PERFORMING DUAL DISPATCH OF BLOCKS AND HALF BLOCKS	US	14/213,218	3/14/2014	US 2014-0317387 A1	10/23/2014	Published

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METHOD FOR EMULATING A GUEST CENTRALIZED FLAG ARCHITECTURE BY USING A NATIVE STUPID FLAG ARCHITECTURE	US	61/800,487	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR EMULATING A GUEST CENTRALIZED FLAG ARCHITECTURE BY USING A NATIVE DISTRIBUTED FLAG ARCHITECTURE	US	14/213,730	3/14/2014	US 2014-0281436 A1	9/18/2014	Published
A METHOD FOR EMULATING A GUEST CENTRALIZED FLAG ARCHITECTURE BY USING A NATIVE DISTRIBUTED FLAG ARCHITECTURE	TW	103109493	3/14/2014	TW201504942	2/1/2015	Granted
A METHOD FOR EMULATING A GUEST CENTRALIZED FLAG ARCHITECTURE BY USING A NATIVE DISTRIBUTED FLAG ARCHITECTURE	PCT	PCT/US2014/024828	3/12/2014	WO/2014/151043	9/25/2014	Expired 9/15/2015
A METHOD FOR EMULATING A GUEST CENTRALIZED FLAG ARCHITECTURE BY USING A NATIVE DISTRIBUTED FLAG ARCHITECTURE	CN	201480024832.5	3/12/2014 Entry Date 11/02/2015	CN105247484	1/13/2016	Published
A METHOD FOR EMULATING A GUEST CENTRALIZED FLAG ARCHITECTURE BY USING A NATIVE DISTRIBUTED FLAG ARCHITECTURE	EP	14770976.0	3/12/2014 Entry Date 9/17/2015	EP2972836	1/20/2016	Published
A METHOD FOR EMULATING A GUEST CENTRALIZED FLAG ARCHITECTURE BY USING A NATIVE DISTRIBUTED FLAG ARCHITECTURE	IN	5551/CHENP/2015	3/12/2014 Entry Date 9/11/2015	27/2016	7/1/2016	Published
A METHOD FOR EMULATING A GUEST CENTRALIZED FLAG ARCHITECTURE BY USING A NATIVE DISTRIBUTED FLAG ARCHITECTURE	KR	10-20157029107	3/12/2014 Entry Date 10/13/2015	10-20150130510	11/23/2015	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
METHOD AND APPARATUS FOR PREDICTING FORWARDING OF DATA FROM A STORE TO A LOAD	US	61/793,466	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS FOR PREDICTING FORWARDING OF DATA FROM A STORE TO A LOAD	US	14/063,173	10/25/2013	US 2014-0281408 A1	9/18/2014	Published
METHOD FOR PREDICTING FORWARDING OF DATA FROM A STORE TO A LOAD	US	14/063,409	10/25/2013	US 2014-0281384 A1	9/18/2014	Published
METHOD AND APPARATUS FOR PREVENTING NON-TEMPORAL ENTRIES FROM POLLUTING SMALL STRUCTURES USING A TRANSIENT BUFFER	US	61/793,042	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS FOR PREVENTING NON-TEMPORAL ENTRIES FROM POLLUTING SMALL STRUCTURES USING A TRANSIENT BUFFER	US	14/182,618	2/18/2014	US 2014-0317351 A1	10/23/2014	Published
METHOD AND APPARATUS TO ALLOW EARLY DEPENDENCY RESOLUTION AND DATA FORWARDING IN A MICROPROCESSOR	US	61/792,676	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS TO ALLOW EARLY DEPENDENCY RESOLUTION AND DATA FORWARDING IN A MICROPROCESSOR	US	14/211,476	3/14/2014	US 2014-0281410 A1	9/18/2014	Published
METHOD AND APPARATUS TO ALLOW EARLY DEPENDENCY RESOLUTION AND DATA FORWARDING IN A MICROPROCESSOR	TW	103109878	3/17/2014	TW201502981	1/16/2015	Granted
METHOD AND APPARATUS TO ALLOW EARLY DEPENDENCY RESOLUTION AND DATA FORWARDING IN A MICROPROCESSOR	PCT	PCT/US2014/026176	3/13/2014	WO/2014/151652	9/25/2014	Expired 9/15/2015

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
METHOD AND APPARATUS FOR NEAREST POTENTIAL STORE TAGGING	US	61/792,885	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS FOR NEAREST POTENTIAL STORE TAGGING	US	14/209,736	3/13/2014	US 2014-0281409 A1	9/18/2014	Published
METHOD AND APPARATUS FOR GUEST RETURN ADDRESS STACK EMULATION SUPPORTING SPECULATION	US	61/793,174	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS FOR GUEST RETURN ADDRESS STACK EMULATION SUPPORTING SPECULATION	US	14/211,655	3/14/2014	US 2014-0281388 A1	9/18/2014	Published
METHOD AND APPARATUS FOR GUEST RETURN ADDRESS STACK EMULATION SUPPORTING SPECULATION	TW	103109877	3/17/2014	TW201506783	2/16/2015	Granted
METHOD AND APPARATUS FOR GUEST RETURN ADDRESS STACK EMULATION SUPPORTING SPECULATION	PCT	PCT/US2014/026252	3/13/2014	WO/2014/151691	9/25/2014	Expired 9/15/2015
METHOD AND APPARATUS FOR GUEST RETURN ADDRESS STACK EMULATION SUPPORTING SPECULATION	CN	20148002170.3	3/13/2014 Entry Date 10/16/2015	CN105122206	12/2/2015	Published
METHOD AND APPARATUS FOR GUEST RETURN ADDRESS STACK EMULATION SUPPORTING SPECULATION	EP	14770972.9	3/13/2014 Entry Date 9/15/2015	EP2972798	1/20/2016	Published
METHOD AND APPARATUS FOR GUEST RETURN ADDRESS STACK EMULATION SUPPORTING SPECULATION	IN	5510/CHENP/2015	3/13/2014 Entry Date 9/11/2015	27/2016	7/1/2016	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
METHOD AND APPARATUS FOR GUEST RETURN ADDRESS STACK EMULATION SUPPORTING SPECULATION	KR	10-20157029321	3/13/2014 Entry Date 10/14/2015	10-20150132431 Unexamined	11/25/2015	Published
METHOD AND APPARATUS TO AVOID DEADLOCK DURING INSTRUCTION SCHEDULING USING DYNAMIC PORT REMAPPING	US	61/793,541	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS TO AVOID DEADLOCK DURING INSTRUCTION SCHEDULING USING DYNAMIC PORT REMAPPING	US	14/101,615	12/10/2013	US 2014-0282575 A1	12/10/2013	Allowed
METHOD AND APPARTUS TO AVOID DEADLOCK DURING INSTRUCTION SCHEDULING USING DYNAMIC PORT REMAPPING	US	15/219,119	7/25/2016	N/A	N/A	Pending
METHOD AND APPARTUS TO AVOID DEADLOCK DURING INSTRUCTION SCHEDULING USING DYNAMIC PORT REMAPPING	TW	103109486	3/14/2014	TW201504941	2/1/2015	Granted
METHOD AND APPARATUS TO AVOID DEADLOCK DURING INSTRUCTION SCHEDULING USING DYNAMIC PORT REMAPPING	PCT	PCT/US2014/027200	3/14/2014	WO/2014/152315	9/25/2014	Expired 9/15/2015
METHOD AND APPARATUS TO AVOID DEADLOCK DURING INSTRUCTION SCHEDULING USING DYNAMIC PORT REMAPPING	CN	201480024939.X	3/14/2014 Entry Date 11/02/2015	CN105190539	12/23/2015	Published
METHOD AND APPARATUS TO AVOID DEADLOCK DURING INSTRUCTION SCHEDULING USING DYNAMIC PORT REMAPPING	EP	14770080.1	3/14/2014 Entry Date 9/15/2015	EP2972783	1/20/2016	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
METHOD AND APPARATUS TO AVOID DEADLOCK DURING INSTRUCTION SCHEDULING USING DYNAMIC PORT REMAPPING	IN	5511/CHENP/2015	3/14/2014 Entry Date 9/11/2015	27/2016	7/1/2016	Published
METHOD AND APPARATUS TO AVOID DEADLOCK DURING INSTRUCTION SCHEDULING USING DYNAMIC PORT REMAPPING	KR	10-20157028638	3/14/2014 Entry Date 10/12/2015	10-20150128958 Unexamined	11/18/2015	Published
METHOD AND APPARATUS FOR EFFICIENT SCHEDULING FOR ASYMMETRICAL EXECUTION UNITS	US	61/799,062	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS FOR EFFICIENT SCHEDULING FOR ASYMMETRICAL EXECUTION UNITS	US	14/107,116	12/16/2013	US 2014-0373022 A1	12/18/2014	Published
METHOD AND APPARATUS FOR EFFICIENT SCHEDULING FOR ASYMMETRICAL EXECUTION UNITS	TW	103109880	3/17/2014	TW201506784	2/16/2015	Granted
METHOD AND APPARATUS FOR EFFICIENT SCHEDULING FOR ASYMMETRICAL EXECUTION UNITS	PCT	PCT/US2014/027252	3/14/2014	WO/2014/152359	9/25/2014	Expired 9/15/2015
METHOD AND APPARATUS FOR EFFICIENT SCHEDULING FOR ASYMMETRICAL EXECUTION UNITS	CN	201480021706.4	3/14/2014 Entry Date 10/16/2015	CN105122211	12/2/2015	Published
METHOD AND APPARATUS FOR EFFICIENT SCHEDULING FOR ASYMMETRICAL EXECUTION UNITS	EP	14768312.2	3/14/2014 Entry Date 9/17/2015	EP2972844	1/20/2016	Published
METHOD AND APPARATUS FOR EFFICIENT SCHEDULING FOR ASYMMETRICAL EXECUTION UNITS	IN	5548/CHENP/2015	3/14/2014 Entry Date 9/11/2015	27/2016	7/1/2016	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
METHOD AND APPARATUS FOR EFFICIENT SCHEDULING FOR ASYMMETRICAL EXECUTION UNITS	KR	10-20157028996	3/14/2014 Entry Date 10/13/2015	10-20150132356	11/25/2015	Published
METHOD AND APPARATUS FOR A WIDE AND EFFICIENT FRONT-END TO EMULATE A GUEST-ARCHITECTURE	US	61/799,717	3/15/2013	N/A	N/A	Expired 3/15/2014
METHODS, SYSTEMS AND APPARATUS FOR SUPPORTING WIDE AND EFFICIENT FRONT-END OPERATION WITH GUEST-ARCHITECTURE EMULATION	US	14/216,493	3/17/2014	US 2014-0282546 A1	9/18/2014	Published
METHOD AND APPARATUS FOR PREDICTING THE WAY OF SET ASSOCIATIVE SHADOW CACHE	US	61/793,703	3/15/2013	N/A	N/A	Expired 3/15/2014
METHODS, SYSTEMS AND APPARATUS FOR PREDICTING THE WAY OF A SET ASSOCIATIVE CACHE	US	14/215,633	3/17/2014	US 2014-0281242 A1	9/18/2014	Allowed
METHODS, SYSTEMS AND APPARATUS FOR PREDICTING THE WAY OF A SET ASSOCIATIVE CACHE	US	15/257,593	9/6/2016	N/A	N/A	Pending
METHOD AND APPARATUS TO SPEED UP THE LOAD ACCESS AND DATA RETURN SPEED PATH USING EARLY CALCULATED LOWER ADDRESS BITS	US	61/799,116	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS TO SPEED UP THE LOAD ACCESS AND DATA RETURN SPEED PATH USING EARLY LOWER ADDRESS BITS	US	14/211,878	3/14/2014	US 2014-0281116 A1	9/18/2014	Published
METHOD AND APPARATUS TO INCREASE THE SPEED OF THE LOAD ACCESS AND DATA RETURN SPEED PATH USING EARLY LOWER ADDRESS BITS	US	14/281,663	5/19/2014	US 2014-0304492 A1	10/9/2014	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
METHOD AND APPARATUS FOR SORTING ELEMENTS IN HARDWARE STRUCTURES	US	61/793,752	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS FOR SORTING ELEMENTS IN HARDWARE STRUCTURES	US	14/052,571	10/11/2013	US 2014-0281422 A1	9/18/2014	Granted
METHOD AND APPARATUS FOR SORTING ELEMENTS IN HARDWARE STRUCTURES	US	15/215,004	7/20/2016	N/A	N/A	Pending
METHOD AND APPARATUS FOR SORTING ELEMENTS IN HARDWARE STRUCTURES	TW	103109881	3/17/2014	TW201510857	3/16/2015	Published
METHOD AND APPARATUS FOR SORTING ELEMENTS IN HARDWARE STRUCTURES	PCT	PCT/US2014/026312	3/13/2014	WO/2014/151722	9/25/2014	Expired 9/15/2015
SYSTEMS AND METHODS FOR SUPPORTING A PLURALITY OF LOAD ACCESSES OF A CACHE IN A SINGLE CYCLE TO MAINTAIN THROUGHPUT	US	61/800,498	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD AND APPARATUS FOR SUPPORTING A PLURALITY OF LOAD ACCESSES OF A CACHE IN A SINGLE CYCLE TO MAINTAIN THROUGHPUT	US	14/173,602	2/5/2014	US 2014-0156947 A1	6/5/2014	Published
METHOD FOR IMPLEMENTING A LINE SPEED INTERCONNECT STRUCTURE	US	61/852,389	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR IMPLEMENTING A LINE SPEED INTERCONNECT STRUCTURE	US	14/213,909	3/14/2014	US 2014-0269753 A1	9/18/2014	Published
A METHOD FOR IMPLEMENTING A LINE SPEED INTERCONNECT STRUCTURE	TW	103109879	3/17/2014	TW201502994	1/16/2015	Published
A METHOD FOR IMPLEMENTING A LINE SPEED INTERCONNECT STRUCTURE	PCT	PCT/US2014/026427	3/13/2014	WO/2014/151773	9/25/2014	Expired 9/15/2015

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
A METHOD FOR IMPLEMENTING A LINE SPEED INTERCONNECT STRUCTURE	CN	201480024465.9	3/13/2014 Entry Date 10/30/2015	CN105190579	12/23/2015	Published
A METHOD FOR IMPLEMENTING A LINE SPEED INTERCONNECT STRUCTURE	EP	14768040.9	3/13/2014 Entry Date 9/17/2015	EP2972912	1/20/2016	Published
A METHOD FOR IMPLEMENTING A LINE SPEED INTERCONNECT STRUCTURE	IN	5550/CHENP/2015	3/13/2014 Entry Date 9/11/2015	27/2016	7/1/2016	Published
A METHOD FOR IMPLEMENTING A LINE SPEED INTERCONNECT STRUCTURE	KR	10-20157028995	3/13/2014 Entry Date 10/13/2015	10-20150132355	11/25/2015	Published
METHOD FOR A DELAYED BRANCH IMPLEMENTATION BY USING A FRONT END TRACK TABLE	US	61/852,057	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR A DELAYED BRANCH IMPLEMENTATION BY USING A FRONT END TRACK TABLE	US	14/216,683	3/17/2014	US 2014-0281438 A1	9/18/2014	Published
METHOD FOR A STAGED OPTIMIZED HIGH-SPEED ADDER	US	61/852,338	3/15/2013	N/A	N/A	Expired 3/15/2014
METHOD FOR A STAGED OPTIMIZED HIGH-SPEED ADDER	US	14/214,049	3/14/2014	US 2014-0324937 A1	10/30/2014	Published
SYSTEMS AND METHODS FOR ACQUIRING DATA FOR LOADS AT DIFFERENT ACCESS TIMES FROM HIERARCHICAL SOURCES USING A LOAD QUEUE AS A TEMPORARY STORAGE BUFFER AND COMPLETING THE LOAD EARLY	US	13/970,277	8/19/2013	US 2015-0052303 A1	2/19/2015	Published
SYSTEMS AND METHODS FOR FASTER READ AFTER WRITE FORWARDING USING A VIRTUAL ADDRESS	US	14/015,086	8/30/2013	US 2015-0067230 A1	3/5/2015	Granted
SYSTEMS AND METHODS FOR FASTER READ AFTER WRITE FORWARDING USING A VIRTUAL ADDRESS	US	14/819,255	8/5/2015	US 2015-0339238 A1	11/26/2015	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
SYSTEMS AND METHODS FOR READ REQUEST BYPASSING A LAST LEVEL CACHE THAT INTERFACES WITH AN EXTERNAL FABRIC	US	13/970,311	8/19/2013	US 2015-0052304 A1	2/19/2015	Published
SYSTEMS AND METHODS FOR INVASIVE DEBUG OF A PROCESSOR WITHOUT PROCESSOR EXECUTION OF INSTRUCTIONS	US	13/970,344	8/19/2013	US 2015-0052401 A1	2/19/2015	Published
METHOD AND APPARATUS FOR PROVIDING HARDWARE SUPPORT FOR SELF-MODIFYING CODE	US	61/991,951	5/12/2014	N/A	N/A	Expired 5/12/2015
METHOD AND APPARATUS FOR PROVIDING HARDWARE SUPPORT FOR SELF-MODIFYING CODE	US	14/710,372	5/12/2015	US 2015-0324213 A1	11/12/2015	Published
METHOD AND APPARATUS FOR PROVIDING HARDWARE SUPPORT FOR SELF-MODIFYING CODE	PCT	PCT/US2015/030411	5/12/2015	WO/2015/175555	11/19/2015	Published
A RUNTIME ARCHITECTURE FOR EFFICIENTLY OPTIMIZING AND EXECUTING GUEST CODE AND CONVERTING TO NATIVE CODE	US	62/029,383	7/25/2014	N/A	N/A	Expired 7/25/2015
USING A PLURALITY OF CONVERSION TABLES TO IMPLEMENT AN INSTRUCTION SET AGNOSTIC RUNTIME ARCHITECTURE	US	14/806,169	7/22/2015	US 2016-0026482 A1	1/28/2016	Published
USING A PLURALITY OF CONVERSION TABLES TO IMPLEMENT AN INSTRUCTION SET AGNOSTIC RUNTIME ARCHITECTURE	PCT	PCT/US2015/041847	7/23/2015	WO/2016/014863	1/28/2016	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
AN ALLOCATION AND ISSUE STAGE FOR REORDERING A MICROINSTRUCTION SEQUENCE INTO AN OPTIMIZED MICROINSTRUCTION SEQUENCE TO IMPLEMENT AN INSTRUCTION SET AGNOSTIC RUNTIME ARCHITECTURE	US	14/807,141	7/23/2015	US 2016-0026486 A1	1/28/2016	Published
AN ALLOCATION AND ISSUE STAGE FOR REORDERING A MICROINSTRUCTION SEQUENCE INTO AN OPTIMIZED MICROINSTRUCTION SEQUENCE TO IMPLEMENT AN INSTRUCTION SET AGNOSTIC RUNTIME ARCHITECTURE	PCT	PCT/US2015/042002	7/24/2015	WO/2016/014951	1/28/2016	Published
SYSTEM FOR AN INSTRUCTION SET AGNOSTIC RUNTIME ARCHITECTURE	US	14/807,271	7/23/2015	US 2016-0026483 A1	01-28-2016	Published
SYSTEM FOR AN INSTRUCTION SET AGNOSTIC RUNTIME ARCHITECTURE	PCT	PCT/US2015/041850	7/23/2015	WO/2016/014866	1/28/2016	Published
SYSTEM CONVERTER THAT IMPLEMENTS A REORDERING PROCESS THROUGH JIT (JUST IN TIME) OPTIMIZATION THAT ENSURES LOADS DO NOT DISPATCH AHEAD OF OTHER LOADS THAT ARE TO THE SAME ADDRESS	US	14/807,308	7/23/2015	US 2016-0026444 A1	1/28/2016	Published
SYSTEM CONVERTER THAT IMPLEMENTS A REORDERING PROCESS THROUGH JIT(JUST IN TIME) OPTIMIZATION THAT ENSURES LOADS DO NOT DISPATCH AHEAD OF OTHER LOADS THAT ARE TO THE SAME ADDRESS	PCT	PCT/US2015/042019	7/24/2015	WO/2016/014956	1/28/2016	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
USING A CONVERSION LOOK ASIDE BUFFER TO IMPLEMENT AN INSTRUCTION SET AGNOSTIC RUNTIME ARCHITECTURE	US	14/807,313	7/23/2015	US 2016-0026487 A1	1/28/2016	Published
USING A CONVERSION LOOK ASIDE BUFFER TO IMPLEMENT AN INSTRUCTION SET AGNOSTIC RUNTIME ARCHITECTURE	PCT	PCT/US2015/041851	7/23/2015	WO/2016/014867	1/28/2016	Published
SYSTEM CONVERTER THAT EXECUTES A JUST IN TIME OPTIMIZER FOR EXECUTING CODE FROM A GUEST IMAGE	US	14/807,343	7/23/2015	US 2016-0026484 A1	1/28/2016	Published
A SYSTEM CONVERTER THAT EXECUTES A JUST IN TIME OPTIMIZER FOR EXECUTING CODE FROM A GUEST IMAGE	PCT	PCT/US2015/042010	7/24/2015	WO/2016/014953	1/28/2016	Published
SYSTEM CONVERTER THAT IMPLEMENTS A RUN AHEAD RUN TIME GUEST INSTRUCTION CONVERSION/DECODIN G PROCESS AND A PREFETCHING PROCESS WHERE GUEST CODE IS PRE-FETCHED FROM THE TARGET OF GUEST BRANCHES IN AN INSTRUCTION SEQUENCE	US	14/807,353	7/23/2015	US 2016-0026445 A1	1/28/2016	Published
A SYSTEM CONVERTER THAT IMPLEMENTS A RUN AHEAD RUN TIME GUEST INSTRUCTION CONVERSION/DECODIN G PROCESS AND A PREFETCHING PROCESS WHERE GUEST CODE IS PRE-FETCHED FROM THE TARGET OF GUEST BRANCHES IN AN INSTRUCTION SEQUENCE	PCT	PCT/US2015/042032	7/24/2015	WO/2016/014962	1/28/2016	Published
METHODS AND SYSTEMS FOR TRACKING ADDRESSES STORED IN NON-HOME CACHE LOCATIONS	US	14/515,333	10/15/2014	US 2016-0110294 A1	4/21/2016	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
SYSTEMS AND METHODS FOR MANAGING INTER-CPU INTERRUPTS BETWEEN MULTIPLE CPUS	US	14/515,379	10/15/2014	N/A	N/A	Pending
SYSTEMS AND METHODS FOR INVALIDATING DIRECTORY OF NON-HOME LOCATIONS WAYS	US	14/515,345	10/15/2014	US 2016-0110293 A1	4/21/2016	Published
APPARATUS AND METHOD SUPPORTING CODE OPTIMIZATION	US	62/367,537	7/27/2016	N/A	N/A	Pending
SYSTEM AND METHOD FOR MULTIPLEXING VECTOR MASK	US	62/367,553	7/27/2016	N/A	N/A	Pending
SYSTEM AND METHOD FOR MULTIPLEXING VECTOR COMPARES	US	62/367,558	7/27/2016	N/A	N/A	Pending
ULTRA LARGE INSTRUCTION BLOCK ARCHITECTURE (ULIB)	US	60/791,782	4/12/2006	N/A	N/A	Expired 4/12/2007
TIME-LAG SLICED ARCHITECTURE (TLSA)	US	60/791,649	4/12/2006	N/A	N/A	Expired 4/12/2007
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	PCT	PCT/US2007/066536	4/12/2007	WO/2007/143278	12/13/2007	Expired 10/12/2008
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	CN	200780017317.4	4/12/2007 Entry Date 11/12/2008	CN101449256	6/3/2009	Granted
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	CN	201310589048.6	4/12/2007	CN103646009	3/19/2014	Granted
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	EP	07811845.2	4/12/2007	EP2011018	1/7/2009	Granted

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	DE	07811845.2	4/12/2007	EP2011018	1/7/2009	Granted
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	GB	07811845.2	4/12/2007	EP2011018	1/7/2009	Granted
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	NL	07811845.2	4/12/2007	EP2011018	1/7/2009	Granted
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	IN	4129/KOLNP/2008	4/12/2007 Entry Date 10/13/2008	10/2009	3/6/2009	Published
A METHOD AND APPARATUS FOR PROCESSING COMPUTER INSTRUCTIONS	IN	51/KOLNP/2012	4/12/2007	8/2014	2/21/2014	Published
PLURAL MATRICES OF EXECUTION UNITS FOR PROCESSING MATRICES OF ROW DEPENDENT INSTRUCTIONS IN SINGLE CLOCK CYCLE IN SUPER OR SEPARATE MODE	US	12/296,919	4/12/2007 Entry Date 12/19/2008	US 2009-0113170 A1	4/30/2009	Granted
PROCESSOR EXECUTING SUPER INSTRUCTION MATRIX WITH REGISTER FILE CONFIGURABLE FOR SINGLE OR MULTIPLE THREADS OPERATIONS	US	13/691,609	11/30/2012	US 2013-0091340 A1	4/11/2013	Granted
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	US	14/733,827	6/8/2015	US 2015-0269118 A1	9/24/2015	Published

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	EP	12150513.5	4/12/2007	EP2477109	7/18/2012	Granted
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	GB	12150513.5	4/12/2007	EP2477109	7/18/2012	Granted
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	NL	12150513.5	4/12/2007	EP2477109	7/18/2012	Granted
APPARATUS AND METHOD FOR PROCESSING AN INSTRUCTION MATRIX SPECIFYING PARALLEL AND DEPENDENT OPERATIONS	DE	12150513.5	4/12/2007	EP2477109	7/18/2012	Granted
PROCESSOR ARCHITECTURE AND METHODS	US	60/792,219	4/14/2006	N/A	N/A	Expired 4/14/2007
EFFICIENT CONTEXT SWITCH ARCHITECTURE	US	60/865,813	11/14/2006	N/A	N/A	Expired 11/14/2007
SELF-GENERATING AND SYNCHRONIZING DYNAMIC AND STATIC THREADING ARCHITECTURE	US	60/865,816	11/14/2006	N/A	N/A	Expired 11/14/2007
UNIFIED ARCHITECTURE FOR DYNAMIC GENERATION, EXECUTION, SYNCHRONIZATION AND PARALLELIZATION OF COMPLEX INSTRUCTION FORMATS	US	60/865,818	11/14/2006	N/A	N/A	Expired 11/14/2007
VIRTUAL REGISTER FILE, REGISTER CACHE AND REGISTER FILE HIERARCHY FOR UNIFIED PARALLEL ARCHITECTURES	US	60/865,820	11/14/2006	N/A	N/A	Expired 11/14/2007

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
APPARATUS AND METHOD FOR PROCESSING INSTRUCTIONS IN A MULTI-THREADED ARCHITECTURE USING CONTEXT SWITCHING	PCT	PCT/US2007/084710	11/14/2007	WO/2008/061154	5/22/2008	Expired 5/14/2009
APPARATUS AND METHOD FOR PROCESSING COMPLEX INSTRUCTION FORMATS IN A MULTI-THREADED ARCHITECTURE SUPPORTING VARIOUS CONTEXT SWITCH MODES AND VIRTUALIZATION SCHEMES	CN	200780046679.6	11/14/2007	CN101627365	1/13/2010	Published
APPARATUS AND METHOD FOR PROCESSING INSTRUCTIONS IN A MULTI-THREADED ARCHITECTURE USING CONTEXT SWITCHING	IN	1939/KOLNP/2009	11/14/2007 Entry date 5/22/2009	25/2009	6/19/2009	Published
PARALLEL PROCESSING OF A SEQUENTIAL PROGRAM USING HARDWARE GENERATED THREADS AND THEIR INSTRUCTION GROUPS EXECUTING ON PLURAL EXECUTION UNITS AND ACCESSING REGISTER FILE SEGMENTS USING DEPENDENCY INHERITANCE VECTORS ACROSS MULTIPLE ENGINES	US	12/514,303	11/14/2007 Entry date 1/5/2010	US 2010-0161948 A1	6/24/2010	Granted
CACHE STORING DATA FETCHED BY ADDRESS CALCULATING LOAD INSTRUCTION WITH LABEL USED AS ASSOCIATED NAME FOR CONSUMING INSTRUCTION TO REFER	US	14/194,589	2/28/2014	US 2014-0181475 A1	6/26/2014	Allowed; issue fee due 10/27/16
APPARATUS AND METHOD FOR PROCESSING INSTRUCTIONS IN A MULTI-THREADED ARCHITECTURE USING CONTEXT SWITCHING	EP	07864410.1	11/14/2007	EP2122461	11/25/2009	Abandoned 2/12/2014

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
APPARATUS AND METHOD FOR PROCESSING COMPLEX INSTRUCTION FORMATS IN A MULTI-THREADED ARCHITECTURE SUPPORTING VARIOUS CONTEXT SWITCH MODES AND VIRTUALIZATION SCHEMES	EP	12174228.2	11/14/2007	EP2523101	11/14/2012	Granted
APPARATUS AND METHOD FOR PROCESSING COMPLEX INSTRUCTION FORMATS IN A MULTI-THREADED ARCHITECTURE SUPPORTING VARIOUS CONTEXT SWITCH MODES AND VIRTUALIZATION SCHEMES	DE	12174228.2	11/14/2007	EP2523101	11/14/2012	Granted
APPARATUS AND METHOD FOR PROCESSING COMPLEX INSTRUCTION FORMATS IN A MULTI-THREADED ARCHITECTURE SUPPORTING VARIOUS CONTEXT SWITCH MODES AND VIRTUALIZATION SCHEMES	FR	12174228.2	11/14/2007	EP2523101	11/14/2012	Granted
APPARATUS AND METHOD FOR PROCESSING COMPLEX INSTRUCTION FORMATS IN A MULTI-THREADED ARCHITECTURE SUPPORTING VARIOUS CONTEXT SWITCH MODES AND VIRTUALIZATION SCHEMES	GB	12174228.2	11/14/2007	EP2523101	11/14/2012	Granted

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Title	Country of Filing	Serial #	Filing Date	Publication #	Publication Date	Status
APPARATUS AND METHOD FOR PROCESSING COMPLEX INSTRUCTION FORMATS IN A MULTI-THREADED ARCHITECTURE SUPPORTING VARIOUS CONTEXT SWITCH MODES AND VIRTUALIZATION SCHEMES	EP	12174229.0	11/14/2007	EP2527972	11/28/2012	Published