

PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT4235541

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
BANG J YOON YOON	09/15/2008
YEOL YOUNG KIM	09/15/2008
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State/Country:	HONG KONG
PROPERTY NUMBERS Total: 13	
Property Type	Number
Patent Number:	7304460
Patent Number:	7271645
Patent Number:	7248121
Patent Number:	7242254
Patent Number:	7224233
Patent Number:	7215209
Patent Number:	7190231
Patent Number:	7148730
Patent Number:	7132869
Patent Number:	7129684
Patent Number:	7057377
Application Number:	11711399
Application Number:	11705998
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SIGNATURE: /TIMOTHY DEVLIN/

DATE SIGNED: 01/20/2017

This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 2

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ASSIGNMENT

A GROUP OF INDIVIDUAL INVESTORS having an internal address at JaYou 2-Cha Apartment 104-Dong 1203-Ho Uam 1-Dong, Nam-Gu Busan City, South Korea 608-774, (hereafter the "ASSIGNOR"), is the 20% owner of issued patents and patent applications which include but not limited to the followings:

- (1) 7,304,460 Smart start-up circuit for switching regulators
- (2) 7,271,645 Smart charge-pump circuit for phase-locked loops
- (3) 7,248,121 Variable lock-in circuit for phase-locked loops
- (4) 7,242,254 Adjustable lock-in circuit for phase-locked loops
- (5) 7,224,233 Smart lock-in circuit for phase-locked loops
- (6) 7,215,209 Controllable idle time current mirror circuit for switching regulators, phase-locked loops, and delay-locked loops

- (7) 7,190,231 High-performance charge-pump circuit for phase-locked loops
- (8) 7,148,730 Z-state circuit for phase-locked loops
- (9) 7,132,869 Zero idle time Z-state circuit for phase-locked loops, delay-locked loops, and switching regulators

- (10) 7,129,684 Variable start-up circuit for switching regulators
- (11) 7,057,377 Z-state circuit for switching regulators
- (12) 11/711,399 Pin number reduction circuit and methodology for mixed-signal IC, memory IC, and SOC

- (13) 11/705,998 Low-voltage drop reference generation circuit for A/D converter

- (14) ANA-01AC014 Robust reference generation circuit for A/D converter
- (15) ANA-01AC015 Robust reference generation circuit for D/A converter
- (16) ANA-01AC018 Filter-based lock-in circuits for PLL and fast system startup

ANA SEMICONDUCTOR., having a place of business at 496 Bevens Dr. San Jose, CA 95129 (hereafter "ASSIGNEE") and which owns 80% of the issued patents and patent applications, desires to acquire all of the rights to the issued patents and patent applications owned by ASSIGNOR.

THEREFORE, for good and valuable consideration, ASSIGNOR hereby transfers and assigns to ASSIGNEE the entire world wide right, title, and interest in and to its owned shares of the issued patents and patent applications, and in any and all reissues, extensions, renewals, reexaminations, divisions and continuations of the issued patents and patent applications.

ASSIGNOR agrees to execute all paper necessary in connection with the issued patents and patent applications and any continuing, divisional, reissue,

reexamination or corresponding international application(s) thereof and also to execute separate assignments in connection with such issued patents and patent applications as ASSIGNEE may deem necessary or expedient.

IN WITNESS WHEREOF, each member of ASSIGNOR executes this ASSIGNMENT with full knowledge of its contents and significance on the date following his or her name.

ASSIGNOR

By:



Signature or Seal

Print Name

Kim Yeol Yong

Date

2008 9.15

By:



Signature or Seal

Name

Yoon Bang Ju

Date

2008 Sep. 15