PATENT ASSIGNMENT COVER SHEET

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NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SHARP CORPORATION	08/23/2016

RECEIVING PARTY DATA

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Postal Code:	19808

PROPERTY NUMBERS Total: 15

Property Type	Number
Patent Number:	6420279
Patent Number:	6185131
Patent Number:	6747901
Patent Number:	6744667
Patent Number:	6873007
Patent Number:	7109764
Patent Number:	6831872
Patent Number:	8390052
Patent Number:	7529148
Patent Number:	7723839
Patent Number:	7002594
Patent Number:	7777759
Patent Number:	7821522
Patent Number:	6353263
Patent Number:	RE41826

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DATE SIGNED:	03/14/2017

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ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Sharp Corporation, a corporation organized under the laws of Japan, with an office at 1 Takumi-cho, Sakai-ku, Sakai-shi, Osaka 590-8522, Japan ("***Assignor***"), does hereby sell, assign, transfer, and convey unto III Holdings 10, LLC, a Delaware limited liability company, with an address at 2711 Centerville Rd, Suite 400, Wilmington, DE 19808, USA ("***Assignee***"), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the "***Patent Rights***"):

(a) the provisional patent applications, patent applications and patents listed in the table below (the "***Patents***");

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6420279	US	06/28/2001	Methods of using atomic layer deposition to deposit a high dielectric constant material on a substrate Yoshi Ono
JP4055941	JP	06/20/2002	METHOD OF DEPOSITING HIGH DIELECTRIC CONSTANT MATERIAL ON SUBSTRATE BY USING ATOMIC LAYER DEPOSITION METHOD Yoshi Ono
6185131	US	05/26/2000	Nonvolatile semiconductor storage device capable of electrically isolating dummy cell array region from memory cell array region Shuichiro Kouchi
6747901	US	01/23/2002	Nonvolatile semiconductor memory device capable of preventing occurrence of latch-up Yasuaki Hirano

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6744667	US	09/27/2002	BIT LINE CONTROL DECODER CIRCUIT, VIRTUAL GROUND TYPE NONVOLATILE SEMICONDUCTOR STORAGE DEVICE PROVIDED WITH THE DECODER CIRCUIT, AND DATA READ METHOD OF VIRTUAL GROUND TYPE NONVOLATILE SEMICONDUCTOR STORAGE DEVICE Kaoru Yamamoto Nobuhiko Ito
6873007	US	09/09/2003	Nonvolatile semiconductor memory device and process for producing the same Yasuhiro Sugita
JP4546716	JP	11/10/2003	PLL CLOCK SIGNAL GENERATION CIRCUIT Yasuhiko Sakamoto
7109764	US	11/09/2004	PLL clock signal generation circuit Yasuhiko Sakamoto
CNZL200410092393.X	CN	11/10/2004	PLL clock signal generation circuit Yasuhiko Sakamoto
JP4113423	JP	12/04/2002	Correction method for a semiconductor memory device and the reference cell Nobuaki Matsuoka
6831872	US	11/25/2003	Semiconductor memory device and method for correcting a reference cell Nobuaki Matsuoka
KR10-0555273	KR	12/04/2003	Semiconductor memory device and method for correcting a reference cell Nobuaki Matsuoka

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
TWI232455	TW	12/04/2003	Semiconductor memory device and method for correcting a reference cell Nobuaki Matsuoka
DE60343717.6	DE	12/04/2003	Semiconductor memory device and method for correcting a reference cell Nobuaki Matsuoka
FR1426970	FR	12/04/2003	Semiconductor memory device and method for correcting a reference cell Nobuaki Matsuoka
GB1426970	GB	12/04/2003	Semiconductor memory device and method for correcting a reference cell Nobuaki Matsuoka
IT1426970	IT	12/04/2003	Semiconductor memory device and method for correcting a reference cell Nobuaki Matsuoka
CNZL200310119592.0	CN	12/04/2003	Semiconductor memory device and method for correcting reference unit Nobuaki Matsuoka
8390052	US	03/31/2009	Nonvolatile semiconductor memory device Yoshimitsu Yamauchi
7529148	US	04/10/2007	Programmable read-only memory Sunay Shah
KR10-0880058	KR	04/12/2007	Programmable read-only memory Sunay Shah
CNZL200710097136.9	CN	04/12/2007	Programmable read-only memory Sunay Shah

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7723839	US	06/05/2006	Semiconductor device, stacked semiconductor device, and manufacturing method for semiconductor device Yuji Yano
JP3763397	JP	01/22/2001	Image processing device, image display device, a personal computer, an image processing method Hiroyuki Furukawa
TWI170629	TW	03/14/2001	Image processing apparatus and image display apparatus using same Hiroyuki Furukawa
DE60146533.4	DE	03/20/2001	Image processing apparatus with ROM storing a noise signal and image display apparatus using same Hiroyuki Furukawa
FR1137266	FR	03/20/2001	Image processing apparatus with ROM storing a noise signal and image display apparatus using same Hiroyuki Furukawa
GB1137266	GB	03/20/2001	Image processing apparatus with ROM storing a noise signal and image display apparatus using same Hiroyuki Furukawa
CNZL01112049.5	CN	03/23/2001	Image process and image indicator having same Hiroyuki Furukawa
CNZL200410058917.3	CN	03/23/2001	Image processing apparatus and method and image display apparatus Hiroyuki Furukawa

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7002594	US	03/23/2001	Image processing apparatus and image display apparatus using same Yasuhiro Yoshida
KR10-0397915	KR	03/24/2001	IMAGE PROCESSING APPARATUS AND IMAGE DISPLAY APPARATUS USING THE SAME Hiroyuki Furukawa
JP3944204	JP	09/16/2004	Image processing apparatus and an image display device provided with it Hiroyuki Furukawa
JP4369837	JP	09/16/2004	Image processing apparatus and an image display device provided with it Hiroyuki Furukawa
7777759	US	10/07/2005	IMAGE PROCESSING APPARATUS AND IMAGE DISPLAY APPARATUS USING SAME Yasuhiro Yoshida
7821522	US	10/07/2005	IMAGE PROCESSING APPARATUS AND IMAGE DISPLAY APPARATUS USING SAME Yasuhiro Yoshida
JP3565319	JP	04/14/1999	Semiconductor device and a method of manufacturing the same Yoshihisa Dotta
6353263	US	03/02/2000	Semiconductor device and manufacturing method thereof Yoshihisa Dotta

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CNZL00106890.3	CN	03/07/2000	Semiconductor device and manufacture thereof Yoshihisa Dotta
TWI223418	TW	03/02/2001	Semiconductor device Yasunori Chikawa
6836002	US	03/07/2001	Semiconductor device Yasunori Chikawa
CNZL01117392.0	CN	03/09/2001	Semiconductor device Yasunori Chikawa
JP4615189	JP	01/29/2003	Semiconductor device and the interposer chip Hisashige Nishida
DE602004005760.6	DE	01/26/2004	Semiconductor device Hisashige Nishida
FR1443558	FR	01/26/2004	Semiconductor device Hisashige Nishida
GB1443558	GB	01/26/2004	Semiconductor device Hisashige Nishida
KR10-0750764	KR	01/28/2004	Semiconductor device Hisashige Nishida
TWI230992	TW	01/28/2004	Semiconductor device Hisashige Nishida
RE41826	US	06/11/2007	SEMICONDUCTOR DEVICE Hisashige Nishida

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP4536808	JP	09/08/2008	Semiconductor device and the interposer chip Hisashige Nishida
8161250	US	05/20/2009	Methods and systems for partially-transacted data concurrency Harold Scott Hooper
7461318	US	09/28/2004	Communication system realizing USB communications between a host computer and its peripheral device and a communication controller transmitting a USB signal under the USB standard Fumihiro Fukae
8930658	US	03/15/2012	Electronic equipment system and storage device Tatsuaki Amemura
CNZL201210076844.5	CN	03/21/2012	Electronic equipment system and storage device Tatsuaki Amemura
JP4129170	JP	12/05/2002	Semiconductor Storage Device and Correction Method of Storage Data in Memory Cell Koji Hamaguchi
TWI232456	TW	12/04/2003	Semiconductor memory device and method for correcting memory cell data Koji Hamaguchi
DE60344561.6	DE	12/04/2003	Semiconductor memory device and method for correcting memory cell data Koji Hamaguchi

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
FR1426971	FR	12/04/2003	Semiconductor memory device and method for correcting memory cell data Koji Hamaguchi
6967867	US	12/05/2003	Semiconductor memory device and method for correcting memory cell data Koji Hamaguchi
KR10-0555275	KR	12/05/2003	SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR CORRECTING MEMORY CELL DATA Koji Hamaguchi
CNZL200310120107.1	CN	12/05/2003	Semiconductor memory device and method for correcting memory cell data Koji Hamaguchi
8208214	US	03/27/2007	Magnetic sensor device having near field light generation section employing a dielectric layer between a protruding metal layer and magnetic layer Noboru Iwata
6459377	US	07/02/2001	Abnormal condition detecting system detecting abnormal condition of user at residence Tatsuya Sakai
FR1172780	FR	07/05/2001	Abnormal condition detecting system detecting abnormal condition of user at residence Tatsuya Sakai
GB1172780	GB	07/05/2001	Abnormal condition detecting system detecting abnormal condition of user at residence Tatsuya Sakai

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
DE60113198.3	DE	07/05/2001	Abnormal condition detecting system detecting abnormal condition of user at residence Tatsuya Sakai
JP4004984	JP	03/28/2003	ELECTROMAGNETIC FIELD GENERATION ELEMENT, AND HEAD AND DEVICE FOR RECORDING/REPRODUCING INFORMATION Shintaro Miyanishi
7307923	US	03/25/2004	Electro magnetic field generating element, information recording and reproducing head and information recording and reproducing device Shintaro Miyanishi
7742285	US	10/21/2004	Folding portable terminal Katsutoshi Ishikura
DE602004027946.3	DE	10/21/2004	Folding portable terminal Katsutoshi Ishikura
GB1699208	GB	10/21/2004	Folding portable terminal Katsutoshi Ishikura
KR10-0792920	KR	06/23/2006	FOLDING PORTABLE TERMINAL Katsutoshi Ishikura
KR10-0705523	KR	04/15/2004	WIRELESS CONTROL SYSTEM, CONTROL DEVICE CONTROLLABLE DEVICE, DEVICE CONTROL METHOD, CONTROL PROGRAM, AND COMPUTER READABLE RECORDING MEDIUM CONTAINING THE SAME Kenji Sakamoto

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CNZL200480009871.4	CN	04/15/2004	Wireless control system, control device controllable device, device control method, control program, and computer readable recording medium containing the same Kenji Sakamoto
7702323	US	04/15/2004	A Wireless control system, controlling device, controlled devices,method of controlling devices, control program, and storage medium readable by computer for storing the program. Kenji Sakamoto
CNZL200410039946.5	CN	03/15/2004	Network reconfiguration, nodes and connecting object changing method Junji Suetsugu
DE602004017926.4	DE	03/15/2004	Network reconfiguration method Junji Suetsugu
FR1460800	FR	03/15/2004	Network reconfiguration method Junji Suetsugu
GB1460800	GB	03/15/2004	Network reconfiguration method Junji Suetsugu
7342899	US	03/16/2004	Network reconfiguration method, node and link change method, network reconfiguration program, link change program, and recording medium recording the program Junji Suetsugu
6876603	US	05/23/2001	Information write/read head including an optical slit having a light emitting section whose width is shorter than a light beam diffraction limit Hiroshi Fuji

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP4070983	JP	11/26/2001	LIGHT IRRADIATION DEVICE, MAGNETIC RECORDING HEAD AND MAGNETIC RECORDER Miyanishi Shintaro
6687195	US	12/11/2001	Magnetic recording head and magnetic recording device Shintaro Miyanishi
JP4972092	JP	07/23/2007	AV DEVICE Takayuki Suzuki
DE602007026857.5	DE	07/23/2007	AV DEVICE Takayuki Suzuki
FR2046023	FR	07/23/2007	AV DEVICE Takayuki Suzuki
GB2046023	GB	07/23/2007	AV DEVICE Takayuki Suzuki
CNZL200780027899.4	CN	07/23/2007	AV device Takayuki Suzuki
TWI340593	TW	07/26/2007	AV device Takayuki Suzuki
9179087	US	12/24/2008	AV DEVICE Takayuki Suzuki
JP3655521	JP	01/26/2000	Electronic Program Guide Display Control Device Shigeki Takahashi

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
FR1253782	FR	01/26/2001	Electronic Program Guide Display Controller Shigeki Takahashi
KR10-0488370	KR	01/26/2001	Electronic Program Guide Display Controller Shigeki Takahashi
AU772039	AU	01/26/2001	Electronic Program Guide Display Controller Shigeki Takahashi
CA2398196	CA	01/26/2001	Electronic Program Guide Display Controller Shigeki Takahashi
CNZL01806789.1	CN	01/26/2001	Electronic Program Guide Display Controller Shigeki Takahashi
DE60147881.9	DE	01/26/2001	Electronic Program Guide Display Controller Shigeki Takahashi

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, and/or (ii) for which any of the Patents directly or indirectly forms a basis for priority;

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(f) inventions, invention disclosures, and discoveries described in any of the Patents and/or any item in the foregoing categories (b) through (e) that (i) are included in any claim in the Patents and/or any item in the foregoing categories (b) through (e), (ii) are subject matter capable of being reduced to a patent claim in a reissue or reexamination proceeding brought on any of the Patents and/or any item in the foregoing categories (b) through (e), and/or (iii) could have been included as a claim in any of the Patents and/or any item in the foregoing categories (b) through (e);

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(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

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(2) injunctive relief, and
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Assignor will, at the reasonable request of Assignee, do all things necessary, proper, or advisable, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Osaka on 23 Aug., 2016.

ASSIGNOR:

Sharp Corporation

By: _____
Name: Takashi Nishida
Title: Vice President, Head of Intellectual Property Unit
Corporate R&D Division
(Signature MUST be attested)

ATTESTATION OF SIGNATURE PURSUANT TO 28 U.S.C. § 1746

The undersigned witnessed the signature of Takashi Nishida to the above Assignment of Patent Rights on behalf of Sharp Corporation and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. Takashi Nishida is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on August 23, 2016 to execute the above Assignment of Patent Rights on behalf of Sharp Corporation.

3. Takashi Nishida subscribed to the above Assignment of Patent Rights on behalf of Sharp Corporation.

I declare under penalty of perjury under the laws of the United States of America that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

EXECUTED on 23 August, 2016 (date)

_____
Print Name: Naoyuki Takahara