PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4342161

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
LUXTERA, INC.	03/28/2017

RECEIVING PARTY DATA

Name:	SILICON VALLEY BANK
Street Address:	380 INTERLOCKEN CRESCENT
Internal Address:	SUITE 600
City:	BROOMFIELD
State/Country:	COLORADO
Postal Code:	80021

PROPERTY NUMBERS Total: 134

Property Type	Number
Patent Number:	6788847
Patent Number:	6887773
Patent Number:	7027673
Patent Number:	7453132
Patent Number:	7010208
Patent Number:	6999670
Patent Number:	7245803
Patent Number:	7260289
Patent Number:	7184625
Patent Number:	7162124
Patent Number:	7139455
Patent Number:	7006732
Patent Number:	7184626
Patent Number:	7116853
Patent Number:	7136544
Patent Number:	7251386
Patent Number:	7269326
Patent Number:	7085443
Patent Number:	7039258

Property Type	Number
Patent Number:	7095010
Patent Number:	7194166
Patent Number:	7183759
Patent Number:	7024066
Patent Number:	7224174
Patent Number:	7262117
Patent Number:	7031562
Patent Number:	7298939
Patent Number:	7366380
Patent Number:	7116881
Patent Number:	7136563
Patent Number:	7095936
Patent Number:	7046894
Patent Number:	6993236
Patent Number:	7058273
Patent Number:	7251403
Patent Number:	7054533
Patent Number:	7082245
Patent Number:	7079742
Patent Number:	7082246
Patent Number:	7054534
Patent Number:	7072556
Patent Number:	7218826
Patent Number:	7082247
Patent Number:	7397101
Patent Number:	7340709
Patent Number:	7826688
Patent Number:	7068887
Patent Number:	7046895
Patent Number:	7046896
Patent Number:	7259031
Patent Number:	7262852
Patent Number:	7184627
Patent Number:	7260293
Patent Number:	7358527
Patent Number:	7450787
Patent Number:	7231105
Patent Number:	7298945

Property Type	Number
Patent Number:	7251408
Patent Number:	7613369
Patent Number:	7515775
Patent Number:	7773836
Patent Number:	7961992
Patent Number:	8121447
Patent Number:	8165431
Patent Number:	9136946
Patent Number:	8577191
Patent Number:	RE44829
Patent Number:	RE45214
Patent Number:	RE45215
Patent Number:	RE45390
Patent Number:	7616904
Patent Number:	7412138
Patent Number:	7378861
Patent Number:	8787774
Patent Number:	7586608
Patent Number:	7994066
Patent Number:	8238014
Patent Number:	8665508
Patent Number:	9548811
Patent Number:	8687981
Patent Number:	9172474
Patent Number:	9209907
Patent Number:	7881575
Patent Number:	8731410
Patent Number:	9264143
Patent Number:	9553676
Patent Number:	8168939
Patent Number:	8440989
Patent Number:	8772704
Patent Number:	8877616
Patent Number:	9053980
Patent Number:	8895413
Patent Number:	8280207
Patent Number:	8433162
Patent Number:	8861906

Property Type	Number
Patent Number:	9109948
Patent Number:	9417389
Patent Number:	7916377
Patent Number:	7899276
Patent Number:	8798476
Patent Number:	8358940
Patent Number:	8626002
Patent Number:	8592745
Patent Number:	9425342
Patent Number:	8289067
Patent Number:	8604866
Patent Number:	8649639
Patent Number:	8923664
Patent Number:	8625935
Patent Number:	9417466
Patent Number:	8471639
Patent Number:	8754711
Patent Number:	9431977
Patent Number:	8831437
Patent Number:	9356701
Patent Number:	9331096
Patent Number:	9091827
Patent Number:	9417410
Patent Number:	9575253
Patent Number:	9541775
Patent Number:	9389378
Patent Number:	9467227
Patent Number:	9577780
Application Number:	11195357
Application Number:	10777702
Application Number:	14922916
Application Number:	12241961
Application Number:	14105527
Application Number:	14105328
Application Number:	14448473
Application Number:	14926916
Application Number:	14606839
Application Number:	15205400

Property Type	Number
Application Number:	14997938

CORRESPONDENCE DATA

Fax Number: (800)494-7512

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 800-494-5225
Email: ipteam@nationalcorp.com
Correspondent Name: STEWART WALSH
Address Line 1: 1025 VERMONT AVE NW, SUITE 1130
Address Line 2: NATIONAL CORPORATE RESEARCH, LTD
Address Line 4: WASHINGTON, D.C. 20005

ATTORNEY DOCKET NUMBER:	F169256
NAME OF SUBMITTER:	ANDREW NASH
SIGNATURE:	/Andrew Nash/
DATE SIGNED:	03/29/2017

Total Attachments: 23

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THIRD AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement (this "Agreement") is entered into as of March 28, 2017, by and between SILICON VALLEY BANK, a California corporation, with a loan production office located at 380 Interlocken Crescent, Suite 600, Broomfield, Colorado 80021 ("Bank") and LUXTERA, INC., a Delaware corporation with its principal place of business located at 2320 Camino Vida Roble, Carlsbad, California 92011 ("Grantor"). This Agreement amends and restates in its entirety and replaces that certain Second Amended and Restated Intellectual Property Security Agreement by and between Bank and Grantor, dated as of June 29, 2012 (the "Prior Agreement").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodations to Grantor (the "Loans") in the amounts and manner set forth in (i) that certain Third Amended and Restated Loan and Security Agreement by and between Bank and Grantor dated as of the date hereof (as the same may be amended, modified or supplemented from time to time, the "Senior Loan Agreement") and (ii) that certain Mezzanine Loan and Security Agreement by and between Bank and Grantor dated as of the date hereof (as the same may be amended, modified or supplemented from time to time, the "Mezzanine Loan Agreement", and together with the Senior Loan Agreement, collectively, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in its Copyrights, Trademarks, Patents, and Mask Works (as each term is described below) to secure the obligations of Grantor to Bank.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of Grantor's obligations to Bank, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

1. Grant of Security Interest. To secure Grantor's obligations to Bank, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "Intellectual Property Collateral"), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work of authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "Copyrights");

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto (collectively, the "Trademarks");

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "Mask Works");

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

2. Recordation. Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement upon request by Bank.

3. Loan Documents. This Agreement has been entered into pursuant to and in conjunction with the Loan Agreement, which is hereby incorporated by reference. The

provisions of the Loan Agreement shall supersede and control over any conflicting or inconsistent provision herein. The rights and remedies of Bank with respect to the Intellectual Property Collateral are as provided by the Loan Agreement and related documents, and nothing in this Agreement shall be deemed to limit such rights and remedies.

4. Execution in Counterparts. This Agreement may be executed in counterparts (and by different parties hereto in different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a signature page to this Agreement by facsimile or in electronic (i.e., "pdf" or "tif" format) shall be effective as delivery of a manually executed counterpart of this Agreement.

5. Successors and Assigns. This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

6. Governing Law. This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby and thereby shall be governed by, and construed in accordance with, the laws of the United States and the State of California, without giving effect to any choice or conflict of law provision or rule (whether of the State of California or any other jurisdiction).

[Signature page follows.]

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

LUXTERA, INC.

By: _____

Title: CFO

BANK:

SILICON VALLEY BANK

By: _____

Title: _____

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

LUXTERA, INC.

By:_____

Title:_____

BANK:

SILICON VALLEY BANK

By:_____

Title: Managing Director

EXHIBIT A

Copyrights

None.

EXHIBIT B

Patents

Luxtera # (Internal spreadsheet tracking # only)	**Patent or Patent Application Title**	**Provisional Filed**	**USPTO Provisional #**	**US Patent Filed**	**USPTO Application #**	**USPTO #**	**US Patent Issued**
12	Photonic Input/Output Port (Galian Patent)	5-Apr-01	Multiple '01	28-Mar-02	10/109,302	6,788,847	7-Sep-04
20	Methods of Incorporating Germanium within a CMOS Process	13-Dec-02	Multiple '02	10-Jun-03	10/458,165	6,887,773	3-May-05
	Flip-chip devices formed on photonic integrated circuit chips			2-Aug-05	11/195,357		
21	Integrated Dual Waveguides	19-Jun-02	60/389,845	19-Jun-03	10/600,804	7,027,673	11-Apr-06
22	Waveguide Photodetector with Integrated Electronics Divisional of #22	19-Jun-02	Multiple '02	19-Jun-03	10/600,563	7,453,132	18-Nov-08
24	CMOS Process Silicon Waveguides	24-Jun-02	Multiple '02	24-Jun-03	10/606,297	7,010,208	7-Mar-06
26	Active Waveguides for Optoelectronic Devices	27-Aug-02	60/406,155	27-Aug-03	10/650,234	6,999,670	14-Feb-06
27	Optical Waveguide Grating Coupler	11-Feb-03	60/446,842	10-Feb-04	10/776,475	7,245,803	17-Jul-07
28	Optical Waveguide Grating Coupler with Varying Scatter Cross Sections	11-Feb-03	60/446,842	10-Feb-04	10/776,146	7,260,289	21-Aug-07
29	Optical Waveguide Grating Coupler Incorporating Reflective Optical Elements and Anti-Reflection Elements	11-Feb-03	60/446,847	10-Feb-04	10/776,438	7,184,625	27-Feb-07
33	Fiber to Chip Coupler	14-Mar-03	60/454,870	11-Mar-04	10/799,040	7,162,124	9-Jan-07

Luxtera # (Internal spreadsheet tracking # only)	**Patent or Patent Application Title**	**Provisional Filed**	**USPTO Provisional #**	**US Patent Filed**	**USPTO Application #**	**USPTO #**	**US Patent Issued**
34	Electronically Controllable Arrayed Waveguide Gratings	18-Mar-03	60/455,910	17-Mar-04	10/803,747	7,139,455	21-Nov-06
35	Polarization Splitting Grating Couplers	21-Mar-03	60/456,381	12-Dec-03	10/734,374	7,006,732	28-Feb-06
36	Wafer-Level Testing of Optical and Optoelectronic Chips	7-Apr-03	60/461,041	7-Apr-04	10/820,631	7,184,626	27-Feb-07
37	PN Diode Optical Modulators Fabricated in Rib Waveguides	15-Aug-03	60/495,402-4	11-Aug-04	10/917,204	7,116,853	3-Oct-06
38	PN Diode Optical Modulators Fabricated in Strip Loaded Waveguides	15-Aug-03	60/495,402-4	11-Aug-04	10/916,839	7,136,544	14-Nov-06
40	Integrated Photonic-Electronic Circuits and Systems			14-Jan-04	10/758,561	7,251,386	31-Jul-07
42	Photonic Input/Output Port (Continuation of #12)	5-Apr-01	60/281,650	7-Apr-04	10/821,008	7,269,326	11-Sep-07
53	Doping Profiles in PN Diode Optical Modulators	Same as 37	60/495,402-4	11-Aug-04	10/916,857	7,085,443	1-Aug-06
54	Distributed Amplifier Optical Modulators	Same as 37	60/495,402-4	13-Aug-04	10/917,927	7,039,258	2-May-06
55	Silicon on Insulator Resonator Sensors and Modulators and Method of Operating the Same	4-Dec-02	60/430,846	4-Dec-03	10/729,242	7,095,010	22-Aug-06
60	Use of Waveguide grating couplers in an optical mux/demux system	26-Aug-04	60/604,797	26-Aug-05	11/212,858	7,194,166	20-Mar-07

Luxtera # (Internal spreadsheet tracking # only)	Patent or Patent Application Title	Provisional Filed	USPTO Provisional #	US Patent Filed	USPTO Application #	USPTO #	US Patent Issued
68	Optical Probes With Spacing Sensors For Wafer Level Testing Of Optical And Optoelectronic Chips	Same as 36	60/461,041	17-Dec-04	11/015,981	7,183,759	27-Feb-07
69	Littrow Gratings As Alignment Structures For the Wafer Level Testing Of Optical And Optoelectronic Chips	Same as 36	60/461,041	17-Dec-04	11/016,497	7,024,066	4-Apr-06
70	Optical Alignment Loops For Wafer-Level Testing Of Optical And Optoelectronic Chips	Same as 36	60/461,041	17-Dec-04	11/015,957	7,224,174	29-May-07
76	Germanium Integrated CMOS Wafer and Method for Manufacturing the Same	21-Jan-05		22-Feb-05	11/064,035	7,262,117	28-Aug-07
78	Photonic Input/Output Port (Continuation of #42)			1-Feb-05	11/049,261	7,031,562	18-Apr-06
79	Optoelectronic Alignment Structures for the Wafer Level Testing of Optical and Optoelectronic Chips			16-Mar-05	11/083,705	7,298,939	20-Nov-07
80	PLC for Connecting Optical Fibers to Optical or Optoeletronic Devices			18-Apr-05	11/109,210	7,366,380	29-Apr-08
81	CMOS Process Polysilicon Strip Loaded Waveguides with a Three Layer Core			7-Jul-05	11/177,765	7,116,881	3-Oct-06

Luxtera # (Internal spreadsheet tracking # only)	Patent or Patent Application Title	Provisional Filed	USPTO Provisional #	US Patent Filed	USPTO Application #	USPTO #	US Patent Issued
82	CMOS Process Polysilicon Strip Loaded Waveguides with a Two Layer Core			7-Jul-05	11/177,169	7,136,563	14-Nov-06
84	Polysilicon and Silicon Dioxide Light Scatterers for Silicon Waveguides			14-Jul-05	11/183,003	7,095,936	22-Aug-06
85	Polysilicon Light Scatterers for Silicon Waveguides			14-Jul-05	11/182,217	7,046,894	16-May-06
86	Polysilicon and Silicon Dioxide Light Scatterers for Silicon Waveguides on Five Layer Substrates			14-Jul-05	11/182,262	6,993,236	31-Jan-06
87	Polysilicon Light Scatterers for Silicon Waveguides on Five Layer Substrates			14-Jul-05	11/182,662	7,058,273	6-Jun-06
89	Light Scattering Structures Formed in Silicon Waveguides			15-Jul-05	11/183,064	7,251,403	31-Jul-07
90	Light Scattering Structures Formed in Upper Layers of Strip Loaded Waveguides			15-Jul-05	11/182,153	7,054,533	30-May-06
91	Light Scattering Structures Formed in Upper Layer of Strip Loaded Waveguides			15-Jul-05	11/182,134	7,082,245	25-Jul-06
92	Light Scattering Structures Formed in Lower Layers of Strip Loaded Waveguides			15-Jul-05	11/183,035	7,079,742	18-Jul-06
93	Light Scattering Strucutres Formed in Lower Layer of Strip Loaded Waveguides			15-Jul-05	11/183,031	7,082,246	25-Jul-06

Luxtera # (Internal spreadsheet tracking # only)	**Patent or Patent Application Title**	**Provisional Filed**	**USPTO Provisional #**	**US Patent Filed**	**USPTO Application #**	**USPTO #**	**US Patent Issued**
95	Light Scattering Structures Formed in Silicon Strip Loaded Waveguides			15-Jul-05	11/182,165	7,054,534	30-May-06
96	CMOS Process Active Waveguides			29-Aug-05	11/215,459	7,072,556	4-Jul-06
97	CMOS Process Active Waveguides on Five Layer Substrates Division of 7,010,208			29-Aug-05	11/214,704	7,218,826	15-May-07
98	CMOS Process Waveguide Coupler			29-Aug-05	11/215,511	7,082,247	25-Jul-06
106	Germanium Silicon Heterostructure Photodetectors	20-Jul-04	60/589,298	7-Jul-05	11/177,132	7,397,101	8-Jul-08
108	Method of generating a geometrical rule for germanium integration within CMOS	20-Jul-04	60/589,298	7-Jul-05	11/177,133	7,340,709	4-Mar-08
112	Enhancing the Sensitivity of Resonant Optical Modulating and Switching Devices	21-Oct-05	60/729,085	20-Oct-06	11/584,754	7,826,688	2-Nov-10
113	Polarization Splitting Grating Couplers (divisional of #35)			26-Oct-05	11/260,560	7,068,887	27-Jun-06
114	Active Waveguides for Optoelectronic Devices (divisional of #26)			8-Nov-05	11/270,682	7,046,895	16-May-06
115	Active Waveguides for Optoelectronic Devices (divisional of #26)			8-Nov-05	11/270,785	7,046,896	16-May-06

Luxtera # (Internal spreadsheet tracking # only)	Patent or Patent Application Title	Provisional Filed	USPTO Provisional #	US Patent Filed	USPTO Application #	USPTO #	US Patent Issued
116	Integrated Photonic-Electronic Circuits and Systems (divisional of #40)			8-Nov-05	11/270,681	7,259,031	21-Aug-07
117	Wafer-Level Testing of Optical and Optoelectronic Chips (divisional of #36)			14-Nov-05	11/273,753	7,262,852	28-Aug-07
120	Optical Waveguide Grating Coupler Incorporating Reflective Optical Elements and Anti-Reflection Elements (divisional of #29)			16-Nov-05	11/281,776	7,184,627	27-Feb-07
122	Optical Waveguide Grating Coupler with Varying Scatter Cross Sections (continuation of 28, division of 10/776,146)			6-Dec-05	11/296,521	7,260,293	21-Aug-07
124	Systems and Methods for Testing Germanium Devices	3-Feb-05	60/649,779	3-Feb-06	11/347,663	7,358,527	15-Apr-08
126	Distributed Amplifier Optical Modulators (cont of 54)			27-Feb-06	11/363,512	7,450,787	11-Nov-08
128	Integrated Dual Waveguides (continuation of #21)			17-Mar-06	11/384,227	7,231,105	12-Jun-07
129	Polarization Splitting Grating Couplers (continuation of #113)			17-Mar-06	11/384,019	7,298,945	20-Nov-07

Luxtera # (Internal spreadsheet tracking # only)	Patent or Patent Application Title	Provisional Filed	USPTO Provisional #	US Patent Filed	USPTO Application #	USPTO #	US Patent Issued
130	Doping Profiles in PN Diode Optical Modulators (continuation of #53)			5-Apr-06	11/400,163	7,251,408	31-Jul-07
131	Design of CMOS Integrated Germanium Photodiodes	13-Apr-06	60/791,867	13-Apr-07	11/735,251	7,613,369	3-Nov-09
134	Distributed Amplifier Optical Modulator Continuation in Part of #54			29-Sep-06	11/540,172	7,515,775	7-Apr-09
	External cavity laser source			11-Feb-04	10/777,702		
138	Integrated Transceiver with Lightpipe Coupler (div/ cont of #123)			14-Dec-06	11/611,084	7,773,836	10-Aug-10
138D	Integrated Transceiver with Lightpipe Coupler			12-Jun-09	12/483,699	7,961,992	14-Jun-11
138DC1	Integrated Transceiver with Lightpipe Coupler			9-Jun-11	13/156,894	8,121,447	21-Feb-12
138DC2	Integrated Transceiver with Lightpipe Coupler				13/156,979	8,165,431	24-Apr-12
138DC3	Low-cost transceiver approach			16-Mar-12	13/422,635	9,136,946	15-Sep-15
138DC4	Low-cost transceiver approach			16-Mar-12	13/422,695	8,577,191	5-Nov-13
138Reissue	Integrated Transceiver with Lightpipe Coupler			8-Jun-12	13/491,968	RE44,829	8-Apr-14
138DReissue	Integrated Transceiver with Lightpipe Coupler			10-Feb-13	13/772,155	RE45,214	28-Oct-14
138DC1Reissue	Integrated Transceiver with Lightpipe Coupler			21-Feb-13	13/773,300	RE45,215	28-Oct-14

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138DC2Reissue	Integrated Transceiver with Lightpipe Coupler			22-Feb-13	13/774,808	RE45,390	24-Feb-15
140	Waveguide Photodetector with Integrated Electronics Divisional of #22			23-Feb-07	11/710,162	7,616,904	10-Nov-09
142	Optoelectronic Alignment Structures for the Wafer Level Testing of Optical and Optoelectronic Chips (Div of #79)			28-Feb-07	11/713,479	7,412,138	12-Aug-08
149	Optical Alignment Loops For the Wafer-Level Testing Of Optical And Optoelectronic Chips Cont of #70			26-Feb-07	11/711,452	7,378,861	27-May-08
	Method and system for a narrowband, non-linear optoelectronic receiver			6-Oct-08	12/245,867	8,787,774	22-July-14
150	Wafer-Level Testing of Optical and Optoelectronic Chips Cont of # 117 (divisional of #36)			28-Mar-07	11/729,814	7,586,608	8-Sep-09
152	Si Surface Cleaning for Semiconductor Circuits			13-Oct-07	11/871,987	7,994,066	9-Aug-11

Luxtera # (Internal spreadsheet tracking # only)	Patent or Patent Application Title	Provisional Filed	USPTO Provisional #	US Patent Filed	USPTO Application #	USPTO #	US Patent Issued
153R	Method and Circuit for encoding Multi-Level Pulse Amplitude Modulated Signals Using Integrated Optoelectronic Devices (re-filing)	8-Sep-08	61/191,480	8-Sep-09	12/555,291	8,238,014	7-Aug-12
153C1	Method and system for encoding multi-level pulse amplitude modulated signals using integrated optoelectronic devices			7-Aug-12	13/568,616	8,665,508	4-Mar-14
153C2	Method and system for encoding multi-level pulse amplitude modulated signals using integrated optoelectronic devices			4-Mar-14	14/196,122	9,548,811	17-Jan-17
155	Method and System for Split Voltage Domain Transmitter Circuits	2-Oct-07	60/997,282	11-Sep-08	12/208,650	8,687,981	1-Apr-14
155C1	Method and System for Split Voltage Domain Transmitter Circuits			28-Mar-14	14/229,243	9,172,474	27-Oct-15
155C2	Method and System for Split Voltage Domain Transmitter Circuits			26-Oct-15	14/922,916	Allowed	
156	Method and System for a Narrowband, Non-linear Optoelectronic Receiver	10-Oct-07	60/998,314	6-Oct-08	12/245,867	8,787,774	22-Jul-14
156C1	Method and System for a Narrowband, Non-linear Optoelectronic Receiver			22-Jul-14	14/337,736	9,209,907	8-Dec-15

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159	Low Loss Optical Interconnect	30-Jan-08	61/062,978	29-Jan-09	12/362,154	7,881,575	1-Feb-11
164	METHOD AND SYSTEM FOR OPTOELECTRONICS TRANSCEIVERS INTEGRATED ON A CMOS CHIP Combined with #154	29-May-08	61/057,127	30-Sep-08	12/241,961		
167	Method and System for Split Voltage Domain Receiver Circuits (split from 155)			11-Sep-08	12/208,668	8,731,410	20-May-14
167C1	Method and System for Split Voltage Domain Receiver Circuits (split from 155)			19-May-14	14/281,241	9,264,143	16-Feb-16
167C2	Method and System for Split Voltage Domain Receiver Circuits (split from 155)			16-Feb-16	15/045,216	9,553,676	24-Jan-17
168	Method and System for a Light Source Assembly Supporting Direct Coupling To An Integrated Circuit	9-Jul-08	61/079,358	14-May-13	13/894,052	8,772,704	8-Jul-14
168C1	Method and System for a Light Source Assembly Supporting Direct Coupling To An Integrated Circuit			9-Jul-09	12/500,465	8,168,939	1-May-12
168C2 (used to be C1)	Method and System for a Light Source Assembly Supporting Direct Coupling To An Integrated Circuit			25-Apr-12	13/455,641	8,440,989	14-May-13

Luxtera # (Internal spreadsheet tracking # only)	**Patent or Patent Application Title**	**Provisional Filed**	**USPTO Provisional #**	**US Patent Filed**	**USPTO Application #**	**USPTO #**	**US Patent Issued**
168C3	Method and System for a Light Source Assembly Supporting Direct Coupling To An Integrated Circuit			14-May-13	13/894,052	8,772,704	8-Jul-14
176 /181	METHOD AND SYSTEM FOR MONOLITHIC INTEGRATION OF PHOTONICS AND ELECTRONICS IN CMOS PROCESSES	8-Sep-08	61/191,479	4-Sep-09	12/554,449	8,877,616	4-Nov-14
176 / 181 D1	Monolithic integration of photonics and electronics in CMOS processes			2-Feb-12	13/364,845	9,053,980	9-Jun-15
176 / 181 D2	Monolithic integration of photonics and electronics in CMOS processes			2-Feb-12	13/364,909	8,895,413	25-Nov-14
177	Method and system for coupling optical signals into silicon optoelectronic chips	6-Nov-08	61/198,660	6-Nov-09	12/614,024	8,280,207	2-Oct-12
177C1	Methods of coupling optical signals into silicon optoelectronic chips (continuation)			21-Aug-12	13/590,821	8,433,162	30-Apr-13
177C2	Methods of coupling optical signals into silicon optoelectronic chips (continuation)			30-Apr-13	13/873,771	8,861,906	14-Oct-14
177C3	Coupling optical signals into silicon optoelectronic chips (continuation)			14-Oct-14	14/513,886	9,109,948	18-Aug-15

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177C4	Coupling Optical Signals into silicon optoelectronic chips			18-Aug-15	14/829,260	9,417,389	16-Aug-16
179	Integrated control system for laser and Mach-Zehnder interferometer	3-Nov-08	61/198,079	3-Nov-09	12/611,584	7,916,377	29-Mar-11
180	Distributed Amplifier Optical Modulator (Divisional of #134 - Continuation in Part of #54 for claims 31-41)		12/352,415	12-Jan-09	12/352,415	7,899,276	1-Mar-11
182	Method and system for single laser bidirectional links	18-Feb-09	61/207,958	18-Feb-10	12/708,496	8,798,476	5-Aug-14
184	Method and system for optoelectronic receivers for uncoded data	10-Jul-09	61/270,665	6-Jul-10	12/830,917	8,358,940	22-Jan-13
184C1	Method and system for optoelectronic receivers for uncoded data			15-Jan-13	13/741,678	8,626,002	7-Jan-14
187	Method and system for optoelectronic receivers utilizing waveguide heterojunction phototransistors integrated in a CMOS SOI wafer	19-Aug-09	61/274,588	18-Aug-10	12/859,016	8,592,745	26-Nov-13
187C1	Method and system for optoelectronic receivers utilizing waveguide heterojunction phototransistors integrated in a CMOS SOI wafer			26-Nov-13	14/091,259	9,425,342	23-Aug-16
189	Method and system for bandwidth enhancement using hybrid inductors	14-Sep-09	61/276,580	13-Sep-10	12/880,908	8,289,067	16-Oct-12

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189C1	Method and system for bandwidth enhancement using hybrid inductors			16-Oct-12	13/653,041	8,604,866	10-Dec-13
192	Method and system for waveguide mode filters	4-Mar-10	61/339,903	1-Mar-11	13/037,935	8,649,639	11-Feb-14
193	Method and system for multi-mode integrated receivers	15-Jun-10	61/397,739	9-Jun-11	13/156,990	8,923,664	30-Dec-14
194	Method and system for integrated power combiners	15-Jun-10	61/397,738	10-Jun-11	13/157,642	8,625,935	7-Jan-14
194C1	Method and system for integrated power combiners			7-Jan-14	14/149,626	9,417,466	16-Aug-16
196	Method and system for a feedback transimpedance amplifier with sub-40kHz Low-frequency cut-off	2-Jul-10	61/398,987	1-Jul-11	13/175,545	8,471,639	25-Jun-13
196C1	Method and system for a feedback transimpedance amplifier with sub-40kHz Low-frequency cut-off			25-Jun-13	13/926,851	8,754,711	17-Jun-14
196C2	Method and system for a feedback transimpedance amplifier with sub-40kHz Low-frequency cut-off			16-Jun-14	14/305,733	9,431,977	30-Aug-16
197	Method and System for a Photonic Interposer	30-Mar-11	61/516,226	16-Mar-12	13/422,776	8,831,437	9-Sep-14
197C1	Method and System for a Photonic Interposer			2-Sep-14	14/475,484	9,356,701	31-May-16
201	Method and system for hybrid integration of optical communication systems			7-Aug-12	13/568,406	9,331,096	3-May-16

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206	Method and system for grating couplers incorporating perturbed waveguides	9-Jul-12	61/690,952	8-Jul-13	13/936,408	9,091,827	28-Jul-15
206C1	Method and system for grating couplers incorporating perturbed waveguides			28-Jul-15	14/811,199	9,417,410	16-Aug-16
206C2	Method and system for grating couplers incorporating perturbed waveguides			9-Aug-16	15/232,051	9,575,253	21-Feb-17
208	METHOD AND SYSTEM FOR A LOW PARASITIC SILICON HIGH-SPEED PHASE MODULATOR	13-Dec-12	61/797,697	13-Dec-13	14/105,527		
209	METHOD AND SYSTEM FOR STABILIZED DIRECTIONAL COUPLERS	13-Dec-12	61/797,692	13-Dec-13	14/105,328		
210	Method and system for a low-voltage integrated silicon high-speed modulator	19-Mar-13	61/852,702	18-Mar-14	14/217,743	9,541,775	10-Jan-17
211	Connector Coupler for Silicon Photonics Devices	2-Aug-13	61/958,666	3-Jul-14	14/448,473		
212	Ge-on-Si Integrated Photo-Detectors Enabled w/o Contacts on the Germanium	21-Nov-13	61/963,043	29-Oct-15	14/926,916		
213	Method And System For Coupling A Light Source Assembly To An Optical Integrated Circuit	27-Jan-14	61/965,334	27-Jan-15	14/606,839		

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214	Method and System for Optical Power Monitoring of a Light Source Assembly Coupled into a Silicon Photonically-Enabled Integrated Circuit	3-Feb-14	61/965,612	3-Feb-15	14/612,416	9,389,378	12-Jul-16
214C1	Method and System for Optical Power Monitoring of a Light Source Assembly Coupled into a Silicon Photonically-Enabled Integrated Circuit			8-Jul-16	15/205,400		
217	Method and system for an optical connection service interface	13-Mar-14	61/967,254	13-Mar-15	14/657,907	9,467,227	11-Oct-16
221	Method and system for a polarization immune wavelength division multiplexing demultiplexer	26-Jun-14	61/998,385	26-Jun-15	14/752,709	9,577,780	21-Feb-17
226	Method And System for Accurate Gain Adjustment Of A Transimpedance Amplifier Using A Dual Replica And Servo Loop	16-Jan-15	62/125,290	18-Jan-16	14/997,938		

EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date
 The color(s) blue and black is/are claimed as a feature of the mark. The mark consists of a blue hexagon to the left of the work "Luxtera" appearing in black.	4592114	8/26/2014
LUXTERA	4524543	5/6/2014

EXHIBIT D

Mask Works

None.

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