PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
MIPS TECHNOLOGIES, INC.	02/06/2013

RECEIVING PARTY DATA

Name:	BRIDGE CROSSING, LLC
Street Address:	80 LAMBERT LANE, SUITE 115
City:	LAMBERTVILLE
State/Country:	NEW JERSEY
Postal Code:	08530

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	14467661

CORRESPONDENCE DATA

Fax Number: (612)349-9266

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 612-349-5741
Email: mitchell@ptslaw.com
Correspondent Name: JAMES H. PATTERSON
Address Line 1: 80 SOUTH 8TH STREET
Address Line 2: 4800 IDS CENTER
Address Line 4: MINNEAPOLIS, MINNESOTA 55402

ATTORNEY DOCKET NUMBER:	4729.06US05
NAME OF SUBMITTER:	VALERIE P. MITCHELL
SIGNATURE:	/Valerie P. Mitchell/
DATE SIGNED:	04/04/2017

Total Attachments: 27
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Patent Assignment

THIS PATENT ASSIGNMENT (this "**Patent Assignment**") is made to be effective as of February 7, 2013 (the "**Assignment Effective Date**") by and between MIPS Technologies, Inc., a Delaware corporation having a principal place of business at 955 East Arques Avenue, Sunnyvale, California 94085-9521 ("**Assignor**"), and Bridge Crossing, LLC, a Delaware limited liability company having a principal place of business at 80 Lambert Lane, Suite 115 Lambertville, New Jersey 08530 ("**Assignee**") (collectively referred to herein as the "**Parties**" and individually as "**Party**"). Capitalized terms used but not defined herein shall have the meanings assigned to them in the Agreement (as defined below).

WHEREAS, Assignor is the owner of the patents and patent applications listed on Schedule 1 hereto (the "**Patents**") and the abandoned or expired patents and patent applications listed on Schedule 2 hereto (the "**Abandoned Patents**");

WHEREAS, Assignee wishes to acquire all of Assignor's right, title and interest in and to the Patents and Abandoned Patents, and Assignor is willing to assign such rights to Assignee pursuant to this Patent Assignment;

WHEREAS, Assignor and Assignee have entered into a Patent Sale Agreement dated November 5, 2012, governing the terms and conditions of sale of the Assigned Patents and the Abandoned Patents (the "**Agreement**");

NOW, THEREFORE, for good and valuable consideration as set forth in the Agreement, the receipt of which from Assignee is hereby acknowledged, Assignor and Assignee agree as follows:

1. Assignment. Assignor hereby sells, assigns, transfers and sets over to Assignee all of Assignor's right, title and interest in and to:

(a) (i) the Patents; (ii) all patents and patent applications from which the Patents claim priority, directly or indirectly; and (iii) unless otherwise specified on Schedule 1, all continuations and continuations-in-part, divisions, substitutions, continued patent applications, re-examinations, renewals, extensions and reissues thereof, and all foreign counterparts and other applications and patents claiming priority to any of the foregoing, directly or indirectly, and all other corresponding rights that may be secured under the laws of the United States, any foreign jurisdiction or multi-jurisdictional entity (notwithstanding any of the foregoing, the properties assigned under this Patent Assignment shall not include any subject matter that is not disclosed in any patents or patent applications existing as of Assignment Effective Date);

(b) the Abandoned Patents;

(c) all damages based upon infringement of any or all of the Patents or Abandoned Patents; and

(d) all rights to enforce the Patents and Abandoned Patents and to sue for, collect and retain any and all damages for past, present and future infringement of any and all of the Patents and Abandoned Patents; and rights to collect royalties or other payments on account of Assignee's exploitation of any of the Patents and Abandoned Patents.

2. Encumbrances. The Assignor and Assignee acknowledge and agree that the Patents and Abandoned Patents and any subsequent assignment or transfer thereof, are encumbered by and subject to (i) certain third-party agreements (including, without limitation, covenants not to sue and licenses granted by Assignor to third parties prior to the effective date hereof) and (ii) the non-exclusive license-back granted by Assignee to Assignor under that certain Assigned Patent License Agreement between the parties dated as of the Assignment Effective Date.

3. Authorization. Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States and any applicable foreign agency to record this Patent Assignment and issue the Patents to Assignee and its successors, assigns and other legal representatives.

4. Further Actions. Each of the Parties covenants and agrees, at its own expense, to execute and deliver, at the reasonable request of the other Party hereto, such further instruments of transfer and assignment and to take such other action as is necessary to the consummation of the assignments and assumptions contemplated by this Patent Assignment.

5. Counterparts. This Patent Assignment may be executed in two or more counterparts, all of which, taken together, shall be considered to be one and the same instrument. The exchange of a fully executed Patent Assignment (in counterparts or otherwise) by facsimile transmission, by electronic mail in "portable document format" (".pdf") form, or by any other electronic means intended to preserve the original graphic and pictorial appearance of a document, shall be sufficient to bind the Parties to the terms and conditions of this Patent Assignment.

6. Entire Agreement; Modification. With the exception of the Agreement, this Patent Assignment supersedes any arrangements, understandings, promises or agreements made or existing between the Parties hereto prior to or simultaneously with this Patent Assignment and, together with the Agreement (and agreements incorporated by reference therein), constitutes the entire understanding between the Parties. This Patent Assignment may not be modified or amended, except in writing signed by the Parties.

[REMAINDER OF PAGE INTENTIONALLY LEFT BLANK]

IN WITNESS WHEREOF, the Parties have executed this Patent Assignment, made to be effective as of the Assignment Effective Date.

MIPS Technologies, Inc.	**Bridge Crossing, LLC**
By: _____	By: _____
Print Name: Sandeep Vij	Print Name: _____
Title: President and CEO	Title: _____
Date: _____	Date: _____

STATE OF)

COUNTY OF)

On FEBRUARY 6, 2013, before me RAQUEL LEE MILLER, Notary Public, personally appeared SANDEEP VIJ ~~personally known to me~~ (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

RAQUEL LEE MILLER
Commission # 1921315
Notary Public - California
Santa Clara County
My Comm. Expires Feb 6, 2015

WITNESS my hand and official seal.

Raquel Lee Miller
Signature of Notary

IN WITNESS WHEREOF, the Parties have executed this Patent Assignment as of the Assignment Effective Date.

MIPS Technologies, Inc.

By: _____
Print Name: _____
Title: _____
Date: _____

Bridge Crossing, LLC

By: _____
Print Name: DANIEL P. McCLOY
Title: CEO
Date: February 7, 2013

STATE OF)

COUNTY OF)

On _____, before me _____, Notary Public, personally appeared _____ personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

_____
Signature of Notary

SCHEDULE 1

Patents

Registered U.S. Assigned Patents:

Country	Application No.	Filing Date	Registration No.	Issue Date	Title
US	07/918819	7/22/1992	5491702	2/13/1996	Apparatus for Detecting Any Single Bit Error, Detecting Any Two Bit Error, & Detecting any Three or Four Bit Error in a Group of Four Bits for a 25- or 64-Bit Data Word
US	08/063183	5/17/1993	5450607	9/12/1995	Unified Floating Point and Integer Datapath for a RISC Processor
US	08/168822	12/15/1993	5526504	6/11/1996	Variable Page Size Translation Lookaside Buffer
US	08/168832	12/15/1993	5510934	4/23/1996	Apparatus for Processing Instructions in a Computing System
US	08/172684	12/22/1993	5542062	7/30/1996	Two-Level Cache Memory System
US	08/212377	3/11/1994	5479630	12/26/1995	Hybrid Cache Having Physical-Cache & Virtual-Cache Characteristics & Method for Accessing Same
US	08/245200	5/17/1994	5504698	4/2/1996	A Compact Dual Function Adder
US	08/245983	5/17/1994	5619672	4/8/1997	Precise Translation Lookaside Buffer Error Detection & Shutdown Circuit
US	08/324861	10/18/1994	5555384	9/10/1996	Optimized Pipeline Operations for Reduced Instruction Set Computers
US	08/378844	1/26/1995	5524245	6/4/1996	System and Method for Booting Computer for Operation in Either of Two Byte-Order Modes
US	08/379710	1/27/1995	5572713	11/5/1996	Method & Apparatus For Byte Order Switching in a Computer
US	08/405622	3/15/1995	5696958	12/9/1997	Method & Apparatus for Reducing Delays Following the Execution of a Branch Instruction in an Instruction Pipeline
US	08/410524	3/24/1995	5732242	3/24/1998	Prefetching Hints
US	08/449588	5/24/1995	5590294	12/31/1996	Method & Apparatus for Restarting Pipeline Processing
US	08/484313	6/7/1995	5699551	12/16/1997	Two-Level Cache Memory System
US	08/487240	6/13/1995	5740402	4/14/1998	Conflict Resolution in Interleaved Memory Systems with Multiple Parallel Accesses
US	08/491491	6/16/1995	5568442	10/22/1996	RISC Processor Having Improved Instruction Fetching Capability & Utilizing Address Bit Precoding for a Segmented Cache Memory
US	08/561914	11/22/1995	5670898	9/23/1997	Low-Power Compact Digital Logic Topology that Facilitates Large Fan-In & High Speed
US	08/686363	7/24/1996	5870574	2/9/1999	RISC Processor Having Improved Instruction Fetching Capability & Utilizing Address Bit Precoding for a Segmented Cache Memory
US	08/935369	9/22/1997	6092187	7/18/2000	Instruction Prediction Based on Filtering
US	08/947648	10/9/1997	5864703	1/26/1999	Providing Extended Precision in SIMD Vector Arithmetic Operations
US	08/947649	10/9/1997	5933650	8/3/1999	Alignment & Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	08/982244	12/1/1997	6240488	5/29/2001	Prefetching Hints
US	09/216017	12/16/1998	6477562	11/5/2002	Prioritized Instruction Scheduling for Multi-Streaming Processors

US	09/223046	12/30/1998	7159100	1/2/2007	Method for Providing Extended Precision in SIMD Vector Arithmetic Operations
US	09/240012	1/27/1999	6292888	9/18/2001	Register Transfer Unit for Electronic Processor
US	09/263798	3/5/1999	6266758	7/24/2001	Alignment & Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	09/273810	3/22/1999	6389449	5/14/2002	Interstream Control and Communications for Multi-Streaming Digital Processors
US	09/302246	4/29/1999	6345354	2/5/2002	Register File Access
US	09/312302	5/14/1999	7020879	3/28/2006	Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	09/318551	5/27/1999	6732208	5/4/2004	Low Latency System Bus Interface For Multi-Master Processing Environments
US	09/363637	7/30/1999	6912559	6/28/2005	System and Method for Improving the Accuracy of Reciprocal and Reciprocal Square Root Operations Performed by a Floating Point Unit
US	09/364512	7/30/1999	7346643	3/18/2008	Processor with Improved Accuracy for Multiply-Add Operations
US	09/364514	7/30/1999	6697832	2/24/2004	Floating-Point Processor with Improved Intermediate Result Handling
US	09/364786	7/30/1999	7242414	7/10/2007	Processor Having a Compare Extension of an Instruction Set Architecture
US	09/364787	7/30/1999	6714197	3/30/2004	Processor Having an Arithmetic Extension of an Instruction Set Architecture
US	09/364789	7/30/1999	6732259	5/4/2004	Processor Having a Conditional Branch Extension of an Instruction Set Architecture
US	09/373091	8/12/1999	6493776	12/10/2002	Scalable On-Chip System Bus
US	09/373092	8/12/1999	6490642	12/3/2002	Locked Read/Write on Separate Address/Data Bus Using Write Barrier
US	09/373093	8/12/1999	6604159	8/5/2003	Data Release to Reduce Latency in On-Chip System Bus
US	09/373094	8/12/1999	6681283	1/20/2004	Coherent Data Apparatus for an On-Chip Split Transaction System Bus
US	09/373095	8/12/1999	6393500	5/21/2002	Burst-Configurable Data Bus
US	09/383401	8/26/1999	6188248	2/13/2001	Output-Synchronization Free, High-Fanin Dynamic OR/NOR Gate
US	09/494488	1/31/2000	6430655	8/6/2002	Scratchpad RAM with Cache-Like Access Times
US	09/517272	3/2/2000	6446171	9/3/2002	Method and Apparatus for Tracking and Update of LRU Algorithm Using Vectors
US	09/544352	4/6/2000	6425076	7/23/2002	Instruction Prediction Based on Filtering
US	09/577238	5/23/2000	6996596	2/7/2006	Flush-to-nearest mode to improve floating-point accuracy over existing flush-to-zero mode
US	09/586115	6/2/2000	7043467	5/9/2006	Wire-speed Multi-Dimensional Packet Classifier
US	09/591510	6/12/2000	7162615	1/9/2007	Data Transfer Bus Communication Using Single Request to Perform Command and Return Data to Context Associated Destination Registration (Amended)
US	09/592106	6/12/2000	7257814	8/14/2007	Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors
US	09/595776	6/16/2000	7237093	6/26/2007	Instruction Fetching System in a Multithreaded Processor Utilizing Cache Miss Predictions to Fetch Instructions from Multiple Hardware Streams
US	09/602279	6/23/2000	7502876	3/10/2009	Background Memory Manager That Determines if Data Structures Fit in Memory with Memory State Transactions Map
US	09/608750	6/30/2000	7032226	4/18/2006	Methods and Apparatus for Managing a Buffer of Events in the Background
US	09/616385	7/14/2000	7035997	4/25/2006	Methods and Apparatus for Improving Fetching and Dispatch of Instructions in Multithreaded Processor
US	09/637500	8/11/2000	7401205	7/15/2008	High Performance RISC Instruction Set Digital Signal Processor Having Circular Buffer Control and Looping Instruction Commands (as amended)

US	09/654064	9/1/2000	6651160	11/18/2003	Register Set Extension for Compressed Instruction Set
US	09/662832	9/15/2000	7197625	3/27/2007	Alignment & Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	09/665099	9/20/2000	6625737	9/23/2003	System for Prediction and Control of Power Consumption in Digital Systems
US	09/702112	10/30/2000	7149878	12/12/2006	Changing Instruction Set Architecture Mode by Comparison of Current Instruction Execution Address with Boundary Address Register Values
US	09/706154	11/3/2000	7139898	11/21/2006	Fetch and Dispatch Disassociation Apparatus for Multi-Streaming Processors
US	09/706157	11/3/2000	7035998	4/25/2006	Clustering Stream and/or Instruction Queues for Multi-Streaming Processors
US	09/734713	12/13/2000	6448817	9/10/2002	Output-Synchronization Free, High-Fanin Dynamic OR/NOR Gate
US	09/737375	12/14/2000	7058064	6/6/2006	Queuing System for Processors in Packet Routing Operations
US	09/751747	12/29/2000	7237090	6/26/2007	Configurable Out-of-Order Data Transfer in a Coprocessor Interface
US	09/751748	12/29/2000	7287147	10/23/2007	Configurable Coprocessor Interface
US	09/753239	12/29/2000	6754804	6/22/2004	Coprocessor Interface Transferring Multiple Instructions Simultaneously Along with Issue Path Designation and/or Issue Order Designation for the Instructions
US	09/788670	2/21/2001	7599981	10/6/2009	Binary Polynomial Multiplier
US	09/788682	2/21/2001	7162621	1/9/2007	Virtual Instruction Expansion Based on Template and Parameter Selector Information Specifying Sign-Extension or Concatenation
US	09/788683	2/21/2001	7237097	6/26/2007	Partial Bitwise Permutations
US	09/788684	2/21/2001	7711763	5/4/2010	Microprocessor Instructions for Performing Polynomial Arithmetic Operations
US	09/788685	2/21/2001	7181484	2/20/2007	Extended-Precision Accumulation of Multiplier Output
US	09/799610	3/7/2001	7039060	5/2/2006	System and Method for Extracting Fields from Packets Having Fields Spread Over More Than One Register
US	09/804677	3/12/2001	7127586	10/24/2006	Prefetching Hints
US	09/818946	3/28/2001	6742165	5/25/2004	System, Method and Computer Program Product for Web-Based Integrated Circuit Design
US	09/822796	3/30/2001	6643759	11/4/2003	Mechanism to Extend Computer Memory Protection Schemes
US	09/836541	4/18/2001	7711926	5/4/2010	Mapping System and Method for Instruction Set Processing
US	09/844271	4/30/2001	7181728	2/20/2007	User-Controlled Trace Records
US	09/844668	4/30/2001	7134116	11/7/2006	External Trace Synchronization via Periodic Sampling
US	09/844669	4/30/2001	7185234	2/27/2007	Trace Control From Hardware and Software
US	09/844670	4/30/2001	7168066	1/23/2007	Tracing Out-of-Order Load Data
US	09/844671	4/30/2001	7124072	10/17/2006	Program Counter and Data Tracing from a Multi-Issue Processor
US	09/844672	4/30/2001	7069544	6/27/2006	Dynamic Selection of a Compression Algorithm for Trace Data
US	09/844673	4/30/2001	7178133	2/13/2007	Trace Control Based on a Characteristic of a Processor's Operating State
US	09/850195	5/8/2001	7065675	6/20/2006	System and Method for Speeding Up EJTAG Block Data Transfers
US	09/881628	6/13/2001	7649901	1/19/2010	Method and Apparatus for Optimizing Selection of Available Contexts for Packet Processing in Multi-Stream Packet Processing
US	09/881934	6/14/2001	7076630	7/11/2006	Method and Apparatus for Allocating and De-allocating Consecutive Blocks of Memory in Background Memory Management

US	09/882285	6/18/2001	6826681	11/30/2004	Method and Apparatus for Saving and Restoring Processor Register Values and Allocating and Deallocating Stack Memory
US	09/894812	6/28/2001	6976178	12/13/2005	Inhibition Feature to System for Prediction and Control of Power Consumption in Digital Systems
US	09/894830	6/29/2001	7043668	5/9/2006	Optimized External Trace Formats
US	09/894831	6/29/2001	7231551	6/22/2007	Distributed TAP Controller
US	09/894832	6/29/2001	7055070	5/30/2006	Trace Control Block Implementation and Method
US	09/900393	7/5/2001	7042887	5/9/2006	Method and Apparatus for Non-Speculative Pre-Fetch Operation in Data Packet Processing
US	09/905185	7/13/2001	6728859	4/27/2004	Programmable Page Table Access
US	09/924755	8/7/2001	7058065	6/6/2006	Methods and Apparatus for Preventing Undesirable Packet Download with Pending Read/Write Operation in Data Packet Processing
US	09/925314	8/10/2001	7107439	9/12/2006	Control of Software Decompression through the use of Exceptions Due to Unaligned Instruction Fetch
US	09/927129	8/10/2001	7165257	1/16/2007	Context Selection and Activation Mechanism for Activating One of a Group of Inactive Contexts in a Processor Core for Servicing Interrupts
US	09/933934	8/20/2001	7065096	6/20/2006	Method for Allocating Memory Space for Limited Packet Head and/or Tail Growth
US	09/935446	8/22/2001	7415531	8/19/2008	Prediction of Packet Flow, Packet Header and Packet Payload
US	09/948919	9/7/2001	7139901	11/21/2006	Extended Instruction Set for a Packet Processing Applications
US	09/954290	9/11/2001	7082552	7/25/2006	Functional Validation of a Packet Management Unit
US	09/964827	9/25/2001	7155516	12/26/2006	Method and Apparatus for Overflowing Data Packets to a Software-Controlled Memory when they do not Fit into a Hardware-controlled Memory
US	09/977084	10/12/2001	7487339	2/3/2009	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
US	10/071547	2/8/2002	6789100	9/7/2004	Interstream Control and Communications for Multi-Streaming Digital Processors
US	10/135004	4/26/2002	6961819	11/1/2005	Method and Apparatus for Redirection of Operations Between Interfaces
US	10/141579	5/9/2002	7318145	1/8/2008	Random Slip Generator
US	10/141926	5/10/2002	7310706	12/18/2007	Random Cache Line Refill Order
US	10/159818	5/31/2002	6883156	4/19/2005	Apparatus and Method for Relative Position Annotation of Standard Cell Components to Facilitate Datapath Design
US	10/186290	6/27/2002	7017025	3/21/2006	Mechanism for Proxy Management of Multiprocessor Virtual Memory
US	10/186330	6/27/2002	7003630	2/21/2006	Mechanism for Proxy Management of Multiprocessor Storage Hierarchies
US	10/193682	7/12/2002	7911952	3/22/2011	Interface with Credit-Based Flow Control and Sustained Bus Signals
US	10/195522	7/16/2002	7225212	5/29/2007	Extended Precision Accumulator
US	10/255107	9/26/2002	7246287	7/17/2007	Full Scan Solution for Latched-Based Design
US	10/274424	10/18/2002	6987405	1/17/2006	Apparatus and Method for Generating Multi-Phase Signals with Digitally Controlled Trim Capacitors
US	10/278537	10/22/2002	6836833	12/28/2004	Apparatus and Method for Discovering a Scratch Pad Memory Configuration
US	10/448324	5/28/2003	7159101	1/2/2007	System and Method to Trace High-Performance Multi-Issue Processors
US	10/449818	5/30/2003	7194582	3/20/2007	Microprocessor with Improved Data Stream Prefetching
US	10/449825	5/30/2003	7177985	2/13/2007	Microprocessor with Improved Data Stream Prefetching

US	10/637006	8/8/2003	7747989	6/29/2010	Virtual Machine Coprocessor Facilitating Dynamic Compilation
US	10/698061	10/31/2003	7707389	4/27/2010	Multi-ISA Instruction Fetch Unit for a Processor, and Applications Thereof (as amended)
US	10/921077	8/18/2004	7765546	7/27/2010	Interstream Control and Communications for Multi-Streaming Digital Processors
US	10/923584	8/20/2004	7886129	2/8/2011	Configurable Co-processor Interface
US	10/956490	10/1/2004	7315937	1/1/2008	Microprocessor Instructions for Efficient Bit Stream Extractions
US	10/956498	10/1/2004	7873810	1/18/2011	Microprocessor Instruction Using Address Index Values to Enable Access of a Virtual Buffer in Circular Fashion
US	10/994827	11/23/2004	7281123	10/9/2007	Restoring Register Values from Stack Memory Using Instruction with Restore Indication Bit and De-allocation Frame Size Stack Pointer Offset
US	11/003120	12/3/2004	7509456	3/24/2009	Apparatus and Method for Discovering a Scratch Pad Memory Configuration
US	11/026324	12/29/2004	7475303	1/6/2009	HYPERJTAG System Including Debug Probe, On-Chip Instrumentation and Protocol
US	11/051980	2/4/2005	7752627	7/6/2010	Leaky-Bucket Thread Scheduler in a Multithreading Microprocessor
US	11/051998	2/4/2005	7664936	2/16/2010	Prioritizing Thread Selection Partly Based on Stall Likelihood Providing Status Information of Instruction Operand Register Usage at Pipeline Stages
US	11/086258	3/22/2005	7506140	3/17/2009	Return Data Selector Employing Barrel-Incrementer-Based Round Robin Apparatus
US	11/087063	3/22/2005	7490230	2/10/2009	Fetch Director Employing Barrel-Incrementer-Based Round Robin Apparatus for Use in Multithreading Microprocessor
US	11/087064	3/22/2005	7631130	12/8/2009	Barrel-Incrementer-Based Round-Robin Apparatus and Instruction Dispatch Scheduler Employing Same for Use in Multithreading Microprocessor
US	11/087070	3/22/2005	7657883	2/2/2010	Instruction Dispatch Scheduler Employing Round-Robin Apparatus Supporting Multiple Thread Priorities for Use in Multi-threading Micro-processor
US	11/107489	4/14/2005	7600135	10/6/2009	Apparatus and Method for Software Specified Power Management Performance Using Low Power Virtual Threads
US	11/107492	4/14/2005	7627770	12/1/2009	Apparatus and Method for Automatic Low Power Mode Invocation in a Multi-Threaded Processor
US	11/121945	5/5/2005	8234326	7/31/2012	Processor Core and Multiplier That Support Both Vector and Single Value Multiplication
US	11/122004	5/5/2005	8229991	7/24/2012	Processor Core and Multiplier that Support a Multiply and Difference Operation by Inverting Sign Bits in Booth Recoding
US	11/191258	7/27/2005	7681014	3/16/2010	Multithreading Instruction Scheduler Employing Thread Group Priorities
US	11/214466	8/29/2005	7634619	12/15/2009	Method and Apparatus for Redirection of Operations Between Interfaces
US	11/257381	10/24/2005	7620832	11/17/2009	Method and Apparatus for Masking a Microprocessor Execution Signature
US	11/261654	10/31/2005	7711934	5/4/2010	Processor Core and Method for Managing Branch Misprediction in an Out-of-Order Processor Pipeline
US	11/261655	10/31/2005	7734901	6/8/2010	Processor Core and Method for Managing Program Counter Redirection in an Out-of-Order Processor Pipeline
US	11/272718	11/15/2005	7873820	1/18/2011	Processor Utilizing a Loop Buffer to Reduce Power Consumption

US	11/272719	11/15/2005	7562191	7/14/2009	Microprocessor Having a Power-Saving Instruction Cache Way Predictor and Instruction Replacement Scheme
US	11/272737	11/15/2005	7496771	2/24/2009	Processor Accessing a Scratch Pad On-Demand to Reduce Power Consumption
US	11/277101	3/21/2006	7467385	12/16/2008	Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	11/277293	3/23/2006	7715410	5/11/2010	Queuing System for Processors in Packet Routing Operations
US	11/278747	4/5/2006	7661112	2/9/2010	Methods and Apparatus for Managing a Buffer of Events in the Background
US	11/278874	4/6/2006	7707391	4/27/2010	Methods and Apparatus for Improving Fetching and Dispatch of Instructions in Multithreaded Processors
US	11/278890	4/6/2006	7280548	10/9/2007	Method and Apparatus for Non-Speculative Pre-Fetch Operation in Data Packet Processing
US	11/278901	4/6/2006	7197043	3/27/2007	Method for Allocating Memory Space for Limited Packet Head and/or Tail Growth
US	11/279136	4/10/2006	7581091	8/25/2009	System and Method for Extracting Fields from Packets Having Fields Spread Over More Than One Register
US	11/279914	4/17/2006	8181000	5/15/2012	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
US	11/336923	1/23/2006	7721073	5/18/2010	Conditional Branch Execution in a Processor Having a Data Mover Engine That Associates Register Addresses with Memory Addresses
US	11/336937	1/23/2006	7721074	5/18/2010	Conditional Branch Execution in a Processor Having a Read-Tie Instruction and a Data Mover Engine that Associates Register Addresses with Memory Addresses
US	11/336938	1/23/2006	7721075	5/18/2010	Conditional Branch Execution in a Processor Having a Write-Tie Instruction and a Data Mover Engine that Associates Register Addresses with Memory Addresses
US	11/337440	1/24/2006	7546443	6/9/2009	Providing Extended Precision in SIMD Vector Arithmetic Operations
US	11/360338	2/23/2006	7551626	6/23/2009	Queuing System for Processors in Packet Routing Operations
US	11/362764	2/28/2006	7721071	5/18/2010	System and Method for Propagating Operand Availability Identifiers with Instructions Through a Pipeline in an Out-of-Order Processor (as amended)
US	11/365280	2/28/2006	7386701	6/10/2008	Prefetching Hints
US	11/380924	4/29/2006	7644307	1/5/2010	Functional Validation of a Packet Management Unit
US	11/380925	4/29/2006	7194599	3/20/2007	Configurable Co-Processor Interface
US	11/391716	3/28/2006	7721127	5/18/2010	Multithreaded Dynamic Voltage-Frequency Scaling Microprocessor
US	11/410146	4/25/2006	7860911	12/28/2010	Extended Precision Accumulation
US	11/442695	5/25/2006	7627794	12/1/2009	Apparatus and Method for Discrete Test Access Control of Multiple Cores
US	11/442696	5/25/2006	8145882	3/27/2012	Apparatus and Method for Processing Template Based User Defined Instructions
US	11/445518	6/2/2006	7770156	8/3/2010	Dynamic Selection of the Best Compression Algorithm for Trace Data
US	11/463939	8/11/2006	7512740	3/31/2009	Microprocessor with Improved Data Stream Prefetching
US	11/463950	8/11/2006	7664920	2/16/2010	Microprocessor with Improved Data Stream Prefetching
US	11/463954	8/11/2006	7533220	5/12/2009	Microprocessor with Improved Data Stream Prefetching
US	11/463957	8/11/2006	7480769	1/20/2009	Microprocessor with Improved Data Stream Prefetching
US	11/485959	7/14/2006	7370178	5/6/2008	Method for Latest Producer Tracking in an Out-of-Order Processor, and Applications Thereof
US	11/505865	8/18/2006	7650465	1/19/2010	Processor Having a Micro Tag Array That Reduces Data Cache Access Power, and Applications Thereof

US	11/505869	8/18/2006	7657708	2/2/2010	Methods for Reducing Data Cache Access Power in a Processor, and Applications Thereof
US	11/515720	9/6/2006	7647475	1/12/2010	System for Synchronizing an In-Order Co-processor with an Out-of-Order Processor Using a Co-processor Interface Store Data Queue (as amended)
US	11/515723	9/6/2006	8032734	10/4/2011	Coprocessor Load Data Queue for Interfacing an Out-Of-Order Execution Unit with an In-Order Coprocessor
US	11/517569	9/8/2006	8151093	4/3/2012	Software Programmable Hardware State Machines
US	11/532520	9/16/2006	7760748	7/20/2010	Transaction Selector Employing Barrel-Incrementer-Based Round-Robin Apparatus Supporting Dynamic Priorities in Multi-Port Switch
US	11/532521	9/16/2006	7773621	8/10/2010	Transaction Selector Employing Round-Robin Apparatus Supporting Dynamic Priorities in Multi-Port Switch
US	11/532522	9/16/2006	7961745	6/14/2011	Bifurcated Transaction Selector Supporting Dynamic Priorities in Multi-Port Switch
US	11/532523	9/16/2006	7990989	8/2/2011	Transaction Selector Employing Transaction Queue Group Priorities in Multi-Port Switch
US	11/537584	9/29/2006	7702055	4/20/2010	Apparatus and Method for Tracing Processor State From Multiple Clock Domains
US	11/539322	10/6/2006	7406586	7/29/2008	Fetch and Dispatch Disassociation Apparatus for Multi-Streaming Processors
US	11/545706	10/11/2006	7594079	9/22/2009	Data Cache Virtual Hint Way Prediction, and Applications Thereof
US	11/549413	10/13/2006	7506106	3/17/2009	Microprocessor with Improved Data Stream Prefetching
US	11/549418	10/13/2006	7509459	3/24/2009	Microprocessor with Improved Data Stream Prefetching
US	11/552640	10/25/2006	7529915	5/5/2009	Context Switching Processor with Multiple Context Control Register Sets Including Write Address Register Identifying Destination Register for Waiting Context to Store Returned Data From External Source
US	11/552764	10/25/2006	7877481	1/25/2011	Method and Apparatus for Overflowing Data Packets to a Software-Controlled Memory when they do not Fit into a Hardware-controlled Memory
US	11/557005	11/6/2006	8185879	5/22/2012	External Trace Synchronization via Periodic Sampling
US	11/566870	12/5/2006	7765554	7/27/2010	Context Selection and Activation Mechanism for Activating one of a Group of Inactive Contexts in a Processor Core for Servicing Interrupts
US	11/611064	12/14/2006	7509447	3/24/2009	Barrel-Incrementer-Based Round-Robin Apparatus and Instruction Dispatch Scheduler Employing Same for Use in Multithreading Microprocessor
US	11/616539	12/27/2006	7865647	1/4/2011	Efficient Resource Arbitration
US	11/616558	12/27/2006	7840874	11/23/2010	Speculative Cache Tag Evaluation
US	11/620362	1/5/2007	7660969	2/9/2010	Multithreading Instruction Scheduler Employing Thread Group Priorities
US	11/636462	12/11/2006	7509480	3/24/2009	Boundary Address Registers for Selection of ISA Mode
US	11/640491	12/18/2006	8078846	12/13/2011	Conditional Move Instruction Formed Into One Decoded Instruction to be Graduated and Another Decoded Instruction to be Invalidated
US	11/644001	12/22/2006	7617388	11/10/2009	Virtual Instruction Expansion Using Parameter Selector Defining Logic Operation on Parameters for Template Opcode Substitution
US	11/668582	1/30/2007	7487332	2/3/2009	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts
US	11/674924	2/14/2007	7698533	4/13/2010	Configurable Coprocessor Interface

US	11/676242	2/16/2007	7412630	8/12/2008	Trace Control From Hardware and Software
US	11/676541	2/20/2007	7650605	1/19/2010	Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors
US	11/684156	3/9/2007	8103987	1/24/2012	System and Method for Managing the Design and Configuration of an Integrated Circuit Semiconductor Design
US	11/684205	3/9/2007	7774723	8/10/2010	Protecting Trade Secrets During the Design and Configuration of an Integrated Circuit Semiconductor Design
US	11/702659	2/6/2007	7793077	9/7/2010	Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	11/747666	5/11/2007	7886150	2/8/2011	System Debug and Trace System and Method, and Applications Thereof
US	11/764137	6/15/2007	7543207	6/2/2009	Full Scan Solution for Latched-Based Design
US	11/767225	6/22/2007	7769957	8/3/2010	Preventing Writeback Race in Multiple Core Processors
US	11/767261	6/22/2007	7769958	8/3/2010	Avoiding Livelock Using Intervention Messages in Multiple Core Processors
US	11/806845	6/4/2007	7724261	5/25/2010	Processor Having a Compare Extension of an Instruction Set Architecture
US	11/838648	8/14/2007	8069354	11/29/2011	Power Management for System Having One or More Integrated Circuits
US	11/859198	9/21/2007	8131941	3/6/2012	Support for Multiple Coherence Domains
US	11/868429	10/5/2007	7739484	6/15/2010	Method and Apparatus for Saving and Restoring Processor Register Values and Allocating and Deallocating Stack Memory
US	11/876442	10/22/2007	7529907	5/5/2009	Method and Apparatus for Improved Computer Load and Store Operations
US	11/943751	11/21/2007	8190665	5/29/2012	Random Cache Line Refill Order
US	11/949418	12/3/2007	8024393	9/20/2011	Processor with Improved Accuracy for Multiply-Add Operations
US	11/963503	12/21/2007	7917699	3/29/2011	Apparatus and Method for Controlling the Exclusivity Mode of a Level-Two Cache
US	11/976713	10/26/2007	7917882	3/29/2011	Automated Digital Circuit Design Tool that Reduces or Eliminates Adverse Timing Constraints Due to an Inherent Clock Signal Skew, and Applications Thereof
US	12/000413	12/12/2007	8051320	11/1/2011	Clock Ratio Controller for Dynamic Voltage and Frequency Scaled Digital Systems, and Applications Thereof
US	12/021110	1/28/2008	8024539	9/20/2011	Virtual Processor Based Security for On-Chip Memory, and Applications Thereof
US	12/047257	3/12/2008	8001283	8/16/2011	Efficient, Scalable and High Performance Mechanism for Handling IO Requests
US	12/060204	3/31/2008	8230202	7/24/2012	Apparatus and Method for Condensing Trace Information in a Multi-Processor System
US	12/104308	4/16/2008	7747840	6/29/2010	Latest Producer Tracking in Out-of-Order Processor
US	12/173560	7/15/2008	7636836	12/22/2009	Fetch and Dispatch Decoupling Mechanism for Multi-Streaming Processors
US	12/185587	8/4/2008	7822943	10/26/2010	Microprocessor with Improved Data Stream Prefetching
US	12/185594	8/4/2008	8077734	12/13/2011	Method and Apparatus for Predicting Characteristics of Incoming Data Packets to Enable Speculative Processing to Reduce Processor Latency
US	12/187631	8/7/2008	7644319	1/5/2010	Trace Control From Hardware and Software
US	12/274104	11/19/2008	7900207	3/1/2011	Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	12/346652	12/30/2008	8078840	12/13/2011	Thread Instruction Fetch Based On Prioritized Selection From Plural Round-Robin Outputs For Different Thread States
US	12/348181	1/2/2009	7925864	4/12/2011	Method and Apparatus for Binding Shadow Registers to Vectored Interrupts

US	12/348847	1/5/2009	7613966	11/3/2009	HYPERJTAG System Including Debug Probe, On-Chip Instrumentation and Protocol
US	12/421268	4/9/2009	7899993	3/1/2011	Microprocessor Having a Power-Saving Instruction Cache Way Predictor and Instruction Replacement Scheme
US	12/432227	4/28/2009	7926062	4/12/2011	Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	12/477059	6/2/2009	7969186	6/28/2011	Apparatus and Method for Forming a Mixed Signal Circuit with Fully Customizable Analog Cells and Programmable Interconnect
US	12/480414	6/8/2009	8074058	12/6/2011	Providing Extended Precision in SIMD Vector Arithmetic Operations
US	12/506153	7/20/2009	8185717	5/22/2012	Apparatus and Method for Profiling Software Performance on a Processor with Non-Unique Virtual Addresses
US	12/544167	8/19/2009	7895423	2/22/2011	Method for Extracting Fields from Packets having Fields Spread over more than One Register
US	12/649132	12/29/2009	8081645	12/20/2011	Context Sharing Between A Streaming Processing Unit (SPU) and A Packet Management (PMU) In A Packet Processing Environment
US	12/911392	10/25/2010	8078806	12/13/2011	Microprocessor with Improved Data Stream Prefetching
US	12/985680	1/6/2011	8209522	6/26/2012	System and Method for Extracting Fields from Packets having Fields Spread over more than One Register
US	13/027917	2/15/2011	8291364	10/16/2012	Automated Digital Circuit Design Tool that Reduces or Eliminates Adverse Timing Constraints Due to an Inherent Clock Signal Skew, and Applications Thereof
US	13/034567	2/24/2011	8234456	7/31/2012	Apparatus and Method for Controlling the Exclusivity Mode of a Level-Two Cache

U.S. Assigned Patent Applications:

Country	Application No.	Filing Date	Publication No.	Publ. Date	Title
US	10/637005	8/8/2003			Virtual Machine Coprocessor for Accelerating Software Execution
US	13/161332	6/15/2011			Programmable Memory Address Segments

US	13/161354	6/15/2011			Apparatus and Method for Hardware Initiation of Emulated Instructions
US	13/168870	6/24/2011			Apparatus and Method for Accelerated Hardware Page Table Walk
US	13/328781	12/16/2011			System for Compression of Fixed Width Variables in a CPU Hardware Trace
US	13/358399	1/25/2012			Merged Floating Point Operation Using a Modebit
US	13/360319	1/27/2012			MULTITHREADED OPERATION OF A MICROPROCESSOR CACHE
US	13/361441	1/30/2012			Support for Multiple Coherence Domains
US	13/538984	6/29/2012			Carry Look-Ahead Adder with Generate Bits and Propagate Bits Used for Column Sums
US	13/603280	9/4/2012			MICROCONTROLLER WITH VIRTUALIZED SECURITY CONTROLS USING GUEST IDENTIFICATIONS, A COMMON KERNEL ADDRESS SPACE AND OPERATIONAL PRIVILEGES
US	13/609047	9/10/2012			Apparatus and Method for Low Overhead Correlation of Multi-Processor Trace Information
US	61/562975	11/22/2011			Achieving Glitch-Free Clock Domain Crossing Signals Using Formal Verification, Static Timing Analysis, and Sequential Equivalence Checking
US	11/362763	2/28/2006	0204139A1	8/30/2007	Compact Linked-List-Based Multi-Threaded Instruction Graduation Buffer
US	11/485960	7/14/2006	0016326A1	1/17/2008	Latest Producer Tracking in an Out-of-Order Processor, and Applications Thereof
US	11/529710	9/29/2006	0082793A1	4/3/2008	Detection and Prevention of Write-After-Write Hazards, and Applications Thereof
US	11/529728	9/29/2006	0082794A1	4/3/2008	Load/Store Unit for a Processor, and Applications Thereof
US	11/530945	9/12/2006	0074014A1	3/29/2007	Extended Instruction Set for Packet Processing Applications
US	11/627899	1/26/2007	0184361A1	7/31/2008	Systems and Methods for Controlling the Use of Processing Algorithms, and Applications Thereof
US	11/684189	3/9/2007	0222581A1	9/11/2008	Remote Interface for Managing the Design and Configuration of an Integrated Circuit Semiconductor Design
US	11/727640	3/27/2007	0239967A1	10/11/2007	High-Performance RISC-DSP
US	11/830795	7/30/2007	0037886A1	2/5/2009	Apparatus and Method for Evaluating a Free-Running Trace Stream
US	11/864363	9/28/2007	0089510A1	4/2/2009	Speculative Read In a Cache Coherent Microprocessor
US	11/896424	8/31/2007	0063881A1	3/5/2009	Low-overhead/Power-Saving Processor Synchronization Mechanism, and Applications Thereof
US	12/058117	3/28/2008	0248988A1	10/1/2009	Mechanism for Maintaining Consistency of Data Written by IO Devices

US	12/060214	3/31/2008	0249046A1	10/1/2009	Apparatus and Method for Low Overhead Correlation of Multi-Processor Trace Information
US	12/194936	8/20/2008	0049912A1	2/25/2010	Data Cache Way Prediction
US	12/195053	8/20/2008	0049953A1	2/25/2010	Data Cache Receive Flop Bypass
US	12/210150	9/12/2008	0070257A1	3/18/2010	Methods, Systems and Computer Program Products for Evaluating Electrical Circuits from Information Stored in Simulation Dump Files
US	12/332291	12/10/2008	0157981A1	6/18/2009	Coherent Instruction Cache Utilizing Cache-Op Execution Resources
US	12/357929	1/22/2009	0132841A1	5/21/2009	Processor Accessing a Scratch Pad On-Demand to Reduce Power Consumption
US	12/399330	3/6/2009	0198986A1	8/6/2009	Configurable Instruction Sequence Generation
US	12/409363	3/23/2009	0249351A1	10/1/2009	Round-Robin Apparatus and Instruction Dispatch Scheduler Employing Same For Use In Multithreading Microprocessor
US	12/411913	3/26/2009	0187739A1	7/23/2009	Method and Apparatus for Improved Computer Load and Store Operations
US	12/429029	4/23/2009	0271592A1	10/29/2009	Apparatus for Storing Instructions In a Multithreading Microprocessor
US	12/429655	4/24/2009	20090210682A1	8/20/2009	Data Transfer Bus Communication Using Single Request to Perform Command and Return Data to Context Associated Destination Registration (Amended)
US	12/463330	5/8/2009	0282220A1	11/12/2009	Microprocessor with Compact Instruction Set Architecture
US	12/464027	5/11/2009	2010-0287359-A1	11/11/2010	Variable Register and Immediate Field Encoding in an Instruction Set Architecture
US	12/563840	9/21/2009	0011166A1	1/14/2010	Data Cache Virtual Hint Way Prediction, and Applications Thereof
US	12/652598	1/5/2010	0199054A1	8/5/2010	System and Method for Improving Memory Transfer
US	12/748102	3/26/2010	2010-0312991	12/9/2010	Microprocessor with Compact Instruction Set Architecture
US	12/794370	6/4/2010	2010-0306513	12/2/2010	Processor Core and Method for Managing Program Counter Redirection in an Out-of-Order Processor Pipeline
US	12/847772	7/30/2010	0030392 A1	2/2/2012	System and Method for Automatic Hardware Interrupt Handling
US	12/875268	9/3/2010	2011-0055497	3/3/2011	Alignment and Ordering of Vector Elements for Single Instruction Multiple Data Processing
US	13/041948	3/7/2011	2011-0154347	6/23/2011	Interrupt and Exception Handling for Multi-Streaming Digital Processors
US	13/277856	10/20/2011	0036380 A1	2/9/2012	Clock Ratio Controller for Dynamic Voltage and Frequency Scaled Digital Systems, and Appli

US	13/323006	12/12/2011	20120082167	4/5/2012	Method and Apparatus for Predicting Characteristics of Incoming Data Packets to Enable Speculative Processing to Reduce Processor Latency
US	13/404350	2/24/2012	2012/0221838	8/30/2012	Software Programmable Hardware State Machines

Co-Owned Patents:

Country	Status	Application No.	Filing Date	Registration No.	Issue Date	Title
US	Granted	08/167005	12/15/1993	5572704	11/5/1996	System and Method for Coherency in a Split-Level Data Cache System
US	Granted	08/167006	12/15/1993	5493523	2/20/1996	Mechanism and Method for Integer Divide Involving Pre-Alignment of the Divisor Relative to the Dividend
US	Granted	08/168744	12/15/1993	5604909	2/18/1997	Apparatus for Processing Instructions in a Computing System
US	Granted	08/696788	8/14/1996	5632025	5/20/1997	System and Method for Coherency in a Split-Level Data Cache System
US	Granted	08/781851	1/10/1997	5954815	9/21/1999	Apparatus for Processing Instructions in a Computing System
US	Granted	09/363635	7/30/1999	6247124	6/12/2001	Apparatus for Processing Instructions in a Computing System
US	Granted	09/863898	5/24/2001	6691221	2/10/2004	Apparatus for Processing Instructions in a Computing System

US	Granted	08/166969	12/15/1993	5537538	7/16/1996	Debug Mode for a Superscalar RISC Processor

SCHEDULE 2

Abandoned Patents

Country	Application No.	Filing Date	Registration No.	Issue Date	Title
US	06/860304	5/5/1986	4805098	2/14/1989	Write Request Buffering Apparatus
US	06/945486	12/23/1986	4814976	3/21/1989	RISC Computer with Unaligned Reference Handling and Method for the Same
US	06/827269	2/6/1986	4953073	8/28/1990	CPU Chip Having Cache Tag Comparator & Address Translation Unit on Chip & Connected to Off-Chip Cache & Main Memories
US	07/277406	11/28/1988	4959779	9/25/1990	Dual Byte Order Computer Architecture A Functional Unit for Handling Data Sets with Different Byte Orders
US	07/161543	2/29/1988	4879676	11/7/1989	Method of and apparatus using floating point exception signals for controlling several processors
US	07/255791	10/11/1988	5027270	6/25/1991	Processor Controlled Interface with Instruction Streaming
US	07/659526	2/22/1991	5101117	3/31/1992	Variable Delay Line Phase-Locked Loop Circuit
US	07/444639	12/1/1989	5111464	5/5/1992	Interrupt Reporting for Single-Bit Memory
US	07/448715	12/11/1989	5056110	10/8/1991	Differential Bus with Specified Default Value
US	07/444633	12/1/1989	5179670	1/12/1993	Slot Determination Mechanism Using Pulse Counting
US	07/491114	3/9/1990	5113506	5/12/1992	System Having an Address Generating Unit & a Log Comparator Packaged as an Integrated Circuit Separate from Cache Log
US	07/444594	12/1/1989	5226133	7/6/1993	Two-Level Translation Look-Aside Buffer Using Partial Addresses for Enhanced Speed
US	07/366344	6/14/1989	5237671	8/17/1993	Translation Lookaside Buffer Shutdown Scheme
US	07/644705	1/23/1991	5263140	11/16/1993	Variable Page Size Per Entry Translation Look Aside Buffer
US	07/573926	8/28/1990	5285116	2/8/1994	Low Noise High Speed Output Buffer and Method for Controlling Same
US	08/059715	5/10/1993	5307477	4/26/1994	Two-Level Cache Memory System
US	08/019541	2/18/1993	5325507	6/28/1994	Translation Lookaside Buffer Shutdown Scheme
US	08/127105	9/27/1993	5398328	3/14/1995	Method & Apparatus For Byte Order Switching in a Computer
US	08/223388	4/5/1994	5420992	5/30/1995	Backward Compatible Computer Architecture with Extended Wordsize and Address Space
US	07/892918	6/3/1992	5297092	3/22/1994	Sense Amp for Bit Line Sensing and Data Latching
US	07/893156	6/3/1992	5301153	4/5/1994	Redundant Element Substitution Apparatus
US	07/892919	6/3/1992	5327381	7/5/1994	Redundancy Selection Apparatus and Method for an Array
US	07/901910	6/19/1992	5408664	4/18/1995	System and Method for Booting Computer for Operation in Either of Two Byte-Order Modes
US	07/933467	8/21/1992	5317601	5/31/1994	Clock Distribution System for an Integrated Circuit Device
US	08/715246	9/19/1996	5734877	3/31/1998	Processor Chip Having On-Chip Circuitry for Generating a Programmable External Clock Signal & for Controlling Data Patterns
US	09/036684	3/9/1998	5978926	11/2/1999	Processor Chip Having On-Chip Circuitry for Generating a Programmable External Clock Signal & for Controlling Data Patterns
US	07/956867	10/1/1992	5309382	5/3/1994	Binary Shifter
US	08/796142	2/7/1997	5758112	5/26/1998	Pipeline Processor with Enhanced Method and Apparatus for Restoring Register-Renaming Information in the Event of a Branch Misprediction
US	29/036927	3/30/1995	D398009	9/8/1998	Pushbutton Remote Control

US	08/404625	3/14/1995	6216200	4/10/2001	Address Queue	
US	08/772233	12/23/1996	6266735	7/24/2001	Translation lookaside buffer with virtual address conflict prevention	
US	08/813500	3/7/1997	6594728	7/15/2003	Cache Memory with Dual-Way Arrays and Multiplexed Parallel Output	

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US	08/854087	5/9/1997	System Having an Address Generating Unit & a Log Comparator Packaged as an Integrated Circuit Separate from Cache Log
US	08/108526	8/18/1993	System Having an Address Generating Unit & a Log Comparator Packaged as an Integrated Circuit Separate from Cache Log
US	06/827282	2/6/1986	Dual Byte Order Computer Architecture A Functional Unit for Handling Data Sets with Different Byte Orders
US	06/859075	5/2/1986	Translation Lookaside Buffer Shutdown Scheme
US	07/156779	2/17/1988	Variable Delay Line Phase-Locked Loop Circuit
US	07/496050	3/16/1990	Variable Delay Line Phase-Locked Loop Circuit
US	07/444660	12/1/1989	Two-Level Cache Memory System
US	07/444637	12/1/1989	Bus Arbitration Mechanism
US	07/983630	11/30/1992	Bus Arbitration Mechanism
US	08/035544	3/23/1993	Optimized Pipeline Operations for Reduced Instruction Set Computers
US	07/444495	12/1/1989	Optimized Pipeline Operations for Reduced Instruction Set Computers
US	07/564923	8/9/1990	Method & Apparatus For Byte Order Switching in a Computer
US	08/380428	1/30/1995	Method & Apparatus For Byte Order Switching in a Computer
US	07/668275	3/11/1991	Backward Compatible Computer Architecture with Extended Wordsize and Address Space
US	07/679709	4/3/1991	Hybrid Cache Having Physical-Cache & Virtual-Cache Characteristics & Method for Accessing Same
US	07/671560	3/19/1991	Method & Apparatus for Retarting Pipeline Processing
US	08/229076	4/18/1994	Method & Apparatus for Retarting Pipeline Processing
US	08/003072	1/11/1993	Method & Apparatus for Reducing Delays Following the Execution of a Branch Instruction in an Instruction Pipeline
US	08/367661	1/3/1995	Cache Coherency Mechanism for Multiprocessor System
US	07/951648	9/25/1992	Cache Coherency Mechanism for Multiprocessor System
US	09/404792	9/24/1999	Processor Chip Having On-Chip Circuitry for Generating a Programmable External Clock Signal & for Controlling Data.
US	08/353169	12/8/1994	Processor Chip Having On-Chip Circuitry for Generating a Programmable External Clock Signal & for Controlling Data.

US	07/942675	9/9/1992	Processor Chip Having On-Chip Circuitry for Generating a Programmable External Clock Signal & for Controlling Data.
US	08/218145	3/25/1994	Self-Locating Heat Sink & Electro Magnetic Shield Assembly
US	08/023807	2/25/1993	Self-Locating Heat Sink & Electro Magnetic Shield Assembly
US	08/025367	2/24/1993	Self-Locating Heat Sink & Electro Magnetic Shield Assembly
US	08/064189	5/17/1993	RISC Processor Having Improved Instruction Fetching Capability & Utilizing Address Bit Precoding for a Segmented Cache Memory
US	08/168094	12/15/1993	Superscalar Microprocessor Instruction Pipeline Including Dispatching and Kill Control
US	08/168827	12/15/1993	Conflict Resolution in Interleaved Memory Systems with Multiple Parallel Accesses
US	08/476942	6/7/1995	Apparatus for Processing Instructions in a Computing System
US	08/167004	12/15/1993	Load Latency of Zero for Floating Point Load Instructions Using a Load Data Queue
US	08/412212	3/27/1995	Load Latency of Zero for Floating Point Load Instructions Using a Load Data Queue
US	08/941424	9/30/1997	Prefetching Hints
US	08/324127	10/14/1994	Redundant Mapping Tables
US	08/790086	1/29/1997	Redundant Mapping Tables
US	08/324129	10/14/1994	Address Queue
US	08/324124	10/14/1994	Indexing & Multiplexing of Interleaved Cache Memory Arrays
US	08/324128	10/14/1994	Memory Translation
US	08/324360	10/17/1994	Memory Translation
US	10/735804	12/16/2003	Providing Extended Precision in SIMD Vector Arithmetic Operations
US	08/934280	9/19/1997	Instruction Prediction Based on Filtering
US	09/335230	6/17/1999	Processor Having an Arithmetic Extension of an Instruction Set Architecture
US	09/249188	2/12/1999	Processor Having an Arithmetic Extension of an Instruction Set Architecture
US	09/336415	6/17/1999	Processor Having a Compare Extension of an Instruction Set Architecture
US	09/249177	2/12/1999	Processor Having a Compare Extension of an Instruction Set Architecture
US	09/249498	2/12/1999	Processor Having a Conditional Branch Extension of an Instruction Set Architecture
US	09/335444	6/17/1999	Processor Having a Conditional Branch Extension of an Instruction Set Architecture
US	09/336196	6/17/1999	Floating-Point Processor with Improved Intermediate Result Handling
US	10/055346	1/25/2002	System and Method for Improving the Accuracy of Reciprocal and Reciprocal Square Root Operations Performed by a Floating Point Unit
US	09/334927	6/17/1999	System and Method for Improving the Accuracy of Reciprocal and Reciprocal Square Root Operations Performed by a Floating Point Unit
US	11/228997	9/16/2005	Floating-Point Processor with Operating Mode Having Improved Accuracy and High Performance
US	09/702115	10/30/2000	Translation Lookaside Buffer for Selection of ISA Mode
US	09/751746	12/29/2000	A Co-processor Interface that Enables Coprocessor-Specific Branching
US	09/925716	8/10/2001	Partial Bitwise Permutations
US	10/029985	12/31/2001	Cache Scrambling Interface
US	10/115289	4/4/2002	Full Scan Solution for Latched-Based Design
US	10/283326	10/30/2002	A Method for Providing High Frequency Scan Testability on Low Speed Testers

US	10/633677	8/5/2003	Virtual Machine Coprocessor for Accelerating Software Execution
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US	11/608725	12/8/2006	Apparatus and Method to Trace High Performance Multi-Issue Processors
US	09/629805	7/31/2000	Method and Apparatus for Improved Computer Load and Store Operations
US	09/826693	4/4/2001	System and Method for Date Cache Bypassing in a Stream Processing Unit for a Multi-Streaming Processor
US	10/669129	9/22/2003	System and Method for Simulating a Multi-Stage Microprocessor
US	10/684348	10/10/2003	Integrated Mechanism for Suspension and Deallocation of Computational Threads of Execution in a Processor
US	10/777714	2/12/2004	Apparatus and Method for Preventing Duplicate Matching Entries in a Translation Lookaside Buffer
US	11/156270	6/17/2005	Multithreading Instruction Scheduler Employing Thread Group Priorities
US	11/176979	7/7/2005	Multithreading Instruction Scheduler Employing Thread Group Priorities
US	11/537574	9/29/2006	Apparatus and Method for Tracing Instructions with Simplified Instruction State Descriptors
US	11/555122	10/31/2006	Apparatus and Method for Forming a Bus Transaction Trace Stream with Simplified Bus Transaction Descriptors
US	11/670876	2/2/2007	System, Method and Software Application for the Generation of Verification Programs
US	11/767239	6/22/2007	Reduced Handling of Writeback Data
US	11/862154	9/26/2007	Semiconductor with Hardware Locked Intellectual Property and Related Methods
US	11/655267	1/19/2007	Synthesized Assertions in a Self-Correcting Processor and Applications Thereof

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US	60/121807	2/25/1999	High Performance System Bus Interface
US	60/294598	6/1/2001	Random Slip Generator
US	60/294605	6/1/2001	Random Cache Line Refill Order
US	60/318673	9/13/2001	Cache Scrambling Interface
US	60/403126	8/12/2002	Virtual Machine Coprocessor for Accelerating Software Execution
US	60/492312	8/5/2003	Virtual Machine Coprocessor for Accelerating Software Execution
US	60/176937	1/18/2000	Method and Apparatus for Improved Computer Load and Store Operations
US	60/180998	2/8/2000	Wire-speed Multi-Dimensional Packet Classifier
US	60/181364	2/8/2000	Queuing System for Processors in Packet Routing Operations
US	60/297107	6/7/2001	An Improved and Extended Family of Network Services Processors
US	60/482233	6/23/2003	Latency Independent Coherence Protocol
US	60/482230	6/23/2003	Latency Independent Coherence Protocol
US	60/502359	9/12/2003	Mechanism for Assuring Quality of Service for Programs Executing on a Multithread Processor
US	60/502358	9/12/2003	Mechanism for Assuring Quality of Service for Programs Executing on a Multithread Processor
US	60/499180	8/28/2003	Mechanism for Assuring Quality of Service for Programs Executing on a Multithread Processor
US	60/533331	12/29/2003	HYPERJTAG: Protocol and Design Providing Multiple Independent JTAG Debug Probe Connections to Multiple Processor Cores on One Integrated Circuit Through One Set of Signals
US	60/848047	9/29/2006	Data Cache Virtual Hint Way Prediction, and Applications Thereof
US	60/853314	9/29/2006	Twice Issued Conditional Move Instruction, and Applications Thereof
US	60/829099	10/11/2006	Horizontally-Shared Cache Victims in Multiple Core Processors
US	61/013265	12/12/2007	Coherent Instruction Cache Utilizing Cache-Op Execution Resources
US	61/051642	5/8/2008	Compact Instruction Set Architecture
US	61/148880	1/30/2009	System and Method for Improving Memory Transfer
US	61/436931	1/27/2011	Power Reduction Instruction Cache in a Multi-Thread Processor Core

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