PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4391335

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
NXP B.V.	04/12/2017

RECEIVING PARTY DATA

Name:	VLSI TECHNOLOGY LLC
Street Address:	1209 ORANGE STREET
City:	WILMINGTON
State/Country:	DELAWARE
Postal Code:	19801

PROPERTY NUMBERS Total: 15

Property Type	Number
Patent Number:	8120146
Patent Number:	9190611
Patent Number:	8004922
Patent Number:	8963219
Patent Number:	9318428
Patent Number:	6936877
Patent Number:	6150806
Patent Number:	7446598
Patent Number:	7506227
Patent Number:	7380186
Patent Number:	7746715
Patent Number:	8268672
Patent Number:	6791418
Patent Number:	8855187
Application Number:	60277736

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Email: paralegals@daylightlaw.com

Correspondent Name:	ERIC R. SCHEUERLEIN
Address Line 1:	626 JEFFERSON AVENUE, SUITE 7
Address Line 4:	SAN FRANCISCO, CALIFORNIA 94063

NAME OF SUBMITTER:	ERIC SCHEUERLEIN
SIGNATURE:	/Eric Scheuerlein/
DATE SIGNED:	04/29/2017

Total Attachments: 15

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PATENT ASSIGNMENT

WHEREAS, **NXP B.V.**, a corporation duly authorized under the laws of The Netherlands, with its registered office located at High Tech Campus 60, 5656 AG, Eindhoven, The Netherlands (hereinafter referred to as "Assignor"), is the owner, by assignment, of the entire right, title and interest in and to certain patents and applications listed in Schedule A (hereinafter referred to as "PATENTS"); and

WHEREAS, **VLSI Technology LLC**, a United States corporation duly authorized under the law of the State of Delaware, with its registered office located at Corporation Trust Center 1209 Orange Street, Wilmington, DE, 19801 (hereinafter referred to as "Assignee"), desires to acquire Assignor's entire right, title and interest in and to the **PATENTS**;

NOW, THEREFORE, for good, valuable and legally recognized consideration, the receipt of which is hereby acknowledged, Assignor does hereby assign, transfer and convey unto Assignee, its successors and assigns, its entire right, title and interest throughout the world in and to (a) the **PATENTS**; (b) all divisional, continuing, substitute, extension, reissue and other patent applications and applications for any other form of industrial property protection applicable thereto; (c) all patents and patent applications related to the **PATENTS** via terminal disclaimers; (d) the benefit of the right of priority provided by the International Convention for the Protection of Industrial Property, as amended, or by any convention which may henceforth be substituted for it; (e) the right to sue and obtain damages for past infringement of the **PATENTS**; and (f) any and all Letters Patent or other form of industrial property protection relating to the **PATENTS** now or hereafter granted, to be held and enjoyed by the Assignee to the full end of the term or terms for which said Letters Patent, patents or any other form of industrial property protection have been or may be granted, as fully and entirely as the same would have been held and enjoyed by Assignor, had this assignment not been made.

IN WITNESS WHEREOF, intending to be legally bound hereby, the Assignor and Assignee have duly executed this Assignment of Patent Application.

Signed this 12th day of April, 2017

NXP B.V.

By: _____

Jennifer Wuamett

Senior Vice President, Deputy General Counsel

On 04/12/17, before me, the undersigned Notary Public, personally appeared Jennifer Wuamett, personally known or proven to me to be the person who subscribed his/her name above in my presence to this instrument in his/her authorized capacity as the legal representative of the said corporation.

(Seal) SONIA GONGORA NOTARY PUBLIC STATE OF TEXAS ID 12851838-2 EXP. 02-10-2019

Name (Print/Type): Sonia Gongora

Notary Public

VLSI Technology LLC

By: _____

Michael Stolarski

CEO

On 4/22/17, before me, the undersigned Notary Public, personally appeared Michael Stolarski, personally known or proven to me to be the person who subscribed his/her name above in my presence to this instrument in his/her authorized capacity as the legal representative of the said corporation.

(Seal) JOHN RIVERA Official Seal Notary Public - State of Illinois My Commission Expires May 19, 2020

Name (Print/Type): John Rivera

Notary Public

Schedule A

VLSI Family	Family	Status	Title	Filed Date	Granted Date	Region	Application Number	Patent Number	Inventors
29	005105	Lapsed	Dielectric protection layer for precision resistors in integrated circuits	2006-02-10		EP	06101561.6		Joachim Stache | Rainer Hoffmann | Michael Burnus
29	005105	Lapsed	Dielectric protection layer for precision resistors in integrated circuits	2007-02-06		WO	IB2007/050393		Joachim Stache | Rainer Hoffmann | Michael Burnus
29	005105	Granted	Dielectric protection layer for precision resistors in integrated circuits	2007-02-06	2010-12-22	CN	200780004908.8	CN200780004908	Joachim Stache | Rainer Hoffmann | Michael Burnus
29	005105	Lapsed	Dielectric protection layer for precision resistors in integrated circuits	2007-02-06	2010-09-01	EP	07705804.8	EP1984939	Joachim Stache | Rainer Hoffmann | Michael Burnus
29	005105	Abandoned	Dielectric protection layer for precision resistors in integrated circuits	2007-02-06		JP	2008-553873		Joachim Stache | Rainer Hoffmann | Michael Burnus
29	005105	Granted	SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THEREOF	2007-02-06	2012-02-21	US	12/161786	US8120146	Joachim Stache | Rainer Hoffmann | Michael Burnus
29	005105	Granted	Dielectric protection layer for precision resistors in integrated circuits	2007-02-06	2010-09-01	FR	07705804.8	FR1984939	Joachim Stache | Rainer Hoffmann | Michael Burnus
29	005105	Granted	Dielectric protection layer for precision resistors in integrated circuits	2007-02-06	2010-09-01	DE	07705804.8	DE602007008841	Joachim Stache | Rainer Hoffmann | Michael Burnus
29	005105	Legally Abandoned	Dielectric protection layer for precision resistors in integrated circuits	2007-02-06	2010-09-01	GB	07705804.8	GB1984939	Joachim Stache | Rainer Hoffmann | Michael Burnus
40	81057800	Lapsed	Sub-lithography Phase Change line cell with nano-pillar	2007-06-28		EP	07111317.9		David Tio Castro | Almudena Huerta

VLSI Family	Family	Status	Title	Filed Date	Granted Date	Region	Application Number	Patent Number	Inventors
40	81057800	Lapsed	Sub-lithography Phase Change line cell with nano-pillar	2008-06-20		WO	IB2008/052441		David Tio Castro | Almudena Huerta
40	81057800	Granted	AN ELECTRONIC DEVICE, AND METHOD OF MANUFACTURING AN ELECTRONIC DEVICE	2008-06-20	2015-11-17	US	12/665840	US9190611	David Tio Castro | Almudena Huerta
40	81057800	Lapsed	Sub-lithography Phase Change line cell with nano-pillar	2008-06-20	2011-08-24	EP	08763398.8	EP2162931	David Tio Castro | Almudena Huerta
40	81057800	Granted	Sub-lithography Phase Change line cell with nano-pillar	2008-06-20	2011-12-14	CN	200880022320.X	CN200880022320	David Tio Castro | Almudena Huerta
40	81057800	Granted	Sub-lithography Phase Change line cell with nano-pillar	2008-06-20	2011-08-24	FR	08763398.8	FR2162931	David Tio Castro | Almudena Huerta
40	81057800	Granted	Sub-lithography Phase Change line cell with nano-pillar	2008-06-20	2011-08-24	DE	08763398.8	DE602008009136	David Tio Castro | Almudena Huerta
40	81057800	Granted	Sub-lithography Phase Change line cell with nano-pillar	2008-06-20	2011-08-24	GB	08763398.8	GB2162931	David Tio Castro | Almudena Huerta
25	81356003	Granted	POWER ISLAND WITH INDEPENDENT POWER CHARACTERISTICS FOR MEMORY AND LOGIC	2009-06-05	2011-08-23	US	12/479517	US8004922	David Evoy | Jose de Jesus Pineda de Gyvez | Peter Klapproth
25	81356003	Lapsed	Power island with direct supply to SRAM and local LDO supply to logic.	2010-06-07		WO	IB2010/052513		David Evoy | Jose de Jesus Pineda de Gyvez | Peter Klapproth
25	81356003	Granted	POWER ISLAND WITH INDEPENDENT POWER CHARACTERISTICS FOR MEMORY AND LOGIC	2010-06-07	2014-06-18	CN	201080024173.7	CN201080024173	David Evoy | Jose de Jesus Pineda de Gyvez | Peter Klapproth
25	81356003	Published	POWER ISLAND WITH INDEPENDENT POWER CHARACTERISTICS FOR MEMORY AND LOGIC	2010-06-07		EP	10730532.8		David Evoy | Jose de Jesus Pineda de Gyvez | Peter Klapproth

VLSI Family	Family	Status	Title	Filed Date	Granted Date	Region	Application Number	Patent Number	Inventors
37	81392479	Lapsed	Ultra low-power semiconductor switch	2010-10-11	2013-08-14	EP	10187157.2	EP2439777	Gilberto Curatola | Dusan Golubovic | Johannes Josephus Theodorus Marinus Donkers | Guillaume Boccardi | Hans Mertens
37	81392479	Granted	TUNNEL FIELD EFFECT TRANSISTOR	2011-10-11	2015-02-24	US	13/270898	US8963219	Gilberto Curatola | Dusan Golubovic | Johannes Josephus Theodorus Marinus Donkers | Guillaume Boccardi | Hans Mertens
37	81392479	Granted	Ultra low-power semiconductor switch	2010-10-11	2013-08-14	DE	10187157.2	DE602010009356	Gilberto Curatola | Dusan Golubovic | Johannes Josephus Theodorus Marinus Donkers | Guillaume Boccardi | Hans Mertens
41	AT040029	Lapsed	CHIPS WITH TWO GROUPS OF CHIP CONTACTS	2004-05-28		EP	04102408.4		Heimo Scheucher
41	AT040029	Lapsed	CHIPS WITH TWO GROUPS OF CHIP CONTACTS	2005-05-18		WO	IB2005/051613		Heimo Scheucher
41	AT040029	Granted	CHIPS WITH TWO GROUPS OF CHIP CONTACTS	2005-05-18	2010-08-11	CN	200580017250.5	CN200580017250	Heimo Scheucher
41	AT040029	Abandoned	CHIPS WITH TWO GROUPS OF CHIP CONTACTS	2005-05-18		KR	2006-7027518		Heimo Scheucher
41	AT040029	Granted	CHIP HAVING TWO GROUPS OF CHIP CONTACTS	2005-03-18	2016-04-19	US	11/628131	US9318428	Heimo Scheucher
41	AT040029	Lapsed	CHIPS WITH TWO GROUPS OF CHIP CONTACTS	2006-10-30	2012-01-11	EP	05747294.6	EP1754256	Heimo Scheucher

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41	AT040029	Abandoned	CHIPS WITH TWO GROUPS OF CHIP CONTACTS	2005-05-18		JP	2007-514239		Heimo Scheucher
41	AT040029	Granted	CHIPS WITH TWO GROUPS OF CHIP CONTACTS	2005-05-18	2012-01-11	FR	05747294.6	FR1754256	Heimo Scheucher
41	AT040029	Granted	CHIPS WITH TWO GROUPS OF CHIP CONTACTS	2005-05-18	2012-01-11	DE	05747294.6	DE602005032120	Heimo Scheucher
41	AT040029	Granted	CHIPS WITH TWO GROUPS OF CHIP CONTACTS	2005-05-18	2012-01-11	GB	05747294.6	GB1754256	Heimo Scheucher
10	DE010065	Abandoned	ELECTRONIC DEVICE	2002-03-15		CN	02801743.9		Mareike Klee | Rainer Kiewitt | Mike Ju | Wilfried Germer | Wolfgang Brand
10	DE010065	Abandoned	ELECTRONIC DEVICE	2002-03-15		EP	02705008.7		Mareike Klee | Rainer Kiewitt | Mike Ju | Wilfried Germer | Wolfgang Brand
10	DE010065	Granted	Integrated Circuit including a Capacitor with a High Capacitance Density	2002-03-19	2005-08-30	US	10/101328	US6936877	Mareike Klee | Rainer Kiewitt | Mike Ju | Wilfried Germer | Wolfgang Brand
10	DE010065	Lapsed	ELECTRONIC DEVICE	2001-03-21		US	60/277736		Mareike Klee | Rainer Kiewitt | Mike Ju | Wilfried Germer | Wolfgang Brand
10	DE010065	Lapsed	ELECTRONIC DEVICE	2002-03-15		WO	IB2002/000826		Mareike Klee | Rainer Kiewitt | Mike Ju | Wilfried Germer | Wolfgang Brand

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10	DE010065	Abandoned	ELECTRONIC DEVICE	2002-03-15		JP	2002-574697		Mareike Klee | Rainer Kiewitt | Mike Ju | Wilfried Germer | Wolfgang Brand
1	F 098585	Legally Abandoned	ENHANCED PNP CHARGE-PUMP		2004-01-21	DE	69914266.0	DE69914266	David Canard | Vincent Fillatre
1	F 098585	Lapsed	ENHANCED PNP CHARGE-PUMP	1999-08-10	2004-01-21	EP	99202607.0	EP0981203	David Canard | Vincent Fillatre
1	F 098585	Legally Abandoned	ENHANCED PNP CHARGE-PUMP		2004-01-21	FR	99202607.0	FR0981203	David Canard | Vincent Fillatre
1	F 098585	Lapsed	ENHANCED PNP CHARGE-PUMP	1998-08-18		FR	9810509		David Canard | Vincent Fillatre
1	F 098585	Legally Abandoned	ENHANCED PNP CHARGE-PUMP		2004-01-21	GB	99202607.0	GB0981203	David Canard | Vincent Fillatre
1	F 098585	Abandoned	ENHANCED PNP CHARGE-PUMP	1999-08-18		KR	1999-0034134		David Canard | Vincent Fillatre
1	F 098585	Granted	Controlled Current Source for Accelerated Switching	1999-08-18	2000-11-21	US	09/376862	US6150806	David Canard | Vincent Fillatre
1	F 098585	Abandoned	ENHANCED PNP CHARGE-PUMP	1999-08-17		JP	99-230943		David Canard | Vincent Fillatre
17	GB040187	Lapsed	CIRCUIT FOR THE PTAT BIASSING OF THE COLLECTOR CURRENT....	2004-09-15		GB	0420484.8		MICHIEL PERTIJS | Johan Hendrik Huijsing
17	GB040187	Lapsed	CIRCUIT FOR THE PTAT BIASSING OF THE COLLECTOR CURRENT....	2005-09-13		WO	IB2005/052991		MICHIEL PERTIJS | Johan Hendrik Huijsing
17	GB040187	Abandoned	CIRCUIT FOR THE PTAT BIASSING OF THE COLLECTOR CURRENT....	2005-06-19		GB	0507821.7		MICHIEL PERTIJS | Johan Hendrik Huijsing

VLSI Family	Family	Status	Title	Filed Date	Granted Date	Region	Application Number	Patent Number	Inventors
17	GB040187	Lapsed	CIRCUIT FOR THE PTAT BIASSING OF THE COLLECTOR CURRENT....	2005-09-13	2009-12-09	EP	05782924.4	EP1792245	MICHIEL PERTIJS | Johan Hendrik Huijsing
17	GB040187	Granted	CIRCUIT FOR THE PTAT BIASSING OF THE COLLECTOR CURRENT....	2005-09-13	2009-08-05	CN	200580030765.9	CN200580030765	MICHIEL PERTIJS | Johan Hendrik Huijsing
17	GB040187	Granted	Bias Circuits	2005-09-13	2008-11-04	US	11/575301	US7446598	MICHIEL PERTIJS | Johan Hendrik Huijsing
17	GB040187	Abandoned	CIRCUIT FOR THE PTAT BIASSING OF THE COLLECTOR CURRENT....			JP	2007-531912		MICHIEL PERTIJS | Johan Hendrik Huijsing
17	GB040187	Granted	CIRCUIT FOR THE PTAT BIASSING OF THE COLLECTOR CURRENT....	2005-09-13	2009-12-09	FR	05782924.4	FR1792245	MICHIEL PERTIJS | Johan Hendrik Huijsing
17	GB040187	Granted	CIRCUIT FOR THE PTAT BIASSING OF THE COLLECTOR CURRENT....	2005-09-13	2009-12-09	DE	05782924.4	DE602005018235	MICHIEL PERTIJS | Johan Hendrik Huijsing
17	GB040187	Granted	CIRCUIT FOR THE PTAT BIASSING OF THE COLLECTOR CURRENT....	2005-09-13	2009-12-09	GB	05782924.4	GB1792245	MICHIEL PERTIJS | Johan Hendrik Huijsing
18	NL020790	Abandoned	IC WITH ID CODES	2003-07-31		EP	03791083.3		Leon Van de Logt | Frans de Jong
18	NL020790	Lapsed	IC WITH ID CODES	2002-08-30		EP	02078568.9		Leon Van de Logt | Frans de Jong
18	NL020790	Legally Abandoned	IC WITH ID CODES	2003-08-27	2007-05-01	TW	092123606	TWI280379	Leon Van de Logt | Frans de Jong
18	NL020790	Granted	Integrated circuit with embedded identification code	2003-07-31	2009-03-17	US	10/525598	US7506227	Leon Van de Logt | Frans de Jong
18	NL020790	Lapsed	IC WITH ID CODES	2003-07-31		WO	IB2003/003387		Leon Van de Logt | Frans de Jong
18	NL020790	Abandoned	IC WITH ID CODES	2003-07-31		KR	2005-7003189		Leon Van de Logt | Frans de Jong

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18	NL020790	Legally Abandoned	IC WITH ID CODES	2003-07-31	2008-05-28	CN	03820257.3	CN03820257	Leon Van de Logt | Frans de Jong
18	NL020790	Legally Abandoned	IC WITH ID CODES	2003-07-31	2009-06-05	JP	2004-532373	JP4319142	Leon Van de Logt | Frans de Jong
15	NL030095	Lapsed	IEEE STD 1149.1 TAP WITH INTEGRATED SENSORS	2003-01-28		EP	03100172.0		Rodger Frank Schuttert | Frans de Jong
15	NL030095	Lapsed	IEEE STD 1149.1 TAP WITH INTEGRATED SENSORS	2003-12-18		WO	IB2003/006113		Rodger Frank Schuttert | Frans de Jong
15	NL030095	Lapsed	IEEE STD 1149.1 TAP WITH INTEGRATED SENSORS	2003-12-18	2009-11-25	EP	03777124.3	EP1590678	Rodger Frank Schuttert | Frans de Jong
15	NL030095	Legally Abandoned	IEEE STD 1149.1 TAP WITH INTEGRATED SENSORS	2003-12-18	2008-08-27	CN	200380109291.8	CN200380109291	Rodger Frank Schuttert | Frans de Jong
15	NL030095	Legally Abandoned	IEEE STD 1149.1 TAP WITH INTEGRATED SENSORS	2003-12-18		KR	2005-7013867		Rodger Frank Schuttert | Frans de Jong
15	NL030095	Granted	Boundary Scan Circuit with Integrated Sensor for Sensing Physical Operating Parameters	2003-12-18	2008-05-27	US	10/544058	US7380186	Rodger Frank Schuttert | Frans de Jong
15	NL030095	Legally Abandoned	IEEE STD 1149.1 TAP WITH INTEGRATED SENSORS	2003-12-18	2010-10-15	JP	04-567390	JP4606881	Rodger Frank Schuttert | Frans de Jong
15	NL030095	Legally Abandoned	IEEE STD 1149.1 TAP WITH INTEGRATED SENSORS		2009-11-25	FR	03777124.3	FR1590678	Rodger Frank Schuttert | Frans de Jong
15	NL030095	Legally Abandoned	IEEE STD 1149.1 TAP WITH INTEGRATED SENSORS		2009-11-25	DE	03777124.3	DE60330275	Rodger Frank Schuttert | Frans de Jong

VLSI Family	Family	Status	Title	Filed Date	Granted Date	Region	Application Number	Patent Number	Inventors
15	NL030095	Legally Abandoned	IEEE STD 1149.1 TAP WITH INTEGRATED SENSORS		2009-11-25	GB	03777124.3	GB1590678	Rodger Frank Schuttert | Frans de Jong
21	NL030977	Lapsed	IMPROVED ERASE AND READ SCHEME FOR CHARGE TRAPPING MEMORIES	2003-08-13		EP	03102529.9		MICHIEL van Duuren
21	NL030977	Legally Abandoned	IMPROVED ERASE AND READ SCHEME FOR CHARGE TRAPPING MEMORIES	2004-08-10		TW	093123954		MICHIEL van Duuren
21	NL030977	Lapsed	IMPROVED ERASE AND READ SCHEME FOR CHARGE TRAPPING MEMORIES	2004-08-04		WO	IB2004/051382		MICHIEL van Duuren
21	NL030977	Legally Abandoned	IMPROVED ERASE AND READ SCHEME FOR CHARGE TRAPPING MEMORIES	2004-08-04		EP	04744730.5		MICHIEL van Duuren
21	NL030977	Abandoned	IMPROVED ERASE AND READ SCHEME FOR CHARGE TRAPPING MEMORIES	2004-08-04		CN	200480022910.4		MICHIEL van Duuren
21	NL030977	Legally Abandoned	IMPROVED ERASE AND READ SCHEME FOR CHARGE TRAPPING MEMORIES	2004-08-04		KR	2006-7002939		MICHIEL van Duuren
21	NL030977	Granted	Erase and read schemes for charge trapping non-volatile memories	2004-08-04	2010-06-29	US	10/567070	US7746715	MICHIEL van Duuren
21	NL030977	Legally Abandoned	IMPROVED ERASE AND READ SCHEME FOR CHARGE TRAPPING MEMORIES	2004-08-04		JP	06-523097		MICHIEL van Duuren
33	NL040482	Lapsed	CHIP-ON-CHIP WITH IMMENSION SOLDERING BUMP	2004-05-06		EP	04101963.9		Co VAN VEEN | PieterMarian Hochstenbach

VLSI Family	Family	Status	Title	Filed Date	Granted Date	Region	Application Number	Patent Number	Inventors
33	NL040482	Abandoned	CHIP-ON-CHIP WITH IMMENSION SOLDERING BUMP	2005-05-03		TW	094114323		Co VAN VEEN | PieterMarian Hochstenbach
33	NL040482	Lapsed	CHIP-ON-CHIP WITH IMMENSION SOLDERING BUMP	2005-04-28		WO	IB2005/051397		Co VAN VEEN | PieterMarian Hochstenbach
33	NL040482	Abandoned	CHIP-ON-CHIP WITH IMMENSION SOLDERING BUMP	2005-04-28		EP	05732290.1		Co VAN VEEN | PieterMarian Hochstenbach
33	NL040482	Granted	CHIP-ON-CHIP WITH IMMENSION SOLDERING BUMP	2005-04-28	2010-01-20	CN	200580014194.X	CN200580014194	Co VAN VEEN | PieterMarian Hochstenbach
33	NL040482	Granted	Method of Assembly and Assembly Thus Made	2005-04-28	2012-09-18	US	11/579677	US8268672	Co VAN VEEN | PieterMarian Hochstenbach
33	NL040482	Granted	CHIP-ON-CHIP WITH IMMENSION SOLDERING BUMP	2005-04-28	2013-03-01	JP	2007-512626	JP5208500	Co VAN VEEN | PieterMarian Hochstenbach
7	US020364	Lapsed	CAPACITOR COUPLED DYNAMIC BIAS BOOSTING CIRCUIT FOR A...	2003-09-17	2006-08-09	EP	03798995.1	EP1550210	Sifen Luo | Tirdad Sowlati
7	US020364	Abandoned	CAPACITOR COUPLED DYNAMIC BIAS BOOSTING CIRCUIT FOR A...	2003-09-17		KR	2005-7005582		Sifen Luo | Tirdad Sowlati
7	US020364	Granted	CAPACITOR COUPLED DYNAMIC BIAS BOOSTING CIRCUIT FOR A...	2002-10-02	2004-09-14	US	10/262765	US6791418	Sifen Luo | Tirdad Sowlati
7	US020364	Lapsed	CAPACITOR COUPLED DYNAMIC BIAS BOOSTING CIRCUIT FOR A...	2003-09-17		WO	IB2003/004081		Sifen Luo | Tirdad Sowlati
7	US020364	Granted	CAPACITOR COUPLED DYNAMIC BIAS BOOSTING CIRCUIT FOR A...	2003-09-17	2009-04-08	CN	03823597.8	CN03823597	Sifen Luo | Tirdad Sowlati

VLSI Family	Family	Status	Title	Filed Date	Granted Date	Region	Application Number	Patent Number	Inventors
7	US020364	Granted	CAPACITOR COUPLED DYNAMIC BIAS BOOSTING CIRCUIT FOR A...	2003-09-17	2006-08-09	DE	03798995.1	DE60307492	Sifen Luo | Tirdad Sowlati
7	US020364	Granted	CAPACITOR COUPLED DYNAMIC BIAS BOOSTING CIRCUIT FOR A...	2003-09-17	2006-08-09	FR	03798995.1	FR1550210	Sifen Luo | Tirdad Sowlati
7	US020364	Granted	CAPACITOR COUPLED DYNAMIC BIAS BOOSTING CIRCUIT FOR A...	2003-09-17	2006-08-09	GB	03798995.1	GB1550210	Sifen Luo | Tirdad Sowlati
7	US020364	Abandoned	CAPACITOR COUPLED DYNAMIC BIAS BOOSTING CIRCUIT FOR A...	2003-09-17		JP	04-541042		Sifen Luo | Tirdad Sowlati

PATENT ASSIGNMENT

WHEREAS, **NXP B.V.**, a corporation duly authorized under the laws of The Netherlands, with its registered office located at High Tech Campus 60, 5656 AG, Eindhoven, The Netherlands (hereinafter referred to as "Assignor"), is the owner, by assignment, of the entire right, title and interest in and to certain patents and applications listed in Schedule A (hereinafter referred to as "PATENTS"); and

WHEREAS, **VLSI Technology LLC**, a United States corporation duly authorized under the law of the State of Delaware, with its registered office located at Corporation Trust Center 1209 Orange Street, Wilmington, DE, 19801 (hereinafter referred to as "Assignee"), desires to acquire Assignor's entire right, title and interest in and to the **PATENTS**;

NOW, THEREFORE, for good, valuable and legally recognized consideration, the receipt of which is hereby acknowledged, Assignor does hereby assign, transfer and convey unto Assignee, its successors and assigns, its entire right, title and interest throughout the world in and to (a) the **PATENTS**; (b) all divisional, continuing, substitute, extension, reissue and other patent applications and applications for any other form of industrial property protection applicable thereto; (c) all patents and patent applications related to the **PATENTS** via terminal disclaimers; (d) the benefit of the right of priority provided by the International Convention for the Protection of Industrial Property, as amended, or by any convention which may henceforth be substituted for it; (e) the right to sue and obtain damages for past infringement of the **PATENTS**; and (f) any and all Letters Patent or other form of industrial property protection relating to the **PATENTS** now or hereafter granted, to be held and enjoyed by the Assignee to the full end of the term or terms for which said Letters Patent, patents or any other form of industrial property protection have been or may be granted, as fully and entirely as the same would have been held and enjoyed by Assignor, had this assignment not been made.

IN WITNESS WHEREOF, intending to be legally bound hereby, the Assignor and Assignee have duly executed this Assignment of Patent Application.

Signed this 12th day of April, 2017

NXP B.V.

By: _____

Jennifer Wuamett

Senior Vice President, Deputy General Counsel

On 4/12/17, before me, the undersigned Notary Public, personally appeared Jennifer Wuamett, personally known or proven to me to be the person who subscribed his/her name above in my presence to this instrument in his/her authorized capacity as the legal representative of the said corporation.

(Seal) SONIA GONGORA NOTARY PUBLIC STATE OF TEXAS ID 128515592 EXP. 02-10-2019

Name (Print/Type): Sonia Gongora

Notary Public

VLSI Technology LLC

By: _____

Michael Stolarski

CEO

On 4/22/17, before me, the undersigned Notary Public, personally appeared Michael Stolarski, personally known or proven to me to be the person who subscribed his/her name above in my presence to this instrument in his/her authorized capacity as the legal representative of the said corporation.

JOHN RIVERA
Official Seal
Notary Public - State of Illinois
My Commission Expires May 19, 2020

(Seal)

Name (Print/Type): John Rivera

Notary Public

Schedule A

VLSI Family	Family	Status	Title	Filed Date	Granted Date	Region	Application Number	Patent Number	Inventors
1	81407899	Lapsed	SIGNAL PROCESSING METHOD	2011-01-12	2014-06-04	EP	11150750.5	EP2477418	Friedrich Reining
1	81407899	Abandoned	This invention covers a microphone component with a standard digital PDM interface and a software algorithm executed on the receiving side that augments the system dynamics.	2012-01-10		CN	201210005583.8		Friedrich Reining
1	81407899	Granted	SIGNAL PROCESSING METHOD FOR ENHANCING A DYNAMIC RANGE OF A SIGNAL	2012-01-09	2014-10-07	US	13/346031	US8855187	Friedrich Reining
1	81407899	Granted	This invention covers a microphone component with a standard digital PDM interface and a software algorithm executed on the receiving side that augments the system dynamics.	2011-01-12	2014-06-04	DE	11150750.5	DE602011007342	Friedrich Reining
1	81407899	Granted	This invention covers a microphone component with a standard digital PDM interface and a software algorithm executed on the receiving side that augments the system dynamics.	2011-01-12	2014-06-04	GB	11150750.5	GB2477418	Friedrich Reining
1	81407899	Granted	This invention covers a microphone component with a standard digital PDM interface and a software algorithm executed on the receiving side that augments the system dynamics.	2011-01-12	2014-06-04	FR	11150750.5	FR2477418	Friedrich Reining