PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4407819

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
ERYN SMITH	11/28/2016

RECEIVING PARTY DATA

Name:	WESTERN ALLIANCE BANK
Street Address:	55 ALMADEN BLVD., SUITE 100
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95113

PROPERTY NUMBERS Total: 4

Property Type	Number
Application Number:	14717839
Application Number:	13737221
Application Number:	29441627
Application Number:	14538183

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	09627-106
NAME OF SUBMITTER:	NOELLE D. AZZOPARDI
SIGNATURE:	/Noelle D. Azzopardi/
DATE SIGNED:	05/10/2017

Total Attachments: 9
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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This INTELLECTUAL PROPERTY SECURITY AGREEMENT, dated as of November 28, 2016 (the "Agreement") between WESTERN ALLIANCE BANK, an Arizona corporation ("Lender") and Eryn Smith ("Grantor") is made with reference to the Business Loan Agreement, dated as of November 28, 2016 (as amended from time to time, the "Loan Agreement"), between Lender and BEAM SERVICES, INC. ("Borrower"), and that certain Commercial Guaranty dated as of November 28, 2016, between Lender and Grantor (as amended from time to time, the "Guaranty"). Terms defined in the Loan Agreement have the same meaning when used in this Agreement.

For good and valuable consideration, receipt of which is hereby acknowledged, Grantor hereby covenants and agrees as follows:

To secure the Obligations under the Loan Agreement and Guaranty, Grantor grants to Lender a security interest in all right, title, and interest of Grantor in any of the following, whether now existing or hereafter acquired or created in any and all of the following property (collectively, the "Intellectual Property Collateral"):

(a) copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held (collectively, the "Copyrights"), including the Copyrights described in Exhibit A;

(b) trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks (collectively, the "Trademarks"), including the Trademarks described in Exhibit B;

(c) patents, patent applications and like protections including without limitation improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same (collectively, the "Patents"), including the Patents described in Exhibit C;

(d) mask work or similar rights available for the protection of semiconductor chips or other products (collectively, the "Mask Works");

(e) trade secrets, and any and all intellectual property rights in computer software and computer software products;

(f) design rights;

(g) claims for damages by way of past, present and future infringement of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works, and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i) amendments, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j) proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

The rights and remedies of Lender with respect to the security interests granted hereunder are in addition to those set forth in the Loan Agreement, and those which are now or hereafter available to Lender as a matter of law or equity. Each right, power and remedy of Lender provided for herein or in the Loan Agreement, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein, and the exercise by Lender of any one or more of such rights, powers or remedies does not preclude the simultaneous or later exercise by Lender of any other rights, powers or remedies.

IN WITNESS WHEREOF, the parties have executed this Agreement as of the date first written above.

GRANTOR:

ERYN SMITH

By: _____

Bryn Smith

Address for Notices:

Attn:

Tel: _____

Fax: _____

LENDER:

WESTERN ALLIANCE BANK, an Arizona corporation

By: _____

Name: _____

Title: _____

Address for Notices:

Attn:

55 Almaden Boulevard, Suite 100

San Jose, California 95113

Tel: (408) 556-6501

Fax:(408) 282-1681

EXHIBIT A

COPYRIGHTS

Please Check if No Copyrights Exist ☐

Type of Work:	Title:	International Standard Serial Number (ISSN):	Registration Number:	Filing Date:	Pre - registered?

EXHIBIT B

TRADEMARKS

Please Check if No Trademarks Exist ☐

Mark / Title:	U.S. Serial Number:	U.S. Registration Number:	USPTO Reference Number:	Filing Date:

EXHIBIT C

PATENTS

Please Check if No Patents Exist ☐

Title:	Patent Number:	Application Serial Number:	Issued or Published?	Issue Date:
Electrostatic Carrier	US 9,246,415 B2	13/737,221	P	1/26/16
Tri-Modal Carrier for Semiconductive Wafer	US 2015/0129021 A1	14/538,183	P	5/14/15
Electrostatic Carrier	US D689,835 S	29/441,627	P	9/17/13
mobile Electrostatic Tray Carrier for a semiconductive...	US 2015/0255321 A1	14/719,839	P	9/10/15

US 20150255320A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2015/0255320 A1

(43) Pub. Date: Sep. 10, 2015

Smith

(54) MOBILE ELECTROSTATIC CARRIER FOR A SEMICONDUCTIVE WAFER AND A METHOD OF USING THEREOF FOR SINGULATION OF THE SEMICONDUCTIVE WAFER

(71) Applicant: Eryn Smith, Pleasanton, CA (US)

(72) Inventor: Eryn Smith, Pleasanton, CA (US)

(21) Appl. No.: 14/717,839

(22) Filed: May 20, 2015

Related U.S. Application Data

(63) Continuation-in-part of application No. 14/538,183, filed on Nov. 11, 2014.

(60) Provisional application No. 62/001,503, filed on May 21, 2014, provisional application No. 61/902,591, filed on Nov. 11, 2013.

Publication Classification

(51) Int. Cl.

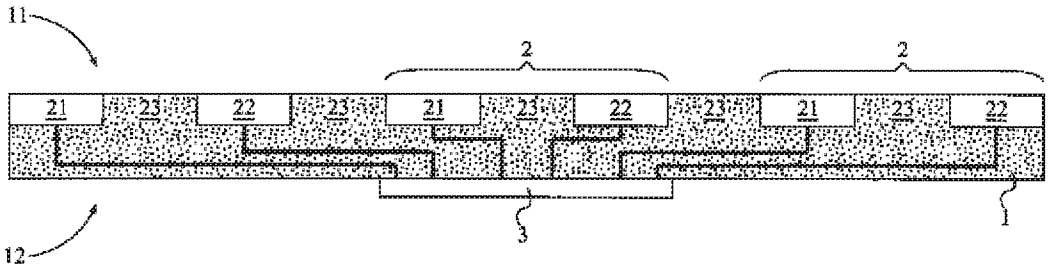
H01L 21/683	(2006.01)
H01L 21/3065	(2006.01)
H01L 21/78	(2006.01)

(52) U.S. Cl.

CPC *H01L 21/6835* (2013.01); *H01L 21/6831* (2013.01); *H01L 21/78* (2013.01); *H01L 21/3065* (2013.01); *H01L 2221/68327* (2013.01); *H01L 2221/68381* (2013.01)

(57) ABSTRACT

A mobile electrostatic carrier (MESC) provides a structural platform to temporarily bond a semiconductive wafer and can be used to transport the semiconductive wafer or be used to perform manufacturing processes on the semiconductive wafer. The MESC uses a plurality of electrostatic field generating (EFG) circuits to generate electrostatic fields across the MESC that allow the MESC to bond to compositional impurities within the semiconductive process. The MESC is particularly useful during singulation for a wafer fabrication process. The MESC holds the semiconductive wafer in a constant position as the semiconductive wafer is cut into a plurality of dies. Once the MESC is discharges its EFG circuits and consequently dissipates its bonding electrostatic fields, the plurality of dies can be easily and readily removed from the MESC.



(12) **United States Patent**
Smith

(10) **Patent No.: US 9,246,415 B2**
(45) **Date of Patent: Jan. 26, 2016**

(54) **ELECTROSTATIC CARRIER TRAY**

(71) Applicant: **Eryn Smith**, Pleasanton, CA (US)

(72) Inventor: **Eryn Smith**, Pleasanton, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 134 days.

(21) Appl. No.: **13/737,221**

(22) Filed: **Jan. 9, 2013**

(65) **Prior Publication Data**

US 2014/0055907 A1 Feb. 27, 2014

Related U.S. Application Data

(60) Provisional application No. 61/691,508, filed on Aug. 21, 2012.

(51) Int. Cl.

H02N 13/00	(2006.01)
H01L 21/673	(2006.01)
H01L 21/683	(2006.01)

(52) U.S. Cl.

CPC ***H02N 13/00*** (2013.01); ***H01L 21/67333*** (2013.01); ***H01L 21/6833*** (2013.01)

(58) **Field of Classification Search**

CPC . H02N 3/00; H01L 21/67333; H01L 21/6833
USPC 361/234
See application file for complete search history.

(56) **References Cited**

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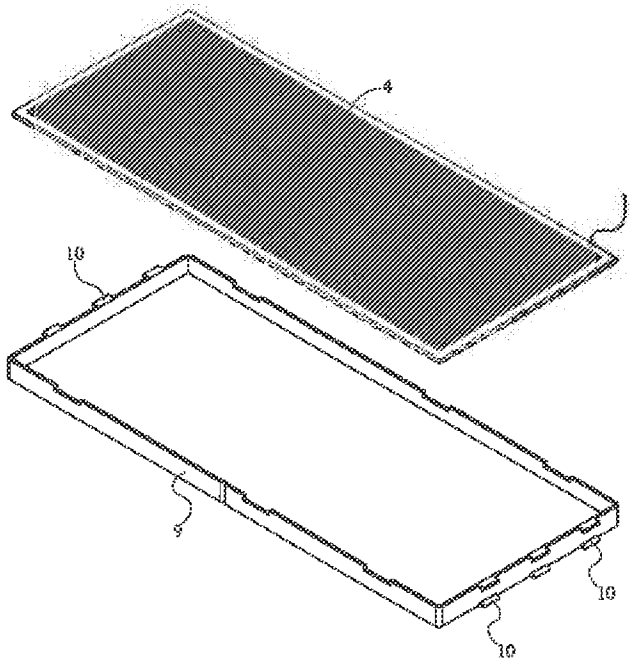
* cited by examiner

Primary Examiner — Thienvu Tran
Assistant Examiner — Kevin J Comber

(57) **ABSTRACT**

An electrostatic carrier tray is an apparatus that is used to temporarily grasp and to transport semiconductive coupons/wafers. The apparatus mainly includes a primary substrate, a plurality of electrostatics field generating circuits, a conformal coating, a structural backing, and a power-delivery and control system. The electrostatics field generating circuits are positioned on one side of the primary substrate, and the power delivery and control system is positioned on the other side of the primary substrate. The electrostatics field generating circuits are used to bond the semiconductive coupons/wafers to the apparatus. The structural backing is used to handle the apparatus while transporting the semiconductive coupons/wafers and is also used to protect the power-delivery and control system from physical damage. The conformal coating is superimposed onto the electrostatics field generating circuits and the primary substrate as a means of protection.

9 Claims, 9 Drawing Sheets



US00D689835S

(12) United States Design Patent

Smith

(10) Patent No.: US D689,835 S
(45) Date of Patent: ** Sep. 17, 2013

(54) **ELECTROSTATIC CARRIER TRAY**

(71) Applicant: **Eryn Smith**, Pleasanton, CA (US)

(72) Inventor: **Eryn Smith**, Pleasanton, CA (US)

(**) Term: **14 Years**

(21) Appl. No.: **29/441,627**

(22) Filed: **Jan. 8, 2013**

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; 439/65, 70–74, 330, 331, 439/620.2; 414/935–941; 118/500, 728, 118/729; 156/345.51, 345.52, 345.53; 279/128; 361/230, 233, 234
See application file for complete search history.

(56) **References Cited**

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Primary Examiner — Elizabeth J Oswecki
(74) *Attorney, Agent, or Firm* — Sinorica, LLC

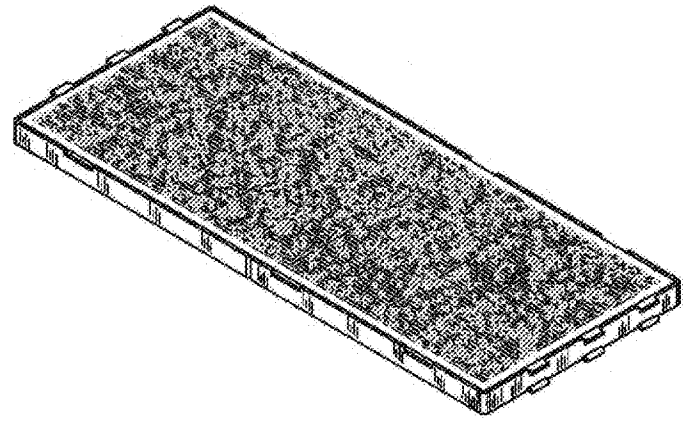
(57) **CLAIM**

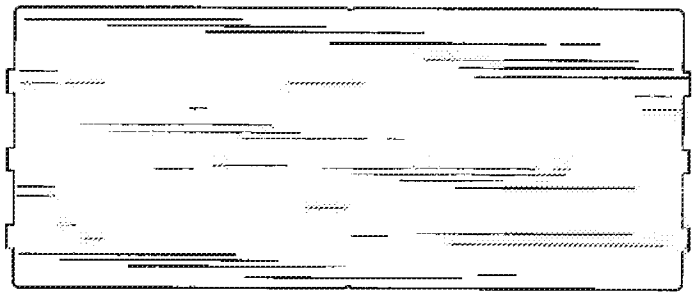
The ornamental design for an electrostatic carrier tray, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of an electrostatic carrier tray showing my new design;
FIG. **2** is a front elevational view thereof;
FIG. **3** is a rear elevational view thereof;
FIG. **4** is a right-side elevational view thereof;
FIG. **5** is a left-side elevational view thereof;
FIG. **6** is a bottom plan view thereof;
FIG. **7** is a top plan view thereof;
FIG. **8** is an exploded perspective view thereof;
FIG. **9** is a perspective view thereof shown in a used condition wherein a plurality of substrates is electrostatically bonded to the plurality of electrostatic field generating circuits; and,
FIG. **10** is a cross-sectional view thereof taken along line **10-10** of FIG. **7**.
The broken lines illustrate the plurality of substrates in FIG. **9** and are included to show environmental structure that forms no part of the claimed design.

1 Claim, 10 Drawing Sheets





US 20150129121A1

(19) United States

(12) Patent Application Publication

Smith

(10) Pub. No.: US 2015/0129121 A1

(43) Pub. Date: May 14, 2015

(54) TRI-MODAL CARRIER FOR A SEMICONDUCTIVE WAFER

(71) Applicant: Eryn Smith, Pleasanton, CA (US)

(72) Inventor: Eryn Smith, Pleasanton, CA (US)

(21) Appl. No.: 14/538,183

(22) Filed: Nov. 11, 2014

Related U.S. Application Data

(60) Provisional application No. 61/902,591, filed on Nov. 11, 2013.

Publication Classification

(51) Int. Cl.
H01L 21/683 (2006.01)

(52) U.S. Cl.
CPC *H01L 21/6833* (2013.01)

(57) ABSTRACT

A tri-modal carrier provides a structural platform to temporarily bond a semiconductive wafer and can be used to transport the semiconductive wafer or be used to perform manufacturing processes on the semiconductive wafer. The tri-modal carrier includes a doped semiconductive substrate, a plurality of electrostatic field generating (EFG) circuits, and a capacitance charging interface. A positive pole and a negative pole from each EFG circuit are embedded into the doped semiconductive substrate. An exposed portion of the doped semiconductive substrate is located between the positive pole and the negative pole, which is used as a biased pole for each EFG circuit. The combination of these poles for each EFG circuit is used to generate a non-uniform electrostatic field for bonding the semiconductive wafer. The tri-modal carrier also uses flat surface properties and the removal of trapped gas particles to strengthen the bond between the tri-modal carrier and the semiconductive wafer.