

## PATENT ASSIGNMENT COVER SHEET

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<b>SUBMISSION TYPE:</b>	NEW ASSIGNMENT
<b>NATURE OF CONVEYANCE:</b>	ASSIGNMENT
<b>CONVEYING PARTY DATA</b>	
<b>Name</b>	<b>Execution Date</b>
FREESCALE SEMICONDUCTOR, INC.	05/09/2014
<b>RECEIVING PARTY DATA</b>	
<b>Name:</b>	INVENSAS CORPORATION
<b>Street Address:</b>	3025 ORCHARD PARKWAY
<b>City:</b>	SAN JOSE
<b>State/Country:</b>	CALIFORNIA
<b>Postal Code:</b>	95134
<b>PROPERTY NUMBERS Total: 1</b>	
<b>Property Type</b>	<b>Number</b>
<b>Application Number:</b>	15607888
<b>CORRESPONDENCE DATA</b>	
<b>Fax Number:</b>	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
<b>Phone:</b>	214-651-5000
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<b>Correspondent Name:</b>	MICHAEL SHENKER
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<b>ATTORNEY DOCKET NUMBER:</b>	48259.219US05
<b>NAME OF SUBMITTER:</b>	MICHAEL SHENKER
<b>SIGNATURE:</b>	/ Michael Shenker, Reg. No. 34,250 /
<b>DATE SIGNED:</b>	05/30/2017
<b>Total Attachments: 3</b>	
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source=48259.219US05 Assignment Freescale to Invensas#page2.tif	
source=48259.219US05 Assignment Freescale to Invensas#page3.tif	

DEED OF ASSIGNMENT

THIS DEED OF ASSIGNMENT ("Assignment"), EFFECTIVE AS OF 5/9<sup>th</sup>, 2014, IS MADE BY AND BETWEEN

Freescale Semiconductor, Inc. (hereinafter "ASSIGNOR"), a Delaware corporation with its principal place of business located at 6501 William Cannon Drive West, Austin, TX, 78735; and

Invensas Corporation (hereinafter "BUYER"), a Delaware corporation having a place of business at 3025 Orchard Parkway, San Jose, California 95134, United States.

WHEREAS:

- A ASSIGNOR is the sole owner in respect of the patents and patent applications listed in the attached Appendix (hereinafter "the PATENTS"); and
- B BUYER is desirous of acquiring all of the worldwide right, title and interest in and to the PATENTS and the inventions disclosed therein.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, ASSIGNOR has sold, assigned and transferred, and does hereby sell, assign and transfer to BUYER all of the worldwide right, title and interest in (i) the PATENTS and the inventions and improvements disclosed therein; (ii) all reissues, divisionals, continuations, continuations-in-part, extensions, renewals, reexaminations and foreign counterparts thereof, and other patents, patent applications, certificates of invention other governmental grants resulting from the PATENTS; (iii) all patents and applications which claim priority to or have common disclosure or common priority with any such patents or patent applications, and (iv) all rights corresponding to any of the foregoing throughout the world (including the right to claim the priority date of any of the PATENTS and the right to sue for and recover damages for any past, present or future infringement of the Patents, and including all benefits, privileges and powers), the same to be held and enjoyed by BUYER for its own use and enjoyment, and for the use and enjoyment of its successors, assigns and other legal representatives, to the end of the term or terms of said PATENTS granted or reissued or reexamined as fully and entirely as the same would have been held and enjoyed by ASSIGNOR, if this assignment and sale had not been made.

IN WITNESS WHEREOF, ASSIGNOR has caused these presents to be signed by its duly appointed officer having full authority to convey its property.

And if the issue date and/or patent number of any of the PATENTS is unknown to ASSIGNOR and BUYER at the time this Assignment is executed, ASSIGNOR does hereby authorize its attorneys to insert on this Assignment the issue date and patent number of said any patent when known.

ASSIGNOR hereby declares that BUYER may take the steps for recordal of this assignment in the sole name of BUYER.

ASSIGNOR hereby undertakes that it shall, without further consideration, but at the expense of BUYER, execute all documents and do all such acts and things as BUYER may in its absolute discretion consider necessary or desirable to enable Letters Patent or any other form of protection to be issued in respect of any of said PATENTS and the inventions disclosed therein in any part of the world and to enable or to assist BUYER to defend oppositions thereto, to maintain the PATENTS and to prosecute for the infringement thereof.

SIGNED for and on behalf of

ASSIGNOR

By [Signature] on May 7, 2014  
(Signature) (Date)

Changhae Park, VP of IP Licensing  
(Print Name and Title)

State of

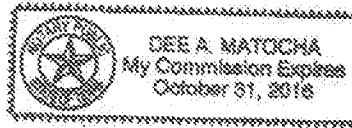
County of )

On this 7<sup>th</sup> day of May, 2014 before me, [Signature] Dee A. Matocha, personally appeared Changhae Park, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the instrument and acknowledged to me that he/she executed the same in his/her authorized capacity and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

[Signature]  
(Notary Public)



APPENDIX - LISTED PATENTS AND PATENT APPLICATIONS

Family #	US Patent No.	US Appl. No.	Filing Date	Issue Date	Title
1	7803714	12/059123	31-Mar-2008	28-Sep-2010	SEMICONDUCTOR THROUGH SILICON VIAS OF VARIABLE SIZE AND METHOD OF FORMATION
2	7935571	12/277512	25-Nov-2008	03-May-2011	THROUGH SUBSTRATE VIAS FOR BACK-SIDE INTERCONNECTIONS ON VERY THIN SEMICONDUCTOR WAFERS
	8283207	13/043094	08-Mar-2011	09-Oct-2012	METHODS OF FORMING THROUGH-SUBSTRATE CONDUCTOR FILLED VIAS, AND ELECTRONIC ASSEMBLIES FORMED USING SUCH METHODS
3	8344503	12/277519	25-Nov-2008	01-Jan-2013	3-D CIRCUITS WITH INTEGRATED PASSIVE DEVICES
	Issue Fee Paid	13/731242	31-Dec-2012	TBD	METHODS OF FORMING 3-D CIRCUITS WITH INTEGRATED PASSIVE DEVICES
4	8039386	12/748101	26-Mar-2010	18-Oct-2011	METHOD FOR FORMING A THROUGH SILICON VIA (TSV)
5	7446017	11/444091	31-May-2006	04-Nov-2008	METHODS AND APPARATUS FOR RF SHIELDING IN VERTICALLY-INTEGRATED SEMICONDUCTOR DEVICES