PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4447265

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
DIABLO TECHNOLOGIES, INC.	02/17/2015

RECEIVING PARTY DATA

Name:	CITY NATIONAL BANK
Street Address:	555 SOUTH FLOWER STREET
Internal Address:	18TH FLOOR
City:	LOS ANGELES
State/Country:	CALIFORNIA
Postal Code:	90071

PROPERTY NUMBERS Total: 8

Property Type	Number
Application Number:	15262462
Application Number:	15251147
Application Number:	14452473
Application Number:	14452477
Application Number:	14694487
Application Number:	14664580
Application Number:	13303048
Application Number:	11720024

CORRESPONDENCE DATA

Fax Number: (703)382-6486

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 7033826485
Email: DHall@VLPLawGroup.com
Correspondent Name: DAVIS HALL
Address Line 1: 1301 N COURTHOUSE ROAD, UNIT 502
Address Line 4: ARLINGTON, VIRGINIA 22201

ATTORNEY DOCKET NUMBER:	CNB-DIABLO TECHNOLOGIES
NAME OF SUBMITTER:	DAVIS HALL

SIGNATURE:	/DavisHall/
DATE SIGNED:	06/06/2017

Total Attachments: 11

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INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement ("Agreement") is entered into as of February 17, 2015 by and between CITY NATIONAL BANK ("Bank") and DIABLO TECHNOLOGIES, INC. ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated September 4, 2014 (the "Closing Date") (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works (as each term is described below) to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

1. Grant of Security Interest. To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "Intellectual Property Collateral"), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "Copyrights");

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and

continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the "Patents");

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto (collectively, the "Trademarks");

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the "Mask Works");

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing; provided, that (A) the security interests granted herein shall not extend to any rights under any license of Grantor to the extent that the granting of a security interest therein would, under the express terms of such license, be prohibited or restricted or result in a breach of the terms of, constitute a default under or result in a termination of any such license governing such rights, unless (x) such prohibition or restriction is not enforceable or is otherwise ineffective under applicable law or (y) consent to such security interest has been obtained from any applicable third party; provided however, that upon termination of such prohibition or restriction, such interest shall immediately become Intellectual Property Collateral without any action by Grantor or Bank; and (B) any United States intent-to-use trademark applications shall not be considered Intellectual Property Collateral to the extent that, and solely during the period in which, the grant of a security interest therein would impair the validity or enforceability of or render void or result in the cancellation of, any registration issued as a result of such intent-to-use trademark applications under applicable law; provided, that upon submission and acceptance by the United States Patent and Trademark Office of an amendment to allege use pursuant to 15 U.S.C. Section 1051(d) (or any successor provision), such intent-to-use trademark application shall be considered "Intellectual Property Collateral."

2. Recordation. Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement upon request by Bank.

Grantor hereby authorizes Bank to (a) modify this Agreement unilaterally by amending the exhibits to this Agreement to include any Intellectual Property Collateral which Grantor obtains subsequent to the date of this Agreement and (b) file a duplicate original of this Agreement containing amended exhibits reflecting such new Intellectual Property Collateral.

3. Loan Documents. This Agreement has been entered into pursuant to and in conjunction with the Loan Agreement, which is hereby incorporated by reference. The provisions of the Loan Agreement shall supersede and control over any conflicting or inconsistent provision herein. The rights and remedies of Bank with respect to the Intellectual Property Collateral are as provided by the Loan Agreement and related documents, and nothing in this Agreement shall be deemed to limit such rights and remedies.

4. Execution in Counterparts. This Agreement may be executed in counterparts (and by different parties hereto in different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a signature page to this Agreement by facsimile or in electronic (i.e., "pdf" or "tif" format) shall be effective as delivery of a manually executed counterpart of this Agreement.

5. Successors and Assigns. This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

6. Governing Law. This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby and thereby shall be governed by, and construed in accordance with, the laws of the United States and the State of California, without giving effect to any choice or conflict of law provision or rule (whether of the State of California or any other jurisdiction).

[Signature page follows.]

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

DIABLO TECHNOLOGIES, INC.
TECHNOLOGIES DIABLO INC.

By: _____

Title: _____

BANK:

CITY NATIONAL BANK

_____

By: _____

Title: _____

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

DIABLO TECHNOLOGIES, INC.
TECHNOLOGIES DIABLO INC.

By: _____

Title: _____

BANK:

CITY NATIONAL BANK

By: _____

Title: SVP

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date
NONE		

EXHIBIT B

Patents

Description	Registration/ Application Number	Registration/ Application Date
SYSTEM AND METHOD OF INTERFACING CO-PROCESSORS AND INPUT/OUTPUT DEVICES VIA A MAIN MEMORY SYSTEM	20160378404 15262462	12/29/2016 09/12/2016
SYSTEM AND METHOD FOR OFFSETTING THE DATA BUFFER LATENCY OF A DEVICE IMPLEMENTING A JEDEC STANDARD DDR4 LRDIMM CHIPSET	20160371204 15251147	12/22/2016 08/30/2016
SYSTEM AND METHOD FOR IMPLEMENTING A MULTI-THREADED DEVICE DRIVER IN A COMPUTER SYSTEM	20160041933 14452473	02/11/2016 08/05/2014
SYSTEM AND METHOD FOR MIRRORING A VOLATILE MEMORY OF A COMPUTER SYSTEM	20160041917 14452477	02/11/2016 08/05/2014
SYSTEM AND METHOD OF INTERFACING CO-PROCESSORS AND INPUT/OUTPUT DEVICES VIA A MAIN MEMORY SYSTEM	9,444,495 20150309959 14635960	09/13/2016 10/29/2015 03/02/2015
SYSTEM AND METHOD FOR OFFSETTING THE DATA BUFFER LATENCY OF A DEVICE IMPLEMENTING A JEDEC STANDARD DDR-4 LRDIMM CHIPSET	20150294696 14664580	10/15/2015 03/20/2015
LOAD REDUCTION DUAL IN-LINE MEMORY MODULE (LRDIMM) AND METHOD FOR PROGRAMMING THE SAME	9,465,557 20150227324 14691051	10/11/2016 08/13/2015 04/20/2015
LOAD REDUCTION DUAL IN-LINE MEMORY MODULE (LRDIMM) AND METHOD FOR PROGRAMMING THE SAME	9,015,408 20140244924 14270293	04/21/2015 08/28/2014 05/05/2014
SYSTEM AND METHOD FOR PROVIDING A COMMAND BUFFER IN A MEMORY SYSTEM	9,552,175 20140237205 14265280	01/24/2017 08/21/2014 04/29/2014
SYSTEM AND METHOD FOR UNLOCKING ADDITIONAL FUNCTIONS OF A MODULE	9,575,908 20140237176 14265241	02/21/2017 08/21/2014 04/29/2014
SYSTEM AND METHOD FOR PROVIDING AN ADDRESS CACHE FOR MEMORY MAP LEARNING	20140237157 14265270	08/21/2014 04/29/2014

SYSTEM AND METHOD OF INTERFACING CO-PROCESSORS AND INPUT/OUTPUT DEVICES VIA A MAIN MEMORY SYSTEM	8,972,805	03/03/2015
	20140223262	08/07/2014
	14247162	04/07/2014
LOAD REDUCTION DUAL IN-LINE MEMORY MODULE (LRDIMM) AND METHOD FOR PROGRAMMING THE SAME	8,738,853	05/27/2014
	20130238849	09/12/2013
	13873633	04/30/2013
SYSTEM AND METHOD OF INTERFACING CO-PROCESSORS AND INPUT/OUTPUT DEVICES VIA A MAIN MEMORY SYSTEM	8,713,379	04/29/2014
	20120204079	08/09/2012
	13303048	11/22/2011
LINEAR PHASE INTERPOLATOR AND PHASE DETECTOR	8,218,705	07/10/2012
	20090103675	04/23/2009
	12081380	04/15/2008
VOLTAGE CONTROLLED OSCILLATOR (VCO) WITH A WIDE TUNING RANGE AND SUBSTANTIALLY CONSTANT VOLTAGE SWING OVER THE TUNING RANGE	7,777,581	08/17/2010
	20090102525	04/23/2009
	11984852	11/23/2007
FULLY ADAPTIVE EQUALIZATION FOR HIGH LOSS COMMUNICATIONS CHANNELS	7,940,839	05/10/2011
	20080260016	10/23/2008
	10597455	01/26/2005
	PCT/CA2005/000078	01/26/2005
RECEIVER-BASED ADAPTIVE EQUALIZER WITH PRE-CURSOR COMPENSATION	8,081,677	12/20/2011
	11720024	11/22/2005
	PCT/CA2005/001765	11/22/2005
	WO2006/056048	06/01/2006
PROGRAMMABLE ASYNCHRONOUS FIRST-IN-FIRST-OUT (FIFO) STRUCTURE WITH MERGING CAPABILITY	7,796,652	09/14/2010
	20070258491	11/08/2007
	11790707	04/27/2007
OPERATING FREQUENCY REDUCTION FOR TRANSVERSAL FIR FILTER	7,889,786	02/15/2011
	20070147559	06/28/2007
	10569825	08/27/2004
	PCT/CA04/01571	08/27/2004
LOAD REDUCTION DUAL IN-LINE MEMORY MODULE (LRDIMM) AND METHOD FOR PROGRAMMING THE SAME	8,452,917	05/28/2013
	20100070690	03/18/2010
	12559185	09/14/2009
BANG-BANG PHASE DETECTOR WITH SUB-RATE CLOCK	8,315,349	11/20/2012
	12258440	10/26/2008
MULTIPLE REFERENCE PHASE LOCKED LOOP	7,902,886	03/08/2011
	12259315	10/28/2008

SYSTEM AND METHOD OF ACCESSING AND CONTROLLING A CO-PROCESSOR AND/OR INPUT/OUTPUT DEVICE VIA REMOTE DIRECT MEMORY ACCESS	20150326684 14271838	11/12/2015 05/07/2014
SYSTEM AND METHOD OF IMPLEMENTING AN OBJECT STORAGE DEVICE ON A COMPUTER MAIN MEMORY SYSTEM	20150324281 1471773	11/12/2015 05/07/2014
SYSTEM AND METHOD FOR BOOTING FROM A NON-VOLATILE MEMORY	20150347151 14289547	12/03/2015 05/28/2014
SYSTEM AND METHOD FOR IMPLEMENTING A MULTI-THREADED DEVICE DRIVER IN A COMPUTER SYSTEM	14452473	
SYSTEM AND METHOD FOR MIRRORING A VOLATILE MEMORY OF A COMPUTER SYSTEM	14452477	
SYSTEM AND METHOD OF INTERFACING CO-PROCESSORS AND INPUT/OUTPUT DEVICES VIA A MAIN MEMORY SYSTEM	61457233	
SYSTEM AND METHOD FOR OFFSETTING THE DATA BUFFER LATENCY OF A DEVICE IMPLEMENTING A JEDEC STANDARD	61/968,998	
SYSTEM AND METHOD FOR PROVIDING A CONFIGURABLE TIMING CONTROL FOR A MEMORY SYSTEM	61/983,386	
SYSTEM AND METHOD OF INTERFACING CO-PROCESSORS AND INPUT/OUTPUT DEVICES VIA A MAIN MEMORY SYSTEM (MCI)	PCT/CA2012/000110	
SYSTEM AND METHOD FOR PROVIDING A CONFIGURABLE TIMING CONTROL FOR A MEMORY SYSTEM	20150310898 14694487	10/29/2015 04/23/2015
System and Method for Offsetting The Data Buffer Latency of a Device Implementing a JEDEC Standard DDR4 LRDIMM Chipset	9,449,651 20150294698 14664580	09/20/2016 10/15/2015 03/20/2015
SYSTEM AND METHOD OF INTERFACING COPROCESSORS AND INPUT/OUTPUT DEVICES VIA A MAIN MEMORY SYSTEM	20120204079 13303048	08/09/2015 11/22/2011
Receiver Based Adaptive Equalizer with PreCursor Compensation	20080240223 11720024	10/02/2008 11/22/2005

EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date
MEMORY1	86822364	11/17/2015
MEMORY CHANNEL INTERFACE (dead mark)	*85896033*	*04/05/2013*
FLASHDIMM (dead mark)	*85893537*	*04/02/2013*
MEGADIMM (dead mark)	*85893536*	*04/02/2013*
TERADIMM	85893534	04/02/2013
MCI	85893533	04/02/2013
MEMORY CHANNEL STORAGE	85893531	04/02/2013
MCS	85893530	04/02/2013

EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date
NONE		