

PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
UNITED TEST AND ASSEMBLY CENTER LIMITED	05/08/2015
RECEIVING PARTY DATA	
Name:	UTAC HEADQUARTERS PTE. LTD.
Street Address:	22 ANG MO KIO INDUSTRIAL PARK 2
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State/Country:	SINGAPORE
Postal Code:	569506
PROPERTY NUMBERS Total: 8	
Property Type	Number
Patent Number:	7476569
Patent Number:	8426246
Application Number:	62009309
Application Number:	62037128
Application Number:	62043276
Application Number:	14615436
Application Number:	62062967
Application Number:	62081541
CORRESPONDENCE DATA	
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NAME OF SUBMITTER:	CARMEN S. NG
SIGNATURE:	/Carmen S. Ng/

PATENT

DATE SIGNED:	11/01/2017
Total Attachments: 5 source=USG-UHQ Assignment#page1.tif source=USG-UHQ Assignment#page2.tif source=USG-UHQ Assignment#page3.tif source=USG-UHQ Assignment#page4.tif source=USG-UHQ Assignment#page5.tif	

ASSIGNMENT

This agreement makes reference to the Assignment Agreement made the 8th day of May 2015 between **United Test and Assembly Center Limited** and **UTAC Headquarters Pte. Ltd.**

United Test and Assembly Center Limited, a corporation of **Singapore**, having its registered office at **22 Ang Mo Kio Industrial Park 2, Singapore 569506** (hereinafter "Assignor"), is the owner of US Patents as those set out and particularized in Annex A (hereinafter "Patents"), and US Patent Applications as those set out and particularized in Annex B (hereinafter "Patent Applications").

UTAC Headquarters Pte. Ltd., a corporation of **Singapore**, having its registered office at **22 Ang Mo Kio Industrial Park 2, Singapore 569506** (hereinafter "Assignee"), desires to acquire the entire rights in and to the Patents and Patent Applications.

Therefore, for good and valuable consideration, Assignor hereby sells or has sold, assigns or has assigned, and transfers or has transferred to Assignee, its successors, assigns and legal representatives, all rights, title and interests in and for the United States and all foreign countries, in and to any and all improvements which are disclosed in the Patents and Patent Applications,

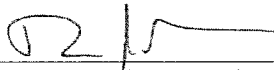
and in and to said Patents and Patent Applications and all other patent applications including divisional, continuing substitute, renewal, reissue, and all other applications for Letters Patent which may have been or will be filed in the United States and all foreign countries on any of said improvements; and in and to all original and reissued patents which may have been or shall be filed in the United States and all foreign countries on said improvements.

Assignor agrees that Assignee may apply for and receive Letters Patent for said improvements in its own name, and that, when requested, at the expense of said Assignee,

their successors, assigns, and legal representatives to carry out in good faith the intent and purpose of this agreement, the undersigned will execute all divisional, continuing substitute, renewal, reissue, and all other patent applications on any and all said improvements; execute all rightful oaths, assignments, powers of attorney and other papers; communicate to said Assignee, its successors, assigns, and representatives, all facts known to the undersigned relating to said improvements and the history thereof; and generally do everything possible which said Assignee, its successors, assigns, or representatives shall consider desirable for aiding in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements and all applications for patents and all patents on said improvements, in said Assignee, its successors, assigns, and legal representatives.


Assignor covenants with said Assignee, its successors, assigns and legal representatives that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Effective Date: 8 May 2015



(Signature)

Douglas DEVINE
for and on behalf of United
Test and Assembly Center
Limited

Witness 1:


(Signature)
LEE Ming Jason
(Print name)

Item #	US Patent Number	Title of Invention
1	6921974	Packaged Device with Thermal Enhancement and Method of Packaging
2	7023076	Multiple Chip Semiconductor Packages
3	7109570	Integrated Circuit Package with Leadframe Enhancement and Method of Manufacturing the Same
4	7323769	High Performance Chip Scale Leadframe Package and Method of Manufacturing the Package
5	7339278	Cavity Chip Package
6	7345357	High Density Chip Scale Leadframe Package and Method of Manufacturing the Package
7	7361995	Molded High Density Electronic Packaging Structure for High Performance Applications
8	7375416	Leadframe Enhancement and Method of Producing a Multi-row Semiconductor Package
9	7443041	Packaging of a Microchip Device
10	7476569	Leadframe Enhancement and Method of Producing a Multi-row Semiconductor Package
11	7642638	Inverted Lead Frame on Substrate
12	7678610	Semiconductor Chip Package and Method of Manufacture
13	7723833	Stacked Die Packages
14	7816775	Die Stacking Option In Conventional Lead Frame Package and Method of Manufacturing
15	7824960	Method of Assembly of a Silicon Stack Semiconductor Package
16	7830006	Structurally Enhanced Integrated Circuit Package and Method of Manufacture
17	7883938	Stacked Die Semiconductor Package and Method of Assembly
18	8030761	Mold Design and Method of Packaging a Semiconductor Package
19	7948095	Semiconductor Package and Method of Making the Same
20	8030768	Semiconductor package with under bump metallization aligned with open vias
21	8039951	Thermally Enhanced Semiconductor Package and Method of Producing the same
22	8115292	Interposer for Semiconductor Package
23	8129222	High Density Chip Scale Leadframe Package and Method of Manufacturing the Package
24	8143719	Vented Die and Package
25	8247272	Copper On Organic Solderability Preservative (OSP) Interconnect and Enhanced Wire Bonding Process
26	8288862	Multiple Die Stack Package
27	8384203	Packaging Structural Member
28	8399985	Mold Design and Method of Packaging a Semiconductor Package
29	8426246	Vented Die and Package
30	8544755	Hybrid SIM card
31	8586465	Through Silicon Via Dies and Packages
32	8647924	Semiconductor Package and Method Of Packaging Semiconductor Devices
33	8703534	SEMICONDUCTOR PACKAGES AND METHODS OF PACKAGING SEMICONDUCTOR DEVICES
34	8716873	Semiconductor packages and methods of packaging semiconductor devices
35	8741762	THROUGH SILICON VIA DIES AND PACKAGES
36	8772921	Interposer for Semiconductor Package
37	8829666	Semiconductor Packages and Methods of Packaging Semiconductor Devices
38	8860079	Semiconductor Packages and Methods of Packaging Semiconductor Devices
39	8916422	SEMICONDUCTOR PACKAGES AND METHODS OF PACKAGING SEMICONDUCTOR DEVICES
40	8816482	Leadframe Design to Improve Mold Flow of Flip Chip in Leadframe Package


17 June 2016

Item #	US Patent Application Number	Title of Invention
1	11846658	Method of Producing a Semiconductor Package
2	13681302	Leadframe Area Array Packaging Technology
3	13737923	PACKAGING STRUCTURAL MEMBER
4	13802769	SEMICONDUCTOR PACKAGES AND METHODS OF PACKAGING SEMICONDUCTOR DEVICES
5	14051417	SEMICONDUCTOR PACKAGES AND METHODS FOR FORMING SEMICONDUCTOR PACKAGE
6	14094763	SEMICONDUCTOR PACKAGES AND METHODS OF PACKAGING SEMICONDUCTOR DEVICES
7	14257017	Semiconductor packages and methods of packaging semiconductor devices
8	14257013	SEMICONDUCTOR PACKAGES AND METHODS OF PACKAGING SEMICONDUCTOR DEVICES
9	62009309	WLCSP HAVING PROTECTIVE LAYER THEREON
10	62037128	WLCSP having protective layer thereon
11	62042276	A semiconductor package having routing traces therein
12	14521481	SEMICONDUCTOR PACKAGES AND METHODS OF PACKAGING SEMICONDUCTOR DEVICES
13	14561157	SEMICONDUCTOR PACKAGES AND METHODS OF PACKAGING SEMICONDUCTOR DEVICES
14	14615436	RELIABLE INTERCONNECT
15	62062967	METHOD OF SINGULATING SEMICONDUCTOR CHIPS
16	62081541	WLCSP Sidewall Protection
17	14678840	Leadframe Area Array Packaging Technology