PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT4684395

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
RAMTRON INTERNATIONAL CORPORATION	12/03/2012

RECEIVING PARTY DATA

Name:	Cypress Semiconductor Corporation
Street Address:	198 Champion Court
City:	San Jose
State/Country:	CALIFORNIA
Postal Code:	95134

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	14077971

CORRESPONDENCE DATA

Fax Number: (408)545-6911

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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ATTORNEY DOCKET NUMBER:	RTN11001C1
NAME OF SUBMITTER:	CHRISTOPHER JORDAN
SIGNATURE:	/Christopher Jordan/
DATE SIGNED:	11/10/2017

Total Attachments: 10
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CORPORATE ASSIGNMENT

RAMTRON INTERNATIONAL CORPORATION, a corporation duly organized under and pursuant to the laws of **DELAWARE** and having its principal place of business at **1850 RAMTRON DRIVE, COLORADO SPRINGS, COLORADO 80921-3620** (hereafter referred to as the "Assignor"), is the owner by respective assignment of the Issued Patents and Pending Patent Applications set forth in **SCHEDULE A**, attached hereto (hereafter referred to as the "Patents and Applications").

CYPRESS SEMICONDUCTOR CORPORATION, a corporation duly organized under and pursuant to the laws of **DELAWARE** and having its principal place of business at **198 CHAMPION COURT, SAN JOSE, CALIFORNIA 95134-1709** (hereafter referred to as the "Assignee"), desires to acquire the entire right, title, and interest in and to the Patents and Applications.

THEREFORE, in consideration of the sum of One Dollar ($1.00) and other good and sufficient consideration, the receipt of which is hereby acknowledged, the Assignor hereby sells, assigns, transfers, and sets over to the Assignee, its successors, legal representatives and assigns the entire right, title and interest in and to the Patents and Applications and all inventions described and claimed therein, the right to file applications on the inventions, and the entire right, title and interest in and to any applications for Letters Patent of the United States or other countries claiming priority to the Patents and Applications, including divisionals, continuations, and continuations-in-part of the Patents and Applications, and reissues, reexaminations, renewals and extensions of the Patents or Letters Patents, and any and all Letters Patent or Patents of the United States of America and all foreign countries that may be granted therefor and thereon, and all rights under the International Convention for the Protection of Industrial Property, the same to be held and enjoyed by the Assignee, for its own use and behalf and the use and behalf of its successors, legal representatives, and assigns, to the full end of the term or terms for which the Patents and Applications have been granted, and for which Letters Patent or Patents may be granted, as fully and entirely as the same would have been held and enjoyed by the Assignor had the present sale and assignment not been made.

By its undersigned representative, the Assignor agrees:

a. to execute all papers necessary in connection with the Patents and Applications and any continuations, continuations-in-part, divisionals, reissues, reexaminations or corresponding applications thereof in any country, and also to execute separate assignments in connection with such application as the Assignee may deem necessary or expedient;

b. to execute all papers necessary in connection with any interference that may be declared concerning the Patents and Applications or any continuations, continuations-in-part, divisionals, reissues or reexaminations thereof, and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such interference; and

c. to perform all affirmative acts and take all lawful oaths that may be necessary or required to obtain a grant of a valid patent to the Assignee on the Patents and Applications and on any continuations, continuations-in-part, divisionals, reissues or reexaminations of the Patents and Applications in any country, and for the procurement, maintenance, enforcement, and defense of Letters Patent or Patents for the inventions described and claimed therein, without charge to the Assignee, its successors, legal representatives, and assigns, but at the cost and expense of the Assignee, its successors, legal representatives, and assigns.

The Assignor hereby covenants that, at the time of execution and delivery of the present assignment, the Assignor is the sole and lawful owner of the entire right, title, and interest in and to the inventions set forth in the Patents and Applications identified above, and has the full and complete right, title, and interest to convey the entire interest herein assigned, and that it has not executed, and will not execute, any agreement in conflict therewith.

The undersigned has reviewed the documents in the Patents and Applications identified above, and, to the best of undersigned's knowledge and belief, title is in the Assignor identified above.

The undersigned is empowered to sign this assignment on behalf of the Assignor.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Patents and Applications, corresponding applications or any patents issuing thereon.

IN WITNESS WHEREOF, executed by the Assignor's undersigned representative on the date following the undersigned's name.

RAMTRON INTERNATIONAL CORPORATION

By: _____

Brad W. Buss

Title: Director and Secretary

Date: December 3, 2012

ASSIGNMENT
SCHEDULE A

PATENT OR APPL NO.	RAMTRON REFERENCE NO.	FILING DATE	ISSUE DATE	TITLE	INVENTORS
5,371,699	RAM 360	11/17/1992	12/6/1994	Non-Volatile Ferroelectric Memory with Folded Bit Lines and Method of Making the Same	William LARSON
5,438,023	RAM 379	3/11/1994	8/1/1995	Passivation Method and Structure for a Ferroelectric Integrated Circuit using Hard Ceramic Materials or the Like	George ARGOS Jr. John D. SPANO Steven D. TRAYNOR
5,475,248	RAM 358 FWC2	9/8/1994	12/12/1995	Semiconductor Device with a Conductive Reaction-Preventing Film	Kazuhiro TAKENAKA
5,523,595	RAM 352 FWC	5/6/1994	6/4/1996	Semiconductor Device having a Transistor, a Ferroelectric Capacitor and a Hydrogen Barrier Film	Kazuhiro TAKENAKA Akira FUJISAWA
5,530,668	RAM 370	4/12/1995	6/25/1996	Ferroelectric Memory Sensing Scheme using Bit Lines Precharged to a Logic One Voltage	Wen-Foo CHERN Dennis WILSON
5,572,459	RAM 371	9/16/1994	11/5/1996	Voltage Reference for a Ferroelectric 1T/1C Based Memory	Dennis R. WILSON H. Brett MEADOWS
5,578,867	RAM 379 DIV	2/27/1995	11/26/1996	Passivation Method and Structure using Hard Ceramic Materials or the Like	George ARGOS Jr. John D. SPANO Steven D. TRAYNOR
5,592,410	RAM 384	4/10/1995	1/7/1997	Circuit and Method for Reducing a Compensation of a Ferroelectric Capacitor by Multiple Pulsing of the Plate Line Following a Write Operation	Donald J. VERHAEGHE Steven D. TRAYNOR
5,598,366	RAM 387	8/16/1995	1/28/1997	Ferroelectric Nonvolatile Random Access Memory Utilizing Self-Bootstrapping Plate Line Segment Drivers	William F. KRAUS Dennis R. WILSON
5,608,246	RAM 368 FWC	9/8/1995	3/4/1997	Integration of High Value Capacitor with Ferroelectric Memory	Michael W. YEAGER Dennis R. WILSON
5,800,683	RAM 396 DIV	5/22/1997	9/1/1998	Use of Calcium and Strontium Dopants to Improve Retention Performance in a PZT Ferroelectric Film	Lee KAMMERDINER Tom DAVENPORT Domokos HADNAGY
5,815,430	RAM 384 DIV	8/1/1996	9/29/1998	Circuit and Method for Reducing Compensation of a Ferroelectric Capacitor by Multiple Pulsing of the Plate Line Following a Write Operation	Donald J. VERHAEGHE Steven D.TRAYNOR
5,818,771	RAM 409	9/30/1996	10/6/1998	Semiconductor Memory Device	Yoshihiko YASU Hiroyuki SAKAI Michael W. YEAGER Donald J. VERHAEGHE
5,852,376	RAM 405	8/23/1996	12/22/1998	Bandgap Reference Based Power-On Detect Circuit Including a Supression Circuit	William F. KRAUS
5,854,568	RAM 424	8/20/1997	12/29/1998	Voltage Boost Circuit and Operation Thereof at Low Power Supply Voltages	Gary Peter MOSCALUK

PATENT OR APPL NO.	RAMTRON REFERENCE NO.	FILING DATE	ISSUE DATE	TITLE	INVENTORS
5,864,932	RAM 407 CIP	10/11/1996	2/2/1999	Partially or Completely Encapsulated Top Electrode of a Ferroelectric Capacitor	Thomas A. EVANS George ARGOS Jr.
5,866,926	RAM 357 FWC	7/19/1993	2/2/1999	Ferroelectric Memory Device with Capacitor Electrode in Direct Contact with Source Region	Kazuhiro TAKENAKA
5,880,989	RAM 414	11/14/1997	3/9/1999	Sensing Methodology for a 1T/1C Ferroelectric Memory	Dennis R. WILSON William F. KRAUS Lark Edward LEHMAN
5,889,428	RAM 386	6/6/1995	3/30/1999	Low Loss, Regulated Charge Pump with Integrated Ferroelectric Capacitors	Dennis YOUNG
5,892,728	RAM 437	11/14/1997	4/6/1999	Column Decoder Configuration for a 1T/1C Ferroelectric Memory	Judith E. ALLEN Dennis R. WILSON Joseph J. PERKALIS
5,902,131	RAM 415	5/9/1997	5/11/1999	Dual-Level Metalization Method for Integrated Circuit Ferroelectric Devices	George ARGOS Tatsuya YAMAZAKI
5,909,624	RAM 368 DIV	10/18/1995	6/1/1999	Method of Making Integration of High Value Capacitor with Ferroelectric Memory	Michael W. YEAGER Dennis R. WILSON
5,920,453	RAM 407	8/20/1996	7/6/1999	Completely Encapsulated Top Electrode of a Ferroelectric Capacitor	Thomas A. EVANS George ARGOS Jr.
5,956,266	RAM 433	11/14/1997	9/21/1999	Reference Cell for a 1T/1C Ferroelectric Memory	Dennis R. WILSON William F. KRAUS Lark E. LEHMAN Steven D. TRAYNOR
5,969,935	RAM 396	3/15/1996	10/19/1999	Use of Calcium and Strontium Dopants to Improve Retention Performance in a PZT Ferroelectric Film	Lee KAMMERDINER Tom DAVENPORT Domokos HADNAGY
5,969,980	RAM 436	11/14/1997	10/19/1999	Sense Amplifier Configuration for a 1T/1C Ferroelectric Memory	Judith E. ALLEN Dennis R. WILSON Lark E. LEHMAN
5,978,251	RAM 439	11/14/1997	11/2/1999	Plate Line Driver Circuit for a 1T/1C Ferroelectric Memory	William F. KRAUS Donald J. VERHAEGHE
5,986,919	RAM 435	11/14/1997	11/16/1999	Reference Cell Configuration for a 1T/1C Ferroelectric Memory	Judith E. ALLEN William F. KRAUS Dennis R. WILSON Lark E. LEHMAN
5,995,406	RAM 440	11/14/1997	11/30/1999	Plate Line Segmentation in a 1T/1C Ferroelectric Memory	William F. KRAUS Lark E. LEHMAN
6,008,659	RAM 397	3/15/1996	12/28/1999	Method of Measuring Retention Performance and Imprint Degradation of Ferroelectric Films	Steven TRAYNOR
6,027,947	RAM 407 CIP2	3/27/1997	2/22/2000	Partially or Completely Encapsulated Top Electrode of a Ferroelectric Capacitor	Thomas A. EVANS George ARGOS Jr.
6,028,783	RAM 434	11/14/1997	2/22/2000	Memory Cell Configuration for a 1T/1C Ferroelectric Memory	Judith E. ALLEN William F. KRAUS Lark E. LEHMAN

PATENT OR APPL NO.	RAMTRON REFERENCE NO.	FILING DATE	ISSUE DATE	TITLE	INVENTORS
6,141,237	RAM 456	7/12/1999	10/31/2000	Ferroelectric Non-Volatile Latch Circuits	Jarrod ELIASON Willaim F. KRAUS
6,150,184	RAM 407 CIP2 DIV	2/15/2000	11/21/2000	Method of Fabricating Partially or Completely Encapsulated Top Electrode of a Ferroelectric Capacitor	Thomas A. EVANS George ARGOS Jr.
6,174,735	RAM 444	10/23/1998	1/16/2001	Method of Manufacturing Ferroelectric Memory Device Useful for Preventing Hydrogen Line Degradation	Thomas A. EVANS
6,185,123	RAM 434 CON	12/17/1999	2/6/2001	Memory Cell Configuration for a 1T/1C Ferroelectric Memory	Judith E. ALLEN William F. KRAUS Lark E. LEHMAN
6,190,926	RAM 399 DIV	7/19/1999	2/20/2001	Yield Enhancement Technique for Integrated Circuit Processing to Reduce Effects of Undesired Dielectric Moisture Retention and Subsequent Hydrogen Out-Diffusion	Stanley C. PERINO Sanjay MITRA George ARGOS Holli HARPER
6,201,726	RAM 444 DIV	6/5/2000	3/13/2001	Ferroelectric Memory Device Structure Useful for Preventing Hydrogen Line Degradation	Thomas A. EVANS
6,203,608	RAM 442	4/15/1998	3/20/2001	Ferroelectric Thin Films and Solutions: Compositions	Shan SUN Thomas Domokos HADNAGY Tom E. DAVENPORT Hiroto UCHIDA Tsutomu ATSUKI Gakuji UOZUMI Kensuke KEGEYAMA Katsumi OGI
6,211,542	RAM 407 CIP3	5/27/1998	4/3/2001	Completely Encapsulated Top Electrode of a Ferroelectric Capacitor using a Lead-Enhanced Escapsulation Layer	Brian Lee EASTEP Thomas A. EVANS
6,242,299	RAM 454	4/1/1999	6/5/2001	Barrier Layer to Protect a Ferroelectric Capacitor After Contact Has Been Made to the Capacitor Electrode	George HICKERT
6,249,014	RAM 446	10/1/1998	6/19/2001	Hydrogen Barrier Encapsulation Techniques for the Control of Hydrogen Induced Degradation of Ferroelectric Capacitors in Conjunction with Multilevel Metal Processing for Non-Volatile Integrated Circuit Memory Devices	Richard A. BAILEY
6,252,793	RAM 435 CON	9/15/2000	6/26/2001	Reference Cell Configuration for a 1T/1C Ferroelectric Memory	Judith E. ALLEN William F. KRAUS Lark E. LEHMAN Dennis R. WILSON
6,263,398	RAM 422	2/10/1998	7/17/2001	Integrated Circuit Memory Device Incorporating a Non-Volatile Memory Array and a Relatively Faster Access Time Memory Cache	Craig TAYLOR Donald G. CARRIGAN Mike ALWAIS
6,275,425	RAM 478	11/16/2000	8/14/2001	Ferroelectric Voltage Boost Circuits	Jarrod ELIASON

PATENT OR APPL NO.	RAMTRON REFERENCE NO.	FILING DATE	ISSUE DATE	TITLE	INVENTORS
6,287,637	RAM 421 CIP2	10/27/1999	9/11/2001	Multi-Layer Approach for Optimizing Ferroelectric Film Performance	Fan CHU Glen FOX Brian EASTEP
6,358,755	RAM 444 DIV2	8/17/2000	3/19/2002	Ferroelectric Memory Device Structure Useful for Preventing Hydrogen Line Degradation	Thomas A. EVANS
6,362,675	RAM 462	7/11/2000	3/26/2002	Nonvolatile Octal Latch and D-Type Register	Michael ALWAIS
6,376,259	RAM 483	3/21/2001	4/23/2002	Method for Manufacturing a Ferroelectric Memory Cell Including Co-Annealing	Fan CHU Glen FOX
6,430,093	RAM 495	5/24/2001	8/6/2002	CMOS Boosting Circuit Utilizing Ferroelectric Capacitors	Jarrod ELIASON William A. KRAUS
6,445,608	RAM 485	9/10/2001	9/3/2002	Ferroelectric Random Access Memory Configurable Output Driver Circuit	Kurt SCHWARTZ Michael ALWAIS
6,459,609	RAM 500	12/13/2001	10/1/2002	Self Referencing 1T/1C Ferroelectric Random Access Memory	Xiao Hong DU
6,495,413	RAM 479	2/28/2001	12/17/2002	Structure for Masking Integrated Capacitors of Particular Utility for Ferroelectric Memory Integrated Circuits	Shan SUN George HICKERT Diana JOHNSON John ORTEGA Eric DALE Masahisa UEDA
6,535,446	RAM 477	5/24/2001	3/18/2003	Two Stage Low Voltage Ferroelectric Boost Circuit	Gary MOSCALUK
6,538,914	RAM 497	4/1/2002	3/25/2003	Ferroelectric Memory with Bit-Plate Parallel Architecture and Operating Method Thereof	Yeonbae CHUNG
6,560,137	RAM 436 CON	1/16/2001	5/6/2003	Sense Amplifier Configuration for a 1T/1C Ferroelectric Memory	Judith E. ALLEN Lark LEHMAN Dennis R. WILSON
6,597,028	RAM 480	6/4/2001	7/22/2003	Capacitively Coupled Ferroelectric Random Access Memory Cell and a Method for Manufacturing the Same	Thomas EVANS Glen FOX
6,613,586	RAM 446 DIV	2/13/2001	9/2/2003	Hydrogen Barrier Encapsulation Techniques for the Control of Hydrogen Induced Degradation of Ferroelectric Capacitors in Conjunction with Multilevel Metal Processing for Non-Volatile Integrated Circuit Memory Devices	Richard A. BAILEY
6,650,158	RAM 493	2/12/2002	11/18/2003	Ferroelectric Non-Volatile Logic Elements	Jarrod ELIASON
6,661,696	RAM 485 CON	8/28/2002	12/9/2003	Ferroelectric Random Access Memory Configurable Output Driver Circuit	Kurt SCHWARTZ Michael ALWAIS
6,682,772	RAM 467	4/24/2000	1/27/2004	High Temperature Deposition of Pt/TiOx for Bottom Electrodes	Glen R. FOX Kou-Kou SUU

PATENT OR APPL NO.	RAMTRON REFERENCE NO.	FILING DATE	ISSUE DATE	TITLE	INVENTORS
6,717,839	RAM 507	3/31/2003	4/6/2004	Bit-Line Shielding Method for Ferroelectric Memories	Xiao Hong DU
6,728,093	RAM 503	7/3/2002	4/27/2004	Method for Producing Crystallographically Textured Electrodes for Textured PZT Capacitors	Glen FOX
6,853,535	RAM 502	7/3/2002	2/8/2005	Method for Producing Crystallographically Textured Electrodes for Textured PZT Capacitors	Glen R. FOX Thomas DAVENPORT
6,856,573	RAM 437 CON	3/13/2003	2/15/2005	Column Decoder Configuration for a 1T/1C Memory	Judith E. ALLEN Dennis R. WILSON Joseph J. PERKALIS
6,894,549	RAM 493 DIV	7/3/2003	5/17/2005	Ferroelectric Non-Volatile Logic Elements	Jarrod ELIASON
7,116,572	RAM 515	11/9/2004	10/3/2006	Circuit for Generating a Centered Reference Voltage for a 1T/1C Ferroelectric Memory	Shan SUN Xiao-Hong DU Fan CHU Bob SOMMERVOLD
7,120,220	RAM 514	12/23/2004	10/10/2006	Non-Volatile Counter	Xiao-Hong DU Craig TAYLOR
7,142,627	RAM 514 CIP	3/17/2005	11/28/2006	Counting Scheme with Automatic Point-of-Reference Generation	Xiao-Hong DU Craig TAYLOR
7,176,824	RAM 511	11/21/2003	2/13/2007	Imprint-Free Coding for Ferroelectric Nonvolatile Counters	Xiao Hong DU Dennis C. YOUNG
7,271,744	RAM 511 CON	12/14/2006	9/18/2007	Imprint-Free Coding for Ferroelectric Nonvolatile Counters	Xiao Hong DU Dennis C. YOUNG
7,313,010	RAM 515 DIV	6/23/2006	12/25/2007	Circuit for Generating a Centered Reference Voltage for a 1T/1C Ferroelectric Memory	Shan SUN Xiao-Hong DU Fan CHU Bob SOMMERVOLD
7,570,090	RAM 527	10/30/2007	8/4/2009	Fast Power-On Detect Circuit with Accurate Trip-Points	Xiao Hong DU
7,652,909	RAM 528	10/21/2007	1/26/2010	2T/2C Ferroelectric Random Access Memory with Complementary Bit-Line Loads	Xiao Hong DU
7,672,151	RAM 555	7/10/1989	3/2/2010	Method for Reading Non-Volatile Ferroelectric Capacitor Memory Cell	Joseph T. EVANS William D. MILLER Richard H. WOMACK
7,924,599	RAM 556	11/29/1989	4/12/2011	Non-Volatile Memory Circuit using Ferroelectric Capacitor Storage Element	Joseph T. EVANS William D. MILLER Richard H. WOMACK
8,081,500	RAM 531	03/31/2009	12/20/2011	Method for Mitigating Imprint in a Ferroelectric Memory	Craig TAYLOR Fan CHU Shan SUN
12/833,817	RAM 601	7/9/2010	N/A	Low Power, Low Pin Count Interface for an RFID Transponder	Mark R. WHITAKER

PATENT OR APPL NO.	RAMTRON REFERENCE NO.	FILING DATE	ISSUE DATE	TITLE	INVENTORS
12/833,836	RAM 602	7/9/2010	N/A	Fast Block Write using an Indirect Memory Pointer	Mark R. WHITAKER Doug D. MORAN Robert John CLARKE Alexander Antony John ROACH
12/833,845	RAM 603	7/9/2010	N/A	RFID Access Method using an Indirect Memory Pointer	Mark R. WHITAKER Danny Lee SECREST
12/833,861	RAM 604	7/9/2010	N/A	Interrupt Generation and Acknowledgment for RFID	Mark R. WHITAKER Leslie Joseph MARENTETTE
13/355,145	RAM 607	1/20/2012	N/A	Authenticating Ferroelectric Random Access Memory (F-Ram) Device and Method	Kurt S. SCHWARTZ Michael BORZA Qiadao LI
13/490,163	RAM 608	6/6/2012	N/A	Generation of Voltage Supply for Low Power Digital Circuit Operation	Agustin OCHOA
13/490,254	RAM 609	6/6/2012	N/A	Dynamic Power Clamp for RFID Power Control	Agustin OCHOA Howard TANG
13/490,115	RAM 610	6/6/2012	N/A	Power-On Sequencing for an RFID Tag	Agustin OCHOA Howard TANG
13/490,267	RAM 611	6/6/2012	N/A	Analog Delay Cells for the Power Supply of an RFID Tag	Agustin OCHOA
13/490,236	RAM 612	6/6/2012	N/A	Bandgap Ready Circuit	Agustin OCHOA
13/490,285	RAM 613	6/6/2012	N/A	Dynamic Adjusting RFID Demodulation Circuit	Agustin OCHOA Bardia PISHDAD
13/490,296	RAM 614	6/6/2012	N/A	Shunt Regulator Circuit having Split Output	Agustin OCHOA Howard TANG
13/467,831	RAM 615	5/9/2012	N/A	Stack Processor using a Ferroelectric Random Access Memory (F-RAM) for Both Code and Data Space	Franck FILLERE
13/467,849	RAM 616	5/9/2012	N/A	Stack Processor using a Ferroelectric Random Access Memory (F-RAM) for Code Space and a Portion of the Stack Memory Space	Franck FILLERE
13/467,874	RAM 617	5/9/2012	N/A	Stack Processor using a Ferroelectric Random Access Memory (F-RAM) for Code Space and a Portion of the Stack Memory Space having an Instruction Set Optimized to Minimize Processor Stack Accesses	Franck FILLERE
13/467,816	RAM 618	5/9/2012	N/A	Stack Processor using a Ferroelectric Random Access Memory (F-RAM) having an Instruction Set Optimized to Minimize Memory Fetch Operations	Franck FILLERE

PATENT OR APPL NO.	RAMTRON REFERENCE NO.	FILING DATE	ISSUE DATE	TITLE	INVENTORS
13/470,117	RAM 623	5/11/2012	N/A	Enhanced Hydrogen Barrier Encapsulation Method for the Control of Hydrogen Induced Degradation of Ferroelectric Capacitors in an F-RAM Process	Shan SUN Tom E. DAVENPORT
13/569,735	RAM 626	8/8/2012	N/A	Method for Fabricating a Damascene Self-Aligned Ferrorelectric Random Access Memory (F-Ram) Device Structure Employing Reduced Processing Steps	John CRONIN Shan SUN Tom E. DAVENPORT
13/569,755	RAM 627	8/8/2012	N/A	Method for Fabricating a Damascene Self-Aligned Ferrorelectric Random Access Memory (F-Ram) with Simultaneous Formation of Sidewall Ferroelectric Capacitors	John CRONIN Shan SUN Tom E. DAVENPORT
13/569,785	RAM 628	8/8/2012	N/A	Method for Fabricating a Damascene Self-Aligned Ferrorelectric Random Access Memory (F-RAM) having a Ferroelectric Capacitor Aligned with a Three Dimensional Transistor Structure	John CRONIN Shan SUN Tom E. DAVENPORT