PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
UTAC THAI LIMITED	05/08/2015

RECEIVING PARTY DATA

Name:	UTAC HEADQUARTERS PTE. LTD.
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PROPERTY NUMBERS Total: 2

Property Type	Number
Patent Number:	7327017
Patent Number:	7205180

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NAME OF SUBMITTER:	CARMEN S. NG
SIGNATURE:	/Carmen S. Ng/
DATE SIGNED:	12/15/2017

Total Attachments: 5
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ASSIGNMENT

This agreement makes reference to the Assignment Agreement made the 8th day of May 2015 between **UTAC Thai Limited** and **UTAC Headquarters Pte. Ltd.**

UTAC Thai Limited, a corporation of **Thailand**, having its registered office at **237 Lasalle Road (Sukuhmvit 105) Bangna, Bangkok 10260, Thailand** (hereinafter "Assignor"), is the owner of US Patents as those set out and particularized in Annex A (hereinafter "Patents"), and US Patent Applications as those set out and particularized in Annex B (hereinafter "Patent Applications").

UTAC Headquarters Pte. Ltd., a corporation of **Singapore**, having its registered office at **22 Ang Mo Kio Industrial Park 2, Singapore 569506** (hereinafter "Assignee"), desires to acquire the entire rights in and to the Patents and Patent Applications.

Therefore, for good and valuable consideration, Assignor hereby sells or has sold, assigns or has assigned, and transfers or has transferred to Assignee, its successors, assigns and legal representatives, all rights, title and interests in and for the United States and all foreign countries, in and to any and all improvements which are disclosed in the Patents and Patent Applications,

and in and to said Patents and Patent Applications and all other patent applications including divisional, continuing substitute, renewal, reissue, and all other applications for Letters Patent which may have been or will be filed in the United States and all foreign countries on any of said improvements; and in and to all original and reissued patents which may have been or shall be filed in the United States and all foreign countries on said improvements.

Assignor agrees that Assignee may apply for and receive Letters Patent for said improvements in its own name, and that, when requested, at the expense of said Assignee, their successors, assigns, and legal representatives to carry out in good faith the intent and

purpose of this agreement, the undersigned will execute all divisional, continuing substitute, renewal, reissue, and all other patent applications on any and all said improvements; execute all rightful oaths, assignments, powers of attorney and other papers; communicate to said Assignee, its successors, assigns, and representatives, all facts known to the undersigned relating to said improvements and the history thereof; and generally do everything possible which said Assignee, its successors, assigns, or representatives shall consider desirable for aiding in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements and all applications for patents and all patents on said improvements, in said Assignee, its successors, assigns, and legal representatives.

Assignor covenants with said Assignee, its successors, assigns and legal representatives that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Effective Date: *8 May 2015*

(Signature)

Douglas **DEVINE**

for and on behalf of UTAC Thai Limited

Witness 1:

(Signature)

LEE *Ming Jason*

(Print name)

UTAC Thai Limited - UTAC Headquarters Pte. Ltd.
Annex A - Patents

Item #	US Patent Number	Title of Invention
1	7153724	Method of fabricating No-Lead Package for Semiconductor Die with Half Etched Leadframe
2	7049683	Semiconductor package including organometallic coating formed on surface of leadframe roughened using chemical etchant to prevent separation between leadframe and molding compound
3	7327017	Semiconductor package including leadframe roughened with chemical etchant to prevent separation between leadframe and molding compound
4	7205180	Process of fabricating semiconductor packages using leadframes roughened with chemical etchant
5	7060535	Flat no-lead semiconductor die package including stud terminals
6	6943061	Method of fabricating semiconductor chip package using screen printing epoxy on wafer
7	7572168	Method and apparatus for high speed singulation
8	7656173	Testing and burn-in using strip socket
9	7696772	Testing and burn-In using a strip socket
10	7718522	Method and apparatus for plating a semiconductor package
11	7790512	Molded-Leadframe Substrate Semiconductor Package
12	8063470	Method and Apparatus for No Lead Semiconductor Package
13	8071426	Method and Apparatus for No Lead Semiconductor Package
14	8013437	Package with Heat Transfer
15	7922877	Apparatus for plating a semiconductor package
16	8129229	Flip Chip with Collapse control using Frame design and treatment for leadframe package (Process)
17	8125077	Package with Heat Transfer on Top
18	8310060	Lead frame land grid array (product)
19	8338922	Molded Leadframe Subsstrate Semiconductor Package
20	8334764	Sensor to prevent double semiconductor units in test socket
21	8367476	Metallic solderability preservation coating on metal part of semiconductor package to prevent oxide
22	8368189	Auxiliary leadframe portion for stabilizing wire bond and avoiding bend lead during handling
23	8449356	High Pressure Cooling Nozzle for Singulating Semiconductor Package
24	8431443	Metallic solderability preservation coating on metal part of semiconductor package to prevent oxide
25	8461694	Lead Frame Ball Grid Array with traces Under Die Having Interlocking Features(Product)
26	8460970	Lead Frame Ball Grid Array with traces Under Die Having Interlocking Features(Process)
27	8487451	Lead Frame Land Grid Array with routing connector trace under unit
28	8492906	Protruded Terminal Lead Frame Land Grid Array Package
29	8569877	Metallic solderability preservation coating on metal part of semiconductor package to prevent oxide
30	8575762	Very exremely thin semiconductor package
31	8575732	Leadframe Multi Terminals IC Package
32	8652879	Protruded Terminal Lead Frame Land Grid Array Package
33	8648474	Lead frame land grid array (method)
34	8685794	Lead Frame Land Grid Array with routing connector trace under unit
35	8704381	Very Extremely Thin Semiconductor Package
36	8722461	Leadframe Multi Terminals IC Package
~~37~~	~~8816482~~	~~Leadframe Design to Improve Mold Flow of Flip Chip in Leadframe Package~~
38	8875537	Method of and system for cooling a singulation process
39	8871571	Apparatus for and methods of attaching heat slugs to package tops

17 June 2016

UTAC Thai Limited - UTAC Headquarters Pte. Ltd.
Annex B - Patent Applications

Item #	US Patent Application Number	Title of Invention
1	12383135	Lead frame land grid array (method)
2	12002186	Molded-Leadframe Substrate Semiconductor Package
3	12002054	Molded-Leadframe Substrate Semiconductor Package
4	12378119	Molded-Leadframe Substrate Semiconductor Package
5	12964698	Molded Leadframe Substrate Semiconductor Package
6	13235124	Method of and System for Cooling a Singulation Process ...(Method)
7	12231710	Flip Chip Cavity Package
8	12914694	FlipChip Cavity Package
9	12834688	Leadframe feature to minimize flip-chip semiconductor die collapse during flip-chip reflow (Post supporter version)
10	13214106	Singulation method for semiconductor package with plating on side of connectors
11	13333897	Feature of Heat Slug Attach to Semiconductor Package
12	13689531	Post-Mold concept for exposing trace semiconductor package(Product)
13	13689566	Post-Mold concept for exposing trace semiconductor package(Process)
14	13710152	Auxiliary leadframe portion for stabilizing wire bond and avoiding bend lead during handling
15	13851007	Plating Terminal and Routing Interconnection Semiconductor Device
16	13850994	Method of Manuafcturing Semiconductor Devices Including Terminals with Internal Routing Interconnections
17	13886888	Molded Leadframe Substrate Semiconductor Package
18	13851822	Protruding Terminal with Internal Routing Interconnection Semiconductor Device
19	12576846	Molded Leadframe Substrate Semiconductor Package
20	61990040	Semiconductor Package with Partial Platted on Side Terminal
21	62126262	Semiconductor Package with Partial Plated on Side Terminals