PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4729780

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	MERGER
EFFECTIVE DATE:	05/01/2012

CONVEYING PARTY DATA

Name	Execution Date
STANDARD MICROSYSTEMS CORPORATION	05/01/2012

RECEIVING PARTY DATA

Name:	MICROCHIP TECHNOLOGY INCORPORATED
Street Address:	2355 WEST CHANDLER BLVD.
City:	CHANDLER
State/Country:	ARIZONA
Postal Code:	85224-6199

PROPERTY NUMBERS Total: 25

Property Type	Number
Application Number:	13315868
Application Number:	12371375
Application Number:	12359056
Application Number:	12393996
Application Number:	13246973
Application Number:	12364144
Application Number:	12360245
Application Number:	12367242
Application Number:	12367009
Application Number:	12620656
Application Number:	12620679
Application Number:	12620726
Application Number:	12788590
Application Number:	12632495
Application Number:	12627734
Application Number:	12788896
Application Number:	12789005
Application Number:	12790161
Application Number:	12788385

Property Type	Number
Application Number:	12787730
Application Number:	12765233
Application Number:	12872834
Application Number:	12874187
Application Number:	13049932
Application Number:	13025818

CORRESPONDENCE DATA

Fax Number: (512)402-3575

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 5124023575
Email: trosson@sgbfirm.com
Correspondent Name: SLAYDEN GRUBERT BEARD PLLC
Address Line 1: 401 CONGRESS AVE
Address Line 2: SUITE 1900
Address Line 4: AUSTIN, TEXAS 78701

ATTORNEY DOCKET NUMBER:	SMSC - MTI 141-165
NAME OF SUBMITTER:	TODD ROSSON
SIGNATURE:	/TAR/
DATE SIGNED:	12/12/2017

Total Attachments: 229
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EXECUTION COPY

AGREEMENT AND PLAN OF MERGER

by and among

MICROCHIP TECHNOLOGY INCORPORATED

MICROCHIP TECHNOLOGY MANAGEMENT CO.

and

STANDARD MICROSYSTEMS CORPORATION

Dated as of May 1, 2012

ARTICLE I
DEFINITIONS & INTERPRETATIONS

ARTICLE II
THE MERGER

ARTICLE III
REPRESENTATIONS AND WARRANTIES OF THE COMPANY

[redacted]

ARTICLE IV
REPRESENTATIONS AND WARRANTIES OF PARENT AND MERGER SUB

[redacted]

[redacted]

ARTICLE IX
GENERAL PROVISIONS

[redacted]

[redacted]

AGREEMENT AND PLAN OF MERGER

This AGREEMENT AND PLAN OF MERGER (this "Agreement") is made and entered into as of May 1, 2012, by and among MICROCHIP TECHNOLOGY INCORPORATED, a Delaware corporation ("Parent"), MICROCHIP TECHNOLOGY MANAGEMENT CO., a Delaware corporation and a wholly owned subsidiary of Parent ("Merger Sub"), and STANDARD MICROSYSTEMS CORPORATION, a Delaware corporation (the "Company"). All capitalized terms used in this Agreement shall have the respective meanings ascribed thereto in Article I.

W I T N E S S E T H:

WHEREAS, the Board of Directors of the Company (the "Company Board") unanimously has (i) determined that this Agreement and the transactions contemplated hereby, including the Merger, are advisable, (ii) determined that this Agreement and the transactions contemplated hereby, including the Merger, are fair to and in the best interests of the Company and its stockholders, (iii) approved this Agreement and the transactions contemplated hereby, including the Merger, and (iv) resolved to recommend that the Company stockholders adopt this Agreement, all upon the terms and subject to the conditions set forth herein.

WHEREAS, the Boards of Directors of Parent and Merger Sub unanimously have (i) determined that this Agreement and the transactions contemplated hereby, including the Merger, are advisable, and (ii) approved this Agreement and the transactions contemplated hereby, including the Merger, all upon the terms and subject to the conditions set forth herein.

WHEREAS, concurrently with the execution and delivery of this Agreement, as a condition and inducement to the willingness of Parent and Merger Sub to enter into this Agreement, each of the directors and certain officers of the Company, in their respective capacities as stockholders of the Company, have entered into Voting Agreements with Parent substantially in the form attached hereto as Annex A (each, a "Voting Agreement" and collectively, the "Voting Agreements").

NOW, THEREFORE, in consideration of the foregoing premises and the representations, warranties, covenants and agreements set forth herein, as well as other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged and accepted, and intending to be legally bound hereby, Parent, Merger Sub and the Company hereby agree as follows:

ARTICLE I
DEFINITIONS & INTERPRETATIONS

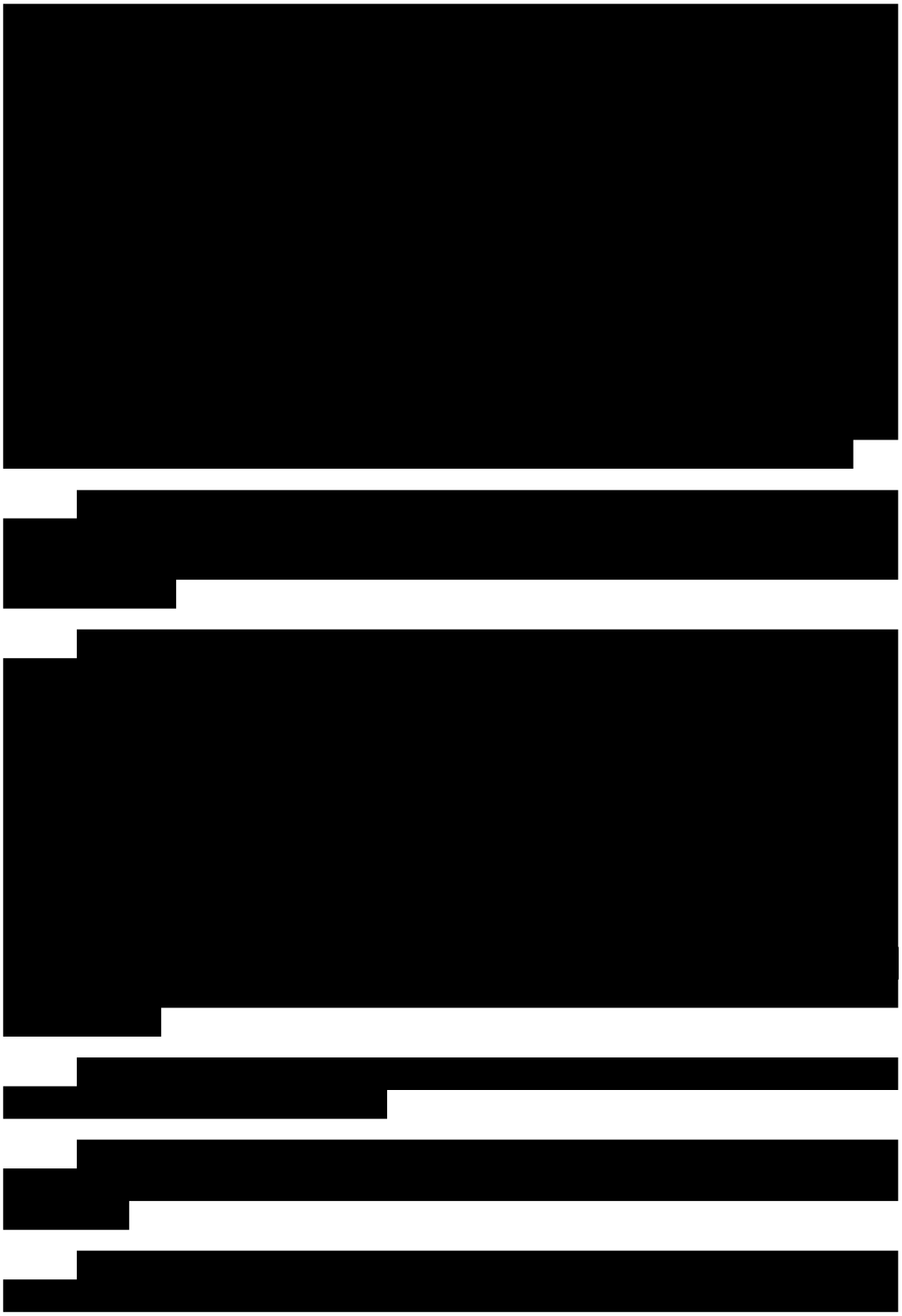
1.1 Certain Definitions. For all purposes of and under this Agreement, the following capitalized terms shall have the following respective meanings:

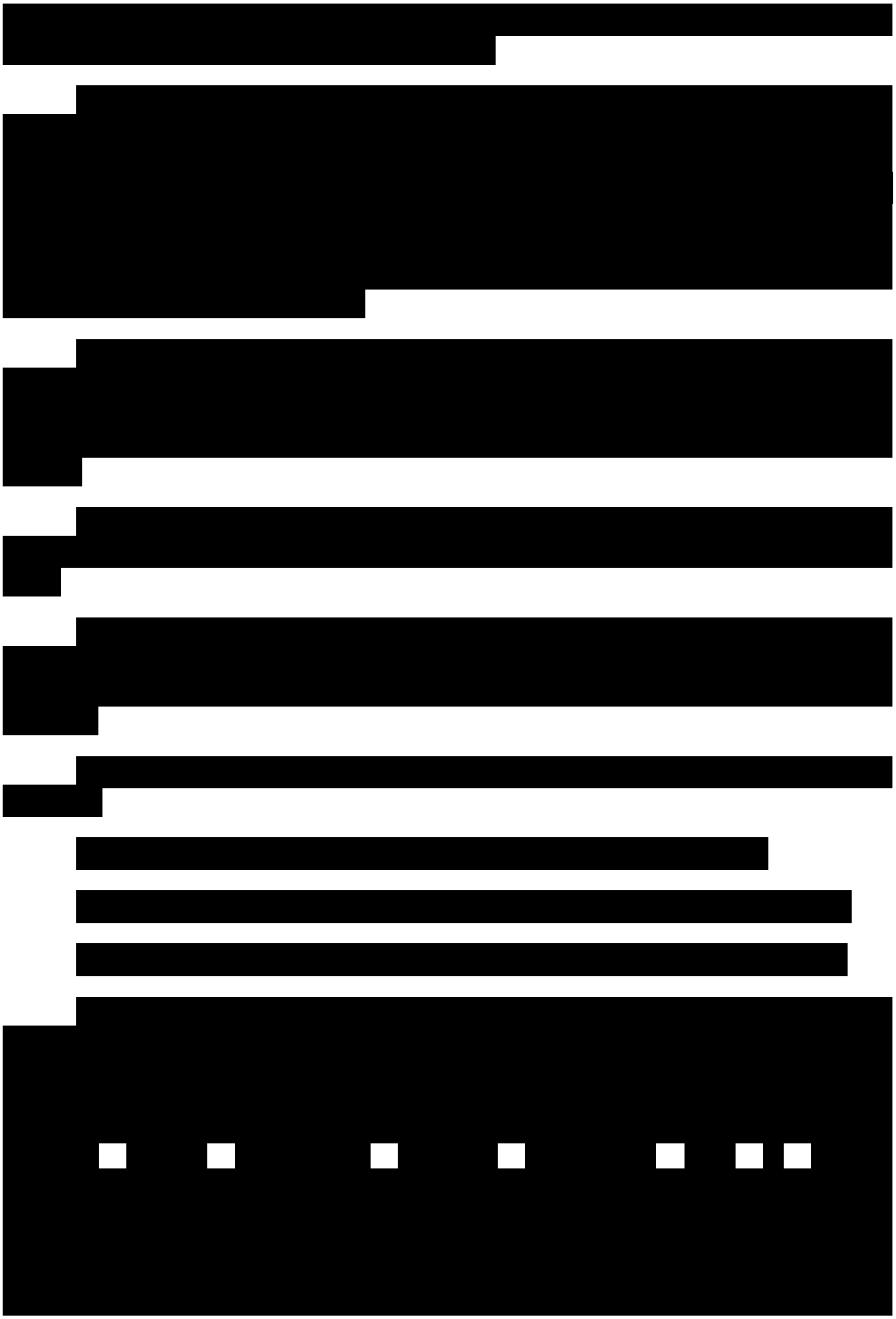
[redacted]

"Company IP" means all Intellectual Property Rights that are used by or otherwise licensed to or owned by the Company or any of its Subsidiaries.

"Company Intellectual Property Rights" means all of the Intellectual Property Rights owned by or exclusively licensed to the Company or any of its Subsidiaries.

[redacted]





"Intellectual Property Rights" means any or all of the following and all statutory and/or common law rights throughout the world in, arising out of, or associated therewith: (i) all United States and foreign patents and utility models, including utility patents and design patents, and all registrations and applications therefore (including provisional applications) and all reissues, divisions, renewals, extensions, re-examinations, provisionals, continuations and continuations in part thereof and equivalent or similar rights anywhere in the world in inventions (collectively, "Patents"); (ii) all inventions (whether or not patentable, reduced to practice or made the subject of a pending patent application), invention disclosures and improvements, all trade secrets, know-how, and confidential or proprietary information (collectively, "Trade Secrets"); (iii) all works of authorship, copyrights (registered or otherwise, including in Software), mask works, copyright and mask work registrations and applications and all other rights corresponding thereto throughout the world, and all rights therein provided by international treaties or conventions (collectively, "Copyrights"); (iv) all industrial designs and any registrations and applications therefore; (v) all trade names, trade dress, logos, or other corporate designations, trademarks and service marks, whether or not registered, including all common law rights, and trademark and service mark registrations and applications, including all marks registered in the United States Patent and Trademark Office and the Trademark Offices of other nations throughout the world, and all rights therein provided by international treaties or conventions (collectively, "Trademarks"); (vi) all rights in

databases and data collections (including knowledge management databases, customer lists and customer databases) and Software; (viii) all rights to Uniform Resource Locators, Web site addresses and domain names and applications and registrations therefore (collectively, "Domain Names"); and (ix) any similar, corresponding or equivalent rights to any of the foregoing.

[redacted]

[redacted]

"Registered IP" means all United States, international and foreign: (i) Patents; (ii) Trademark registrations and applications for registration; (iii) Copyright registrations and applications for registration; (iv) Domain Name registrations; and (v) any other Intellectual Property Rights that are the subject of an application or registration.

[redacted]

"Subsidiary" means, with respect to any Person, any entity of which securities or other ownership interests having ordinary voting power to elect a majority of the board of directors or other persons performing similar functions are at any time directly or indirectly owned by such Person.

[redacted]

[redacted]

1.2 Additional Definitions. The following capitalized terms shall have the respective meanings ascribed thereto in the respective sections of this Agreement set forth opposite each of the capitalized terms below:

Term	Section Reference
[redacted]	[redacted]

Term	Section Reference
[redacted]	[redacted]
Company IP Agreements	3.22(e)
Company Registered IP	3.22(b)
[redacted]	[redacted]

Term	Section Reference
[redacted]	[redacted]

1.3 Certain Interpretations.

(a) Unless otherwise indicated, all references herein to Sections, Articles, Annexes, Exhibits or Schedules, shall be deemed to refer to Sections, Articles, Annexes, Exhibits or Schedules of or to this Agreement, as applicable.

(b) Unless otherwise indicated, the words "include," "includes" and "including," when used herein, shall be deemed in each case to be followed by the words "without limitation."

(c) The table of contents and headings set forth in this Agreement are for convenience of reference purposes only and shall not affect or be deemed to affect in any way the meaning or interpretation of this Agreement or any term or provision hereof.

(d) Unless otherwise specifically provided, all references in this Agreement to "Dollars" or "$" means United States Dollars.

(e) As used in this Agreement, the singular or plural number shall be deemed to include the other whenever the context so requires. Article, Section, clause and Schedule references contained in this Agreement are references to Articles, Sections, clauses and Schedules in or to this Agreement, unless otherwise specified.

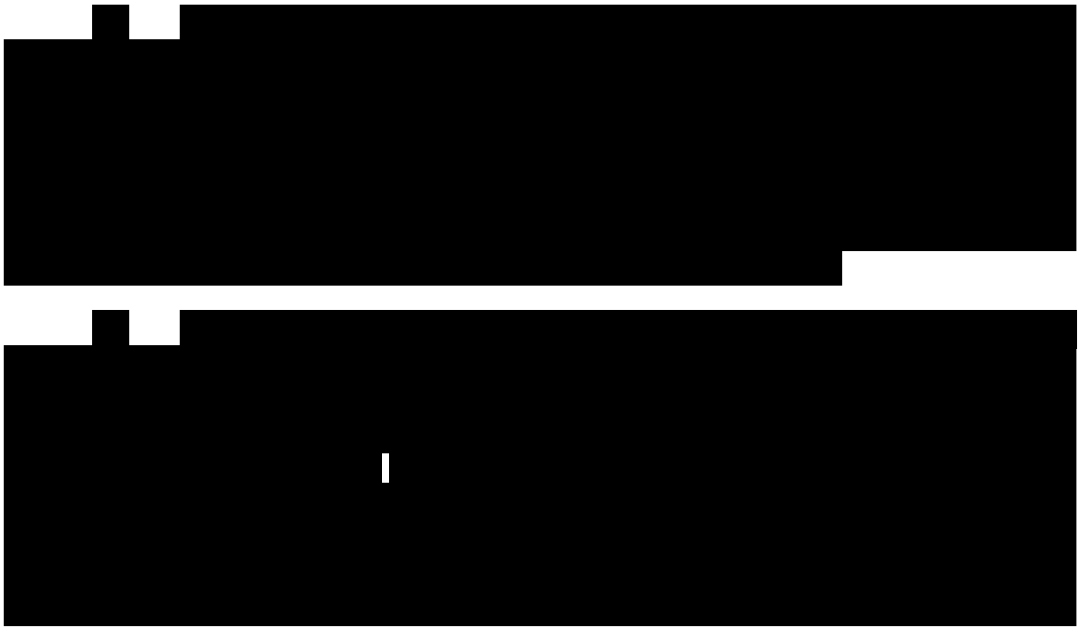
(f) As used in this Agreement, the word "extent" and the phrase "to the extent" shall mean the degree to which a subject or other thing extends, and such word or phrase shall not mean simply "if".

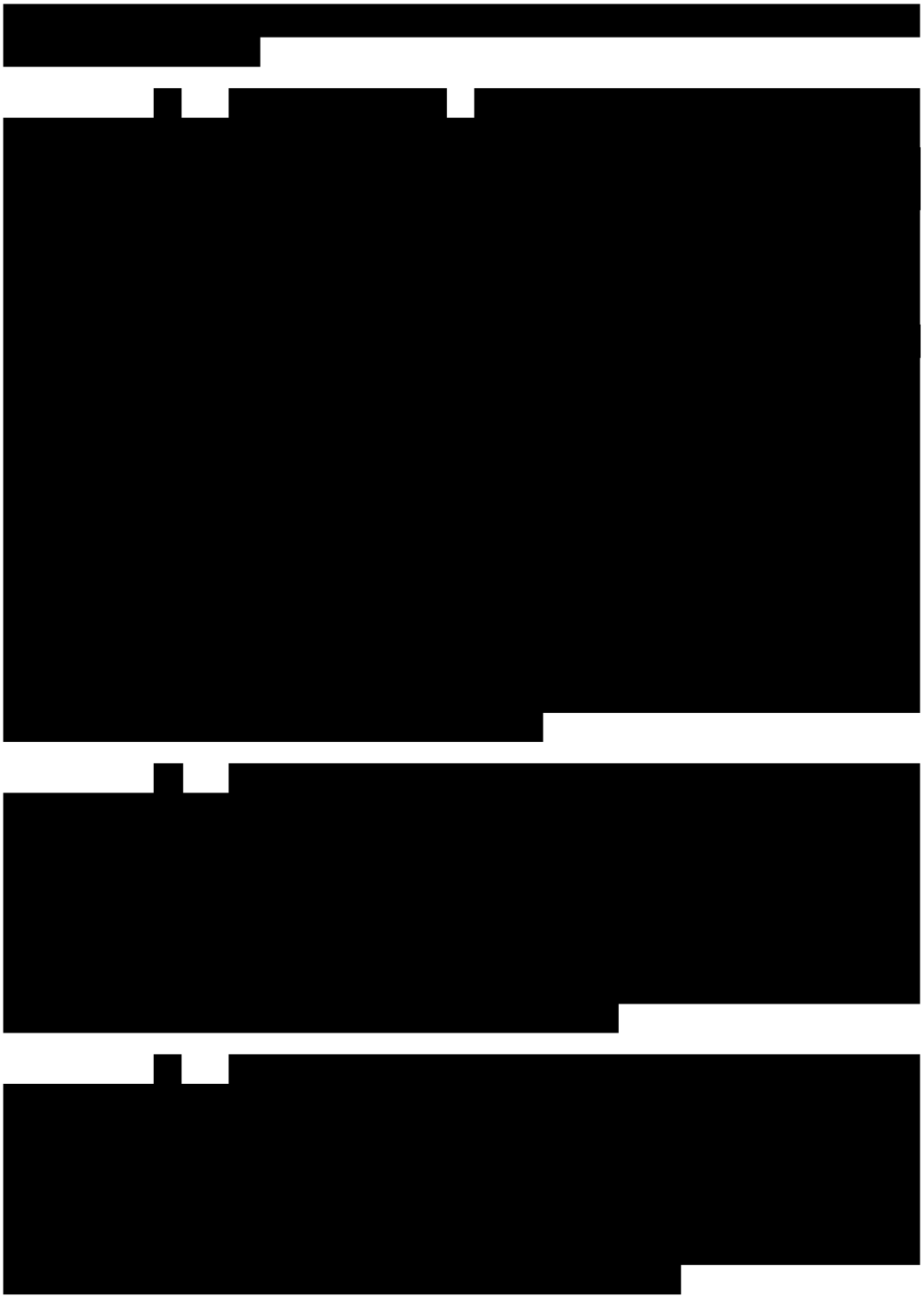
(g) Whenever any reference is made in this Agreement to the Company having "made available" any document or information, such phrase shall include having made such document or information available (i) prior to the date of this Agreement in the electronic data room utilized in connection with the transactions contemplated by this Agreement or (ii) if such document is referred to in the Index to Exhibits in the Company Form 10-K, in the Electronic Data Gathering, Analysis and Retrieval (EDGAR) database of the SEC.

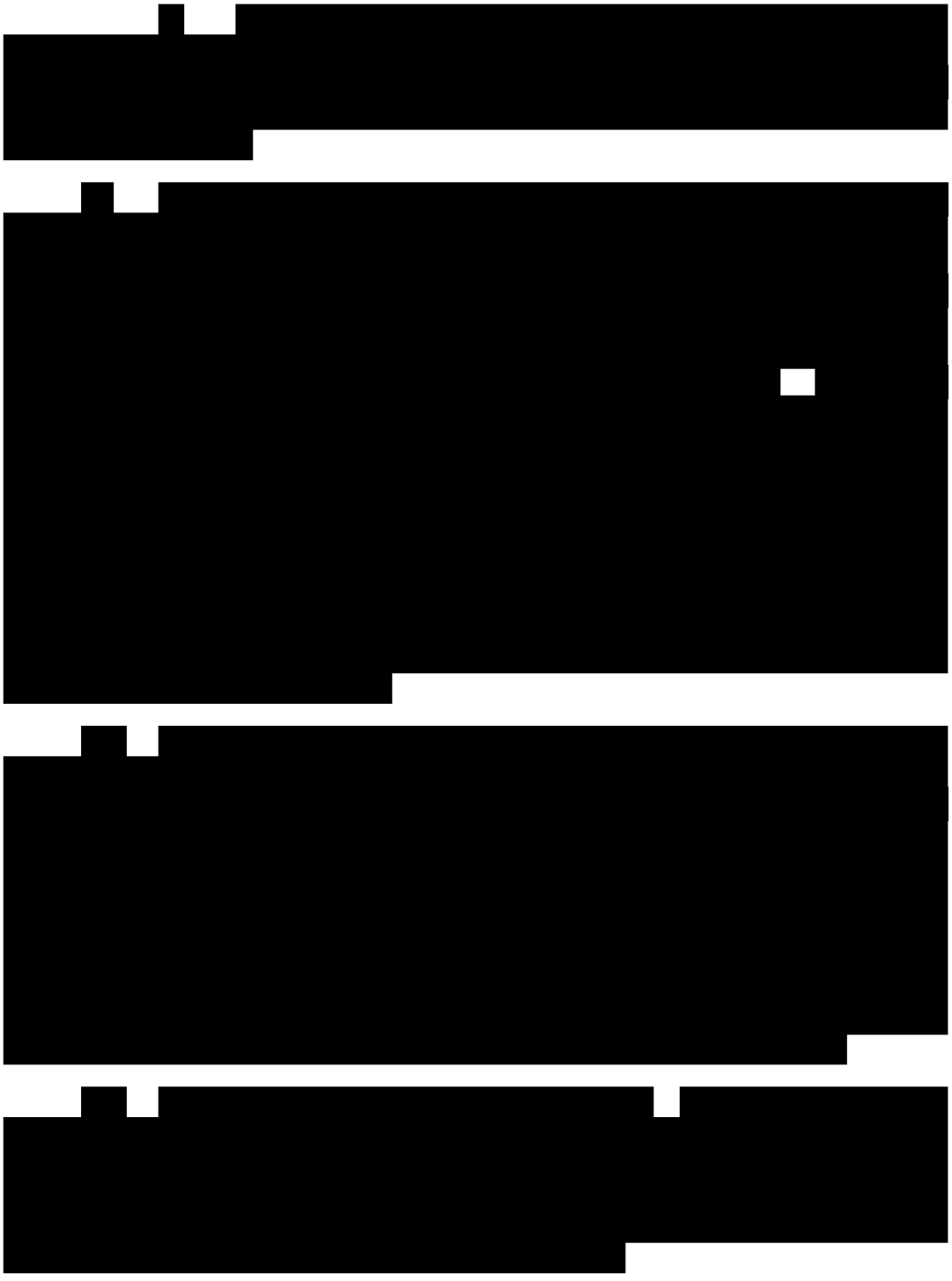
(h) The parties hereto agree that they have been represented by counsel during the negotiation and execution of this Agreement and, therefore, waive the application of any Applicable Law or rule of construction providing that ambiguities in an agreement or other document will be construed against the party drafting such agreement or document.

ARTICLE II
THE MERGER

2.1 The Merger. Upon the terms and subject to the conditions set forth in this Agreement and the applicable provisions of Delaware Law, at the Effective Time, Merger Sub shall be merged with and into the Company, the separate corporate existence of Merger Sub shall thereupon cease and the Company shall continue as the surviving corporation. The Company, as the surviving corporation of the Merger, is sometimes hereinafter referred to as the "Surviving Corporation."







ARTICLE III
REPRESENTATIONS AND WARRANTIES OF THE COMPANY

Except, with respect to any Section of this Article III, as set forth in the section of the disclosure letter delivered by the Company to Parent on the date of this Agreement (the "Company Disclosure Letter") that specifically relates to such Section or in another section of the Company Disclosure Letter to the extent it is reasonably apparent from the text of such disclosure that such disclosure is applicable to such Section, and except as disclosed in the Annual Report on Form 10-K of the Company for the fiscal year ended February 29, 2012 (the "Company Form 10-K") (other than disclosures in the "Risk Factors" or "Forward-Looking Statements" sections of such reports, other disclosures that are similarly non-specific or are predictive or forward-looking in nature and excluding any exhibits incorporated by reference in such reports), the Company hereby represents and warrants to Parent and Merger Sub as follows:

3.1 Organization and Standing. The Company is a corporation duly organized, validly existing and in good standing under Delaware Law. The Company has the requisite power and authority to carry on its business as it is presently being conducted and to own, lease or operate its respective properties and assets. The Company is duly qualified to do business and is in good standing in each jurisdiction where the character of its properties owned or leased or the nature of its activities make such qualification necessary (to the extent the "good standing" concept is applicable in the case of any jurisdiction outside the United States), except where the failure to be so qualified or in good standing has not had and would not reasonably be expected to have, individually or in the aggregate, a Company Material Adverse Effect. The Company has delivered or made available to Parent complete and correct copies of its certificate of incorporation and bylaws, as amended to date. The Company is not in violation of its certificate of incorporation or bylaws. The Company has delivered or made available to Parent complete and correct copies of the minutes (or, in the case of draft minutes, the most recent drafts thereof) of all meetings of the stockholders, the Company Board and each committee of the Company Board held since January 1, 2010 other than any such minutes relating to this Agreement or the transactions contemplated hereby or any alternatives to this Merger considered by the Company Board.

3.2 Subsidiaries.

(a) Section 3.2(a) of the Company Disclosure Letter contains a complete and accurate list of the name and jurisdiction of organization of each Subsidiary of the Company. Except for the Company's Subsidiaries, the Company does not own, directly or indirectly, any capital stock of, or other equity or voting interest in, any Person.

(b) Except as has not had and would not reasonably be expected to have, individually or in the aggregate, a Company Material Adverse Effect, each of the Company's Subsidiaries (i) is duly organized, validly existing and in good standing under the Applicable Laws of the jurisdiction of its respective organization (to the extent the "good standing" concept is applicable in the case of any jurisdiction outside the United

States), (ii) has the requisite power and authority to carry on its respective business as it is presently being conducted and to own, lease or operate its respective properties and assets, (iii) is duly qualified to do business and is in good standing in each jurisdiction where the character of its properties owned or leased or the nature of its activities make such qualification necessary (to the extent the "good standing" concept is applicable in the case of any jurisdiction outside the United States) and (iv) is in compliance with its respective certificate of incorporation, bylaws or other applicable constituent documents. The Company has delivered or made available to Parent complete and correct copies of the certificates of incorporation and bylaws or other constituent documents, as amended to date, of each of the Company's Subsidiaries.

[redacted]

Pages 22-39 intentionally omitted

3.22 Intellectual Property.

(a) Section 3.22(a) of the Company Disclosure Letter contains a complete and accurate list of all Company Products and all Domain Names under which Company operates its business.

(b) Section 3.22(b) of the Company Disclosure Letter contains a complete and accurate list of the Company Intellectual Property Rights that are Registered IP and material unregistered Trademarks ("Company Registered IP"), in each case listing, as applicable, (i) the name of the current owner, (ii) the jurisdiction where the application/registration is located, (iii) the application or registration number, (iv) the filing date, and issuance/registration/grant date, and (v) the prosecution status thereof.

(c) To the Knowledge of the Company, the Company Registered IP is valid, sustaining and enforceable.

(d) To the Knowledge of the Company, with respect to each item of Company Registered IP, all necessary registration, maintenance and renewal fees have been paid.

(e) Section 3.22(e) of the Company Disclosure Letter contains a complete and accurate list of all Contracts (i) under which the Company or any of its Subsidiaries has the right to use any material Company IP, other than Shrink-Wrap Code or (ii) under which the Company or any of its Subsidiaries licenses to others the right to use any material Company Intellectual Property Rights, other than non-disclosure agreements and non-exclusive license agreements entered into in the ordinary course of business (such

Contracts, the "Company IP Agreements"). The Company has made available to Parent complete and correct copies of each such Company IP Agreement. To the Knowledge of the Company, (x) each Company IP Agreement is valid and binding on the Company or the Subsidiary of the Company that is a party thereto and is in full force and effect, (y) neither the Company nor any of its Subsidiaries that are a party thereto, nor any other party thereto, is in breach of, or default under, any such Company IP Agreement, and (z) no event has occurred that with notice or lapse of time or both would constitute such a breach or default thereunder by the Company or any of its Subsidiaries, in each of clauses (x), (y) and (z), except as is not and would not reasonably be expected to be, individually or in the aggregate, material to the Company and its Subsidiaries, taken as a whole. To the Knowledge of the Company, there are no pending material disputes regarding the scope of such Company IP Agreements, performance under the Company IP Agreements, or with respect to payments made or received under such Company IP Agreements.

(f) To the Knowledge of the Company, (i) the Company and its Subsidiaries own or have sufficient rights to use all Intellectual Property Rights that are either used in or necessary for the conduct of the business of the Company and its Subsidiaries as currently conducted, and (ii) neither the operation of the business of the Company nor the use, provision, support, reproduction, making, distribution, marketing, sale, license or display of the Company Products by Company or its Subsidiaries infringes or misappropriates the Intellectual Property Rights or Moral Rights of any Person, in each of clauses (i) and (ii), except as is not and would not reasonably be expected to be, individually or in the aggregate, material to the Company and its Subsidiaries, taken as a whole.

(g) To the Knowledge of the Company, the Company and its Subsidiaries own all right, title and interest in the owned Company Intellectual Property Rights, free and clear of all Liens other than (i) obligations arising under the terms of any of the Company IP Agreements listed on Section 3.22(e) of the Company Disclosure Letter (or other Contracts that need not be listed in Section 3.22(e)) and (ii) Permitted Liens. To the Knowledge of the Company, the Company and its Subsidiaries have the exclusive right to bring actions against any person that is infringing any Company Intellectual Property Rights and to retain for themselves any damages recovered in any such action. To the Knowledge of the Company, no Person other than the Company and its Subsidiaries has ownership rights to any Company Intellectual Property Rights.

(h) The Company and each of its Subsidiaries have taken commercially reasonable steps to protect the confidentiality of the Trade Secrets that comprise any part of the Company Intellectual Property Rights, and to the Knowledge of the Company, there is no unauthorized use, disclosure or misappropriation of any such Trade Secrets by any Person. To the Knowledge of the Company, all use and disclosure of Trade Secrets owned by another Person by the Company or any of its Subsidiaries have been pursuant to the terms of a written agreement with such Person or such use and disclosure by the Company or any of its Subsidiaries was otherwise lawful, except as is not and would not reasonably be expected to be, individually or in the aggregate, material to the Company and its Subsidiaries, taken as a whole. Without limiting the foregoing, the Company and its

Subsidiaries have a policy requiring employees, consultants and contractors to execute a confidentiality and assignment agreement which (i) assigns to the Company or one of its Subsidiaries all right, title and interest in any Intellectual Property Rights created by such persons within the scope of their involvement with the Company or applicable Subsidiary and (ii) provides reasonable protection for Trade Secrets of the Company and its Subsidiaries. To the Knowledge of the Company, to the extent permissible under Applicable Law, all current or former employees, consultants and contractors of the Company or any Subsidiary that have created any Company Intellectual Property Rights have executed such agreements, and no party to any such agreement is in breach thereof.

(i) To the Knowledge of the Company, no Person is infringing upon or otherwise violating any Company Intellectual Property Rights, and neither the Company nor any of its Subsidiaries have asserted or threatened any claim against any Person alleging the same that remains unresolved, except as is not and would not reasonably be expected to be, individually or in the aggregate, material to the Company and its Subsidiaries, taken as a whole.

(j) There is no unresolved Legal Proceeding brought by a third party that has been served upon, filed or, to the Knowledge of the Company, threatened with respect to (i) any alleged infringement or other violation by the Company or any of its Subsidiaries or any of its or their current products or services or other operation of the Company's or any of its Subsidiaries' business of the Intellectual Property Rights of such third party or (ii) any challenge to the validity or enforceability of, or contesting the Company's or any of its Subsidiaries' rights with respect to, any Company Intellectual Property Rights except, in each of clauses (i) and (ii), as is not and would not reasonably be expected to be, individually or in the aggregate, material to the Company and its Subsidiaries, taken as a whole. The Company and its Subsidiaries are not subject to any Order of any Governmental Entity that materially restricts or impairs the use, transfer or licensing of any Company Intellectual Property Rights.

(k) To the Knowledge of the Company, the execution and delivery of this Agreement and the consummation of the transactions contemplated hereby (including the Merger) will not result in any of the following events that, but for the consummation of the transactions contemplated hereby, would not have occurred: (i) the Company or its Subsidiaries granting to any third party any rights or licenses to any Company Intellectual Property Rights, except to the extent currently licensed, (ii) the vesting of any right of termination or cancellation of the counterparty under any Company IP Agreement, (iii) any payment of fees, penalties or royalties under any Company IP Agreement (other than user, seat-based or similar fees), (iv) a change in the scope of any Intellectual Property Rights granted to, or by, the Company or its Subsidiaries, (v) the imposition of any Lien on any owned Company Intellectual Property Rights (other than Permitted Liens), or (vi) after the Merger, Parent or any of its Subsidiaries or Affiliates being required to grant any third party any rights or licenses to any of Parent's or any of its Subsidiaries' or Affiliates' Intellectual Property Rights (except with respect to the Company Intellectual Property Rights), in each of clauses (i) through (vi), except as is not and would not reasonably be

expected to be, individually or in the aggregate, material to the Company and its Subsidiaries, taken as a whole.

(l) Except as set forth in Section 3.22(l) of the Company Disclosure Letter, no Software that constitutes Public Software was or is contained or included in, incorporated into, or integrated with any Company Product. Section 3.22(l) of the Company Disclosure Letter sets forth a list of all such Public Software, including: (i) the name of the Public Software; (ii) the website at which the license terms are available; (iii) the applicable Company Product referred to in the first sentence of this Section 3.22(l); and (iv) whether or not the Public Software has been modified or distributed.

(m) The Company and its Subsidiaries are in full compliance with all Public Software license agreements to which the Company or a Subsidiary, as applicable, is a party, except as is not and would not reasonably be expected to be, individually or in the aggregate, material to the Company and its Subsidiaries, taken as a whole.

(n) To the Knowledge of the Company, neither the Company nor any of its Subsidiaries have published or disclosed any Source Code owned by the Company or its Subsidiaries, except to their employees, customers or advisers pursuant to non-disclosure agreements, commercial agreements or license agreements subject to confidentiality obligations, nor has any other Person done so, except as authorized by the Company under a non-disclosure agreement, commercial agreement or license agreement subject to confidentiality obligations, in each case, except as is not and would not reasonably be expected to be, individually or in the aggregate, material to the Company and its Subsidiaries, taken as a whole. The consummation of the transactions contemplated hereby (including the Merger) will not constitute a condition sufficient to entitle the beneficiary under any Source Code escrow arrangement under which the Company or any of its Subsidiaries have deposited any material Source Code for any Company Product to require release of such Source Code.

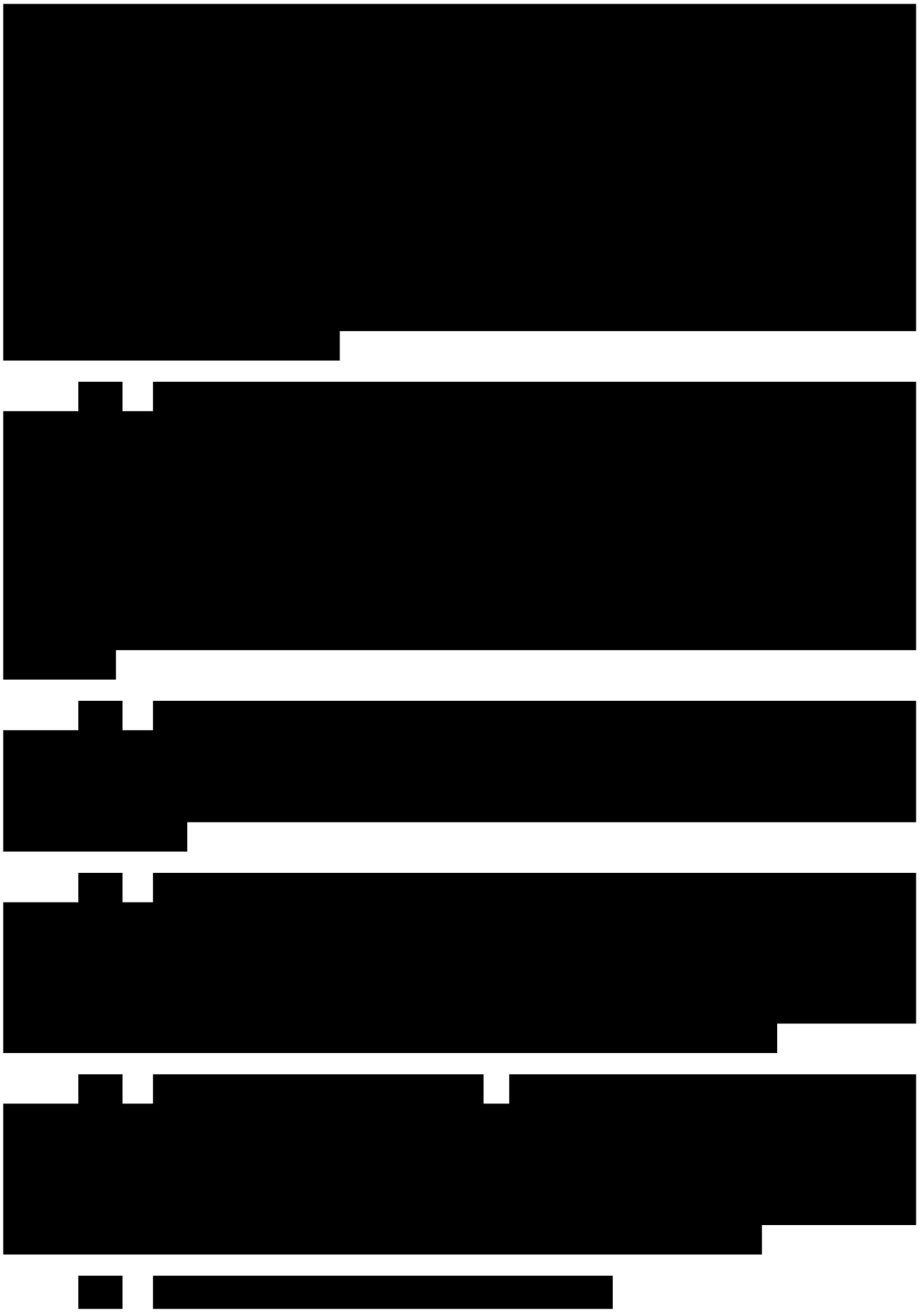
(o) To the Knowledge of the Company, all personally identifiable information which has been collected, stored, maintained or otherwise used by the Company and its Subsidiaries has been collected, stored, maintained and used in accordance with all Applicable Laws, Contracts, and Company policies and industry standards, except as is not and would not reasonably be expected to be, individually or in the aggregate, material to the Company and its Subsidiaries, taken as a whole. To the Knowledge of the Company, neither the Company nor its Subsidiaries has received a notice of noncompliance with Applicable Laws, Contracts or Company policies related to personally identifiable information.

(p) To the Knowledge of the Company, there are no material defects or errors in the Company Products or any "back door," "time bomb," "Trojan horse," "worm," "drop dead device," "virus" or other software routines or hardware components that permit unauthorized access or the unauthorized disruption, impairment, disablement or erasure of such Company Product or data or other software of users of the Company Products.

(q) The Company and its Subsidiaries have taken reasonable steps and implemented reasonable procedures to prevent viruses and other disabling codes from entering Company Products and to otherwise safeguard the information technology systems, and personally identifiable information contained therein, of the Company and its Subsidiaries. To the Knowledge of the Company, there have been no material unauthorized intrusions or breaches of the security of information technology systems of the Company and its Subsidiaries. The Company and its Subsidiaries have reasonable disaster recovery plans procedures and facilities for the business.

(r) Section 3.22(r) of the Company Disclosure Letter sets forth a true and complete list of all industry standards bodies or similar organizations in which the Company and/or any of its Subsidiaries is a member. To the Knowledge of the Company, there is no obligation to license any of the Company Intellectual Property Rights to any third party as a result of participation or membership in any standards body or similar organization. To the Knowledge of the Company, the Company and its Subsidiaries are in material compliance with their current membership in such organizations.

(s) To the Knowledge of the Company, no rights have been granted to any Governmental Entity with respect to any Company Product other than substantially the same standard commercial rights as are granted by the Company to commercial end users of the Company Products in the ordinary course of business consistent with past practices.



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[redacted]

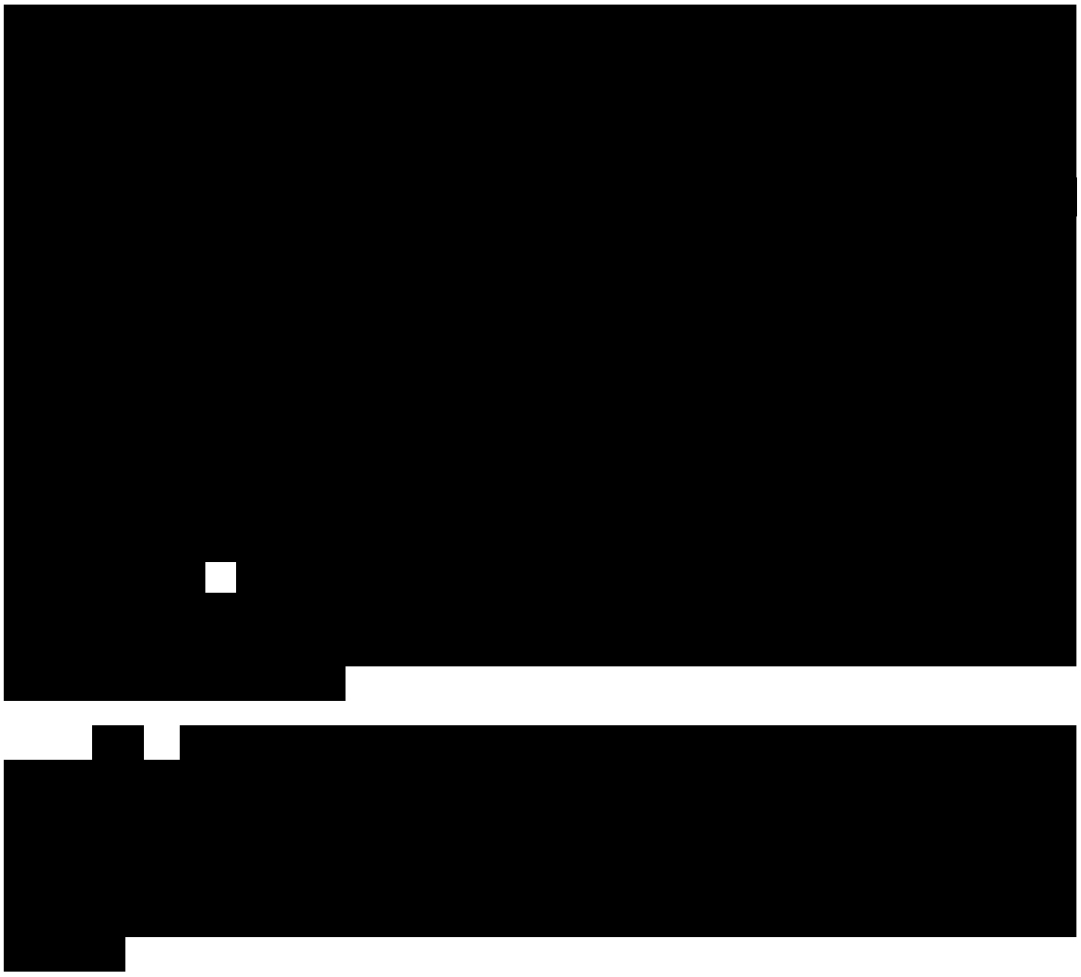
ARTICLE IV
REPRESENTATIONS AND WARRANTIES OF PARENT AND MERGER SUB

Parent and Merger Sub hereby represent and warrant to the Company as follows:

4.1 Organization and Standing. Each of Parent and Merger Sub is duly organized, validly existing and in good standing under the laws of the State of Delaware and has the requisite corporate power and authority to conduct its business as it is presently being conducted and to own, lease or operate its respective properties and assets. Each of Parent and Merger Sub is duly qualified to do business and is in good standing in each jurisdiction where the character of its properties owned or leased or the nature of its activities make such qualification necessary, except where the failure to be so qualified or in good standing has not had and would not reasonably be expected to have, individually or in the aggregate, a Parent Material Adverse Effect.

[redacted]

Pages 47-79 intentionally omitted



9.12 Counterparts. This Agreement may be executed in one or more counterparts, all of which shall be considered one and the same agreement and shall become effective when one or more counterparts have been signed by each of the parties and delivered to the other party, it being understood that all parties need not sign the same counterpart.

IN WITNESS WHEREOF, the undersigned have caused this Agreement to be executed by their respective duly authorized officers to be effective as of the date first above written.

MICROCHIP TECHNOLOGY INCORPORATED

By: Steve Sanghi
Name: Steve Sanghi
Title: Chairman, President and Chief Executive Officer

MICROCHIP TECHNOLOGY MANAGEMENT CO.

By: Steve Sanghi
Name: Steve Sanghi
Title: Director and President

STANDARD MICROSYSTEMS CORPORATION

By: Christine King
Name: Christine King
Title: President and Chief Executive Officer

[Signature Page to Merger Agreement]

COMPANY DISCLOSURE LETTER

This disclosure letter (this "Company Disclosure Letter") is being delivered by Standard Microsystems Corporation, a Delaware corporation (the "Company"), to Microchip Technology Incorporated, a Delaware corporation ("Parent"), in connection with the execution and delivery of the Agreement and Plan of Merger dated as of May 1, 2012 (the "Agreement") by and among Parent, a Delaware corporation and a wholly-owned subsidiary of Parent ("Merger Sub") and the Company. The information set forth in this Company Disclosure Letter, which relates to the representations, warranties, covenants and agreements of the Company, is subject to the following qualifications:

1. Inclusion of any item in this Company Disclosure Letter (a) does not represent an admission or determination by the Company that such item is material or would constitute or would be reasonably likely to have a Material Adverse Effect or is required to be disclosed in order for the representations and warranties of the Company to be true and correct, nor shall it be deemed to establish a standard for materiality or a Material Adverse Effect, (b) does not represent an admission or determination by the Company that such item did not arise in the ordinary course of business or in a manner consistent with past practice and (c) shall not constitute, or be deemed to be, an admission or indication by any party to any third party of any matter whatsoever (including any breach or violation of any Contract, Applicable Law or Order or any infringement of any Intellectual Property Right). In cases where a representation or warranty is qualified by a reference to materiality or a Material Adverse Effect, the disclosure of any matter in this Company Disclosure Letter shall not imply that any other undisclosed matter that has a greater value or could otherwise be deemed to be more significant (i) is or is reasonably likely to be material or (ii) has had or would be reasonably likely to have a Material Adverse Effect. Except as otherwise expressly contemplated herein, this Company Disclosure Letter and the information and disclosures contained herein are intended only to qualify and limit the representations, warranties, covenants and agreements of the Company contained in the Agreement and shall not be deemed to expand in any way the scope or effect of any such representations, warranties, covenants and agreements. The items in this Company Disclosure Letter include brief descriptions or summaries of certain agreements, instruments and other documents, which descriptions do not purport to be comprehensive, and are qualified in their entirety by reference to the text of the documents described.

2. The disclosure set forth in one Section or subsection of this Company Disclosure Letter shall be deemed to apply to and qualify the Section or subsection of the Agreement to which it corresponds in number and each other Section or subsection of the Agreement to the extent that it is reasonably apparent from the text of the disclosure that such disclosure is relevant to such other Section or subsection.

3. Headings shall not have the effect of amending or changing the express description of the items in this Company Disclosure Letter in the corresponding Sections of the Agreement.

4. The information contained in this Company Disclosure Letter is in all respects subject to the Confidentiality Agreement.

5. The rules of interpretation and construction specified in Section 1.3 of the Agreement shall also apply to this Company Disclosure Letter.

Section 3.2

Subsidiaries

(a)

	Name	Jurisdiction of Organization
1.	Standard Microsystems Corporation (Asia)	United States (with branches in Taiwan, Korea, Hong Kong, Beijing, Shanghai, and Shenzhen)
2.	Standard Microsystems KK	Japan
3.	SMSC Analog Technology Center, Inc.	United States
4.	SMSC North America, Inc.	United States
5.	SMSC Europe GmbH	Germany
6.	SMSC Storage, Inc.	United States
7.	Standard Microsystems India Private Limited	India
8.	Bridgeco Technologies India Private Limited	India
9.	BridgeCo, LLC	United States
10.	Standard Microsystems Corporation (Asia) S.C.S.	Luxembourg
11.	SMSC Standard Microsystems (Canada) Corporation	Canada
12.	SMSC Holdings S.à r.l.	Luxembourg
13.	SMSC Trading	Luxembourg (with a branch in Hong Kong)
14.	SMSC Sweden AB	Sweden
15.	K2L GmbH	Germany
16.	SMSC Technology (Shenzhen) Co. Ltd.	China
17.	Wireless Audio IP B.V.	The Netherlands
18.	Wireless Sound Solutions (WSS) B.V.	The Netherlands
19.	Wireless Sound Solutions Pte. Ltd.	Singapore

Section 3.22(b)

Company Registered IP

Patents and Trademarks

See attached Annex 3.22(b) and Supplement to Annex 3.22(b).

Copyrights[3]

1. TX 6-375-230 "MOST NetServices Version 0.40"
2. TXu1-27-175 "MOST NetServices Version 01.10.02"
3. TX 6-375-229 "MOST NetServices Version 01.10.02 (Green Hills)"

[redacted]

[3] Exclusively licensed from the authors (Germany).

Annex 3.22(b) Patents and Trademarks

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	AT	AT 98 951 043.3	1998-10-13	98 951 043.3	--		Phasenregelkreis und integrierte Schaltung dafür	SMSC Europe GmbH
G	DE	DE 98 951 043.3	1998-10-13	98 951 043.3	--		Phasenregelkreis und integrierte Schaltung dafür	SMSC Europe GmbH
G	EP	EP 98 951 043.3	1998-10-13	98 951 043.3	--		Phase-Looked loop and Integrated circuit therefore	SMSC Europe GmbH
G	EP	EP 1 333 580 B1	1998-10-13	03 007 754.9-2206	2006-04-26	1 333 580 B1	Phased-Locked Loop and Integrated Circuit Therefore	SMSC Europe GmbH
G	DE	DE 03 007 754.9	1998-10-13	03 007 754.9	--		Vorrichtung mit einer Phasenregelschleife	SMSC Europe GmbH
G	FR	FR 03 007 754.9-2206	1998-10-13	03 007 754.9-2206	--		Appareil comportant une boucle à verrouillage de phase	SMSC Europe GmbH
G	GB	GB 03 007 754.9-2206	1998-10-13	03 007 754.9-2206	--		Apparatus Comprising a Phase-locked Loop	SMSC Europe GmbH
G	FI	FI 1 012 979 B1	1998-10-13	98 951 043.3	2003-07-30	1 012 979 B1	Phase-Looked loop and Integrated circuit therefore	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	FR	FR 1 012 979 B1	1998-10-13	98 951 043.3	2003-07-30	1 012 979 B1	BOUCLE A PHASE ASSERVIE ET CIRCUIT INTEGRE ASSOCIE	SMSC Europe GmbH
G	GB	GB 1 012 979 B1	1998-10-13	98 951 043.3	2003-07-30	1 012 979 B1	Phase-Looked loop and Integrated circuit therefore	SMSC Europe GmbH
G	IT	IT 1 012 979 B1	1998-10-13	98 951 043.3	2003-07-30	1 012 979 B1	Phase-Looked loop and Integrated circuit therefore	SMSC Europe GmbH
G	NL	NL 1 012 979 B1	1998-10-13	98 951 043.3	2003-07-30	1 012 979 B1	Phase-Looked loop and Integrated circuit therefore	SMSC Europe GmbH
G	SE	SE 1 012 979 B1	1998-10-13	98 951 043.3	2003-07-30	1 012 979 B1	Phase-Looked loop and Integrated circuit therefore	SMSC Europe GmbH
G	AT	AT 265 060 T1	1999-02-12	99 907 000.6	--		Einrichtung und Verfahren zum Takten von digitalen und analogen Schaltungen auf einem gemeinsamen Substrat zur Geräuschverminderung	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	DE	DE 99 907 000.6	1999-02-12	99 907 000.6	--		Einrichtung und Verfahren zum Takten von digitalen und analogen Schaltungen auf einem gemeinsamen Substrat zur Geräuschverminderung	SMSC Europe GmbH
G	EP	EP 99 907 000.6-2212	1999-02-12	99 907 000.6-2212	--		Apparatus and Method for Clocking Digital and Analog Circuits on a Common Substrate to Reduce Noise	SMSC Europe GmbH
G	EP	EP 1 414 156 B1	1999-02-12	03 028 094.5-2206	2006-08-30	1 414 156 B1	APPARATUS FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE AND METHOD	SMSC Europe GmbH
G	AT	AT 03 028 094.5	1999-02-12	03 028 094.5	--		APPARATUS FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE AND METHOD	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	DE	DE 03 028 094.5	1999-02-12	03 028 094.5	--		VORRICHTUNG ZUM TAKTEN VON DIGITALEN UND ANALOGEN SCHALTUNGEN AUF EINEM GEMEINSAMEN SUBSTRAT UND VERFAHREN DAZU	SMSC Europe GmbH
G	FI	FI 03 028 094.5	1997-02-12	03 028 094.5	--		APPARATUS FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE AND METHOD	SMSC Europe GmbH
G	FR	FR 03 028 094.5	1999-02-12	03 028 094.5	--		APPARATUS FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE AND METHOD	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	GB	GB 03 028 094.5	1999-02-12	03 028 094.5	--		APPARATUS FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE AND METHOD	SMSC Europe GmbH
G	IT	IT 03 028 094.5	1999-02-12	03 028 094.5	--		APPARATUS FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE AND METHOD	SMSC Europe GmbH
G	NL	NL 03 028 094.5	1999-02-12	03 028 094.5	--		APPARATUS FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE AND METHOD	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	SE	SE 03 028 094.5	1999-02-12	03 028 094.5	--		APPARATUS FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE AND METHOD	SMSC Europe GmbH
G	FI	FI 1 057 261 B1	1999-02-12	99 907 000.6	2004-04-21	1 057 261 B1	APPARATUS AND METHOD FOR THE CLOCKING OF DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE TO REDUCE NOISE	SMSC Europe GmbH
G	FR	FR 1 057 261 B1	1999-02-12	99 907 000.6	2004-04-21	1 057 261 B1	APPAREIL ET PROCEDE DE SXYNCHRONISATION DE CIRCUITS NUMERIQUES ET ANALOGIQUES D"UN SUBSTRAT COMMUN POUR AMELIORER LES OPERATIONS NUMERIQUES ET REDUIRE L"ERREUR SUR ...	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	GB	GB 1 057 261 B1	1999-02-12	99 907 000.6	2004-04-21	1 057 261 B1	APPARATUS AND METHOD FOR THE CLOCKING OF DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE TO REDUCE NOISE	SMSC Europe GmbH
G	IT	IT 1 057 261 B1	1999-02-12	99 907 000.6	2004-04-21	1 057 261 B1	APPARATUS AND METHOD FOR THE CLOCKING OF DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE TO REDUCE NOISE	SMSC Europe GmbH
G	NL	NL 1 057 261 B1	1999-02-12	99 907 000.6	2004-04-21	1 057 261 B1	APPARATUS AND METHOD FOR THE CLOCKING OF DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE TO REDUCE NOISE	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	SE	SE 1 057 261	1999-02-12	99 907 000.6-2212	2004-04-21	1 057 261	APPARATUS AND METHOD FOR THE CLOCKING OF DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE TO REDUCE NOISE	SMSC Europe GmbH
G	AT	AT 98 953 611.5	1998-10-16	98 953 611.5	--		Phasenregelkreis und Verfahren zum automatischen Einrasten auf einer veränderlichen Eingangsfrequenz	SMSC Europe GmbH
G	DE	DE 98 953 611.5	1998-10-16	98 953 611.5	--		Phasenregelkreis und Verfahren zum automatischen Einrasten auf einer veränderlichen Eingangsfrequenz	SMSC Europe GmbH
G	EP	EP 1 023 776 B1	1998-10-16	98 953 611.5	2003-02-12	1 023 776 B1	Phasenregelkreis und Verfahren zum automatischen Einrasten auf einer veränderlichen Eingangsfrequenz	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	FI	FI 98 953 611.5	1998-10-16	98 953 611.5	--		Phasenregelkreis und Verfahren zum automatischen Einrasten auf einer veränderlichen Eingangsfrequenz	SMSC Europe GmbH
G	FR	FR 98 953 611.5	1998-10-16	98 953 611.5	--		Phasenregelkreis und Verfahren zum automatischen Einrasten auf einer veränderlichen Eingangsfrequenz	SMSC Europe GmbH
G	GB	GB 98 953 611.5	1998-10-16	98 953 611.5	--		Phasenregelkreis und Verfahren zum automatischen Einrasten auf einer veränderlichen Eingangsfrequenz	SMSC Europe GmbH
G	IT	IT 98 953 611.5	1998-10-16	98 953 611.5	--		Phasenregelkreis und Verfahren zum automatischen Einrasten auf einer veränderlichen Eingangsfrequenz	SMSC Europe GmbH
G	NL	NL 98 953 611.5	1998-10-16	98 953 611.5	--		Phasenregelkreis und Verfahren zum automatischen Einrasten auf einer veränderlichen Eingangsfrequenz	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	SE	SE 98 953 611.5	1998-10-16	98 953 611.5	--		Phasenregelkreis und Verfahren zum automatischen Einrasten auf einer veränderlichen Eingangsfrequenz	SMSC Europe GmbH
G	DE	DE 00 911 928.0	2000-02-22	00 911 928.0	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	EP	EP 00 911 928.0-1246	2000-02-22	00 911 928.0-1246	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
F	EP	EP 06 001 159.0-1246	2000-02-22	06 001 159.0-1246	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	DE	DE 06 001 159.0-1246	2000-02-22	06 001 159.0-1246	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	FI	FI 06 001 159.0-1246	2000-02-22	06 001 159.0-1246	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	FR	FR 06 001 159.0-1246	2000-02-22	06 001 159.0-1246	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	GB	GB 06 001 159.0-1246	2000-02-22	06 001 159.0-1246	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	IT	IT 06 001 159.0-1246	2000-02-22	06 001 159.0-1246	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	NL	NL 06 001 159.0-1246	2000-02-22	06 001 159.0-1246	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	SE	SE 06 001 159.0-1246	2000-02-22	06 001 159.0-1246	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	FR	FR 00 911 928.0	2000-02-22	00 911 928.0	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	GB	GB 00 911 928.0	2000-02-22	00 911 928.0	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	IT	IT 00 911 928.0	2000-02-22	00 911 928.0	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	SE	SE 00 911 928.0	2000-02-22	00 911 928.0	--		COMMUNICATION SYSTEM TRANSCEIVERS WITH DATA BYPASS AND POWER SAVING FEATURES	SMSC Europe GmbH
G	US	US 7 327 742 B2	2002-06-26	10/180,696	2008-02-05	7 327 742 B2	Communication System and Method for sending isochronous streaming data within a frame segment using a signaling byte	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	US	US 7,164,691 B2	2002-06-26	10/180,741	2007-01-16	7,164,691 B2	Communication System and Method for sending isochronous streaming data across a synchronous network within a frame segment using a coding violation to signify invalid ...	SMSC Europe GmbH
G	US	US 6,874,048 B2	2002-05-29	10/157,673	2005-03-29	6,874,048 B2	Communication system and methodology for sending a designator for at least one of a set of time-Division multiplexed channels forwarded across a locally synchronized bus	SMSC Europe GmbH
G	US	US 6,922,747 B2	2002-05-29	10/157,097	2005-07-26	6,922,747 B2	Communication system and methodology for addressing and sending data of dissmilar type and size across channels formed within a locally synchronized bus	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	US	US 7 283 564 B2	2002-06-26	10/180,729	2007-10-16	7 283 564 B2	Communictaion system and method for sending asynchronous data and/or isochronous streaming data across a synchronous network within a frame segment using a coding...	SMSC Europe GmbH
G	US	US 7,158,596 B2	2002-08-14	10/218,351	2007-01-02	7,158,596 B2	Communictaion system and method for sending and receiving data at a higher or lower sample rate than a network frame rate using a phase locked loop	SMSC Europe GmbH
F	EP	EP 03799288.0-1237	2003-09-24	03799288.0-1237	--		System and method for transferring data among transceivers substantially void of data dependent jitter	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	EP	EP 01 997 044.1-2415	2001-11-05	01 997 044.1-2415	--		AN ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS	SMSC Europe GmbH
G	DE	DE 01 997 044.1-2415	2001-11-05	01 997 044.1-2415	--		AN ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	FI	FI 01 997 044.1-2415	2001-11-05	01 997 044.1-2415	--		AN ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS	SMSC Europe GmbH
G	FR	FR 01 997 044.1-2415	2001-11-05	01 997 044.1-2415	--		AN ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	GB	GB 01 997 044.1-2415	2001-11-05	01 997 044.1-2415	--		AN ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS	SMSC Europe GmbH
G	IT	IT 01 997 044.1-2415	2001-11-05	01 997 044.1-2415	--		AN ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	NL	NL 01 997 044.1-2415	2001-11-05	01 997 044.1-2415	--		AN ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS	SMSC Europe GmbH
G	SE	SE 01 997 044.1-2415	2001-11-05	01 997 044.1-2415	--		AN ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	WO	WO 02/062028 A2	2001-11-05	01/46920	--		AN ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS	SMSC Europe GmbH
G	DE	DE 03 729 146.5	2003-05-28	03 729 146.5	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	EP	EP 03 729 146.5-2416	2003-05-28	03 729 146.5-2416	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH
F	EP	EP 06 000 673.1-2416	2003-05-28	06 000 673.1-2416	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH
G	DE	DE 06 000 673.1-2416	2003-05-28	06 000 673.1-2416	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	FR	FR 06 000 673.1-2416	2003-05-28	06 000 673.1-2416	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH
F	GB	GB	2003-05-28		--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH
G	SE	SE 06 000 673.1-2416	2003-05-28	06 000 673.1-2416	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	FR	FR 03 729 146.5	2003-05-28	03 729 146.5	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH
G	GB	GB 03 729 146.5	2003-05-28	03 729 146.5	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH
G	IT	IT 03 729 146.5	2003-05-28	03 729 146.5	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	SE	SE 03 729 146.5	2003-05-28	03 729 146.5	--		COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCRONIZED BUS	SMSC Europe GmbH
G	EP	EP 03 736 882.6-2416	2003-06-04	03 736 882.6-2416	--		COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY ...	SMSC Europe GmbH
G	AT	AT 1 525 691 A1	2003-06-04	03 736 882.6	--		Kommunikationssystem zur Sendung von ungleichartigen Daten über ein synchrones Netzwerk	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	DE	DE 03 736 882.6	2003-06-04	03 736 882.6	--		Kommunikationssystem zur Sendung von ungleichartigen Daten über ein synchrones Netzwerk	SMSC Europe GmbH
G	FI	FI 03 736 882.6	2003-06-04	03 736 882.6	--		Communication System for Sending Dissimilar Types of Data across a Synchronous Network	SMSC Europe GmbH
G	FR	FR 03 736 882.6	2003-06-04	03 736 882.6	--		Systeme de Communication pour Envoyer Differents Types de Donnees a Travers un Reseau Synchrone	SMSC Europe GmbH
G	GB	GB 03 736 882.6	2003-06-04	03 736 882.6	--		Communication System for Sending Dissimilar Types of Data across Synchronous Network	SMSC Europe GmbH
G	IT	IT 03 736 882.6	2003-06-04	03 736 882.6	--		Communication System for Sending Dissimilar Types of Data across a Synchronous Network	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	NL	NL 03 736 882.6	2003-06-04	03 736 882.6	--		Communication System for Sending Dissimilar Types of Data across a Synchronous Network	SMSC Europe GmbH
G	SE	SE 03 736 882.6	2003-06-04	03 736 882.6	--		Communication System for Sending Dissimilar Types of Data across a Synchronous Network	SMSC Europe GmbH
G	EP	EP 1 783 936	2003-06-04	7003305.5	2011-05-11	1 783 936	Communication System For Sending Dissimilar Types Of Data Across A Synchronous Networt Within A Frame Segment Using A Signaling Byte Or Coding Violations To Signify Data Transfers Within The Frame Segment	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	DE	DE	2003-06-04		--		Communication System For Sending Dissimilar Types Of Data Across A Synchronous Networt Within A Frame Segment Using A Signaling Byte Or Coding Violations To Signify Data Transfers Within The Frame Segment	SMSC Europe GmbH
G	GB	GB	2003-06-04		--		Communication System For Sending Dissimilar Types Of Data Across A Synchronous Networt Within A Frame Segment Using A Signaling Byte Or Coding Violations To Signify Data Transfers Within The Frame Segment	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	SE	SE	2003-06-04		--		Communication System For Sending Dissimilar Types Of Data Across A Synchronous Networt Within A Frame Segment Using A Signaling Byte Or Coding Violations To Signify Data Transfers Within The Frame Segment	SMSC Europe GmbH
F	EP	EP 03 788 391.5-1237	2003-08-12	03 788 391.5-1237	--		COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING ..	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	EP	EP 2 262 138	2003-08-12	10183313.5	--		COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP. SAMPLE RATE CONVERSION, OR SYNCHRONIZING ..	SMSC Europe GmbH
G	EP	EP 1 513 284	2004-08-26	04 020 230.1-2415	2008-10-08	1 513 284	CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	DE	DE 04 020 230.1-2415	2004-08-26	04 020 230.1-2415	--		CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE	SMSC Europe GmbH
G	FI	FI 04 020 230.1-2415	2004-08-26	04 020 230.1-2415	--		CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	FR	FR 04 020 230.1-2415	2004-08-26	04 020 230.1-2415	--		CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE	SMSC Europe GmbH
G	GB	GB 04 020 230.1-2415	2004-08-26	04 020 230.1-2415	--		CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	IT	IT 04 020 230.1-2415	2004-08-26	04 020 230.1-2415	--		CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE	SMSC Europe GmbH
G	NL	NL 04 020 230.1-2415	2004-08-26	04 020 230.1-2415	--		CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	SE	SE 04 020 230.1-2415	2004-08-26	04 020 230.1-2415	--		CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE	SMSC Europe GmbH
0	DE	DE	--		--		Patentportfolio	SMSC Europe GmbH
F	EP	EP 1 603 284 A1	2005-05-25	05 011 315.8-2416	--		System and Method for Transferring Data Packets Through a Communication System with Ring Topology to a Multimedia Device Utilizing a Different Communication protocol	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	US	US 2005/0271068 A1	2004-06-02	10/859470	--		SYSTEM AND METHOD FOR TRANSFERRING NON-COMLIANT PACKETIZED AND STREAMING DATA INTO AND FROM A MULTIMEDIA DEVICE COUPLED TO A NETWORK ACROSS WHICH COMPLIANT DATA IS SENT	SMSC Europe GmbH
F	EP	EP 1 648 128 A2	2005-10-04	05 021 620.9	--		SELECTIVE SCRAMBLER FOR USE IN A COMMUNICATION SYSTEM AND METHOD TO MINIMIZE BIT ERROR AT THE RECEIVER	SMSC Europe GmbH
F	US	US 2006/0083328 A1	2004-10-15	10/966,254	--		SELECTIVE SCRAMBLER FOR USE IN A COMMUNICATION SYSTEM AND METHOD TO MINIMIZE BIT ERROR AT THE RECEIVER	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	EP	EP 2007/098412	2007-02-16	7757129.7	--		SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS	SMSC Europe GmbH
F	EP	EP	2007-02-16		--		SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	US	US 2007/0255855 A1	2007-02-16	11/676,001	--		SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS	SMSC Europe GmbH
F	WO	WO 2007/098412	2007-02-16	2007/062328	--		SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	EP	EP 2007/098411	2007-02-16	7757128.9	--		TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSON EFFICIENCY	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	EP	EP 12162658.4	2007-02-16	12162658.4	--		TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSON EFFICIENCY	SMSC Europe GmbH
F	US	US 20070280705A1	2006-06-02	11/421,947	--		Transmission Network Having an Optical Receiver that Utilizes Dual Power Pins and a Single Status Pin to Lower Power Consumption, Lower Manufacturing Cost, and Increase Transmission Efficiency	SMSC Europe GmbH

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	WO	WO 2007/098411	2007-02-16	2007/062327	--		TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSON EFFICIENCY	SMSC Europe GmbH
F	DE	DE 10 2010 000 318	2010-02-05	10 2010 000 318.2-53	--			SMSC Europe GmbH
F	DE	DE 10 2010 000 498	2010-02-22	10 2010 000 498.7-32	--		Frequency Compensation Scheme for Stabilizing a Regulator using an External Transistor in a High Voltage Domain	SMSC Europe GmbH
G	CN	CN 200480043240.4	2004-04-05	200480043240.4	2011-02-02	2.0048E+11	Wireless Audio Transmission System and Method with Dynamic Slot Allocation	Wireless Audio IP

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
G	EP	EP 04725839.7	2004-04-05	4725839.7	--		Wireless Audio Transmission System and Method with Dynamic Slot Allocation	Wireless Audio IP
G	DE	DE	2004-04-05		--		Wireless Audio Transmission System and Method with Dynamic Slot Allocation	Wireless Audio IP
G	FR	FR 04725839.7	2004-04-05	4725839.7	--		Wireless Audio Transmission System and Method with Dynamic Slot Allocation	Wireless Audio IP
G	GB	GB 04725839.7	2004-04-05	4725839.7	--		Wireless Audio Transmission System and Method with Dynamic Slot Allocation	Wireless Audio IP
G	JP	JP 4568755	2004-04-05	4568755	2010-08-13	4568755	Wireless audio Transmission System and Method	Wireless Audio IP
F	US	US 2008/0212582 A1	2004-04-05	11/578,206	--		Wireless audio Transmission System and Method	Wireless Audio IP

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	WO	WO 2005/099156	2004-04-05	2004/000225	--		Wireless Audio Transmission System and Method with Dynamic Slot Allocation	Wireless Audio IP
F	DE	DE 11 2007 000 993.4	2007-04-20	11 2007 000 993.4	--		System und Verfahren für Interferenz- bzw. Störungsidentifikation und Frequenzzuweisung	Wireless Audio IP
G	GB	GB 2482868	2007-04-20	819122.3	2010-06-29	2482868	System and Method for Interence Identification and Frequency Allocation	Wireless Audio IP
F	JP	JP 2009-505905	2007-04-20	2009-505905	--		System and Method for Interence Identification and Frequency Allocation	Wireless Audio IP
F	US	US 2009/0097445 A1	2007-04-20	12/297,828	--		System and Method for Interence Identification and Frequency Allocation	Wireless Audio IP
F	CN	CN 101707896	2007-05-14	2.0078E+11	--		A Method for Communicating Data, a Transmitting Unit and a Computer Programm Product	Wireless Audio IP

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	EP	EP 07747432.8	2007-05-14	7747432.8	--		A Method for Communicating Data, a Transmitting Unit and a Computer Programm Product	Wireless Audio IP
F	JP	JP 2010-508321	2007-05-14	2010-508321	--		A Method for Communicating Data, a Transmitting Unit and a Computer Programm Product	Wireless Audio IP
F	US	US 2010/0150066	2007-05-14	12/600,179	--		A Method for Communicating Data. a Transmitting Unit and a Computer Programm Product	Wireless Audio IP
F	WO	WO 2008/140294 A1	2007-05-14	2007/050208	--		Hybride Protocol	Wireless Audio IP
F	EP	EP 10187165.5	2010-10-11	10187165.5	--		An Integrated Circuit System	Wireless Audio IP
F	JP	JP 2011-222768	2011-10-07	2011-222768	--		An Integrated Circuit System	Wireless Audio IP
F	KR	KR 10-2011-0103721	2011-10-11	10-2011-0103721	--		An Integrated Circuit System	Wireless Audio IP

Status	State	File	Date	App No	Pat Date	Pat No	Title	Assignee
F	US	US 13/270,637	2011-10-11	13/270,637	--		An Integrated Circuit System	Wireless Audio IP

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File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-00100	Method and Apparatus for Configuration Control and Power Management Through Special Signaling	10/25/2001	10/004,390	05/01/2003	2003-0084354 A1	04/19/2005	6,883,105 Foreign filing not pursued.
5707-00200	Novel Data Transmission Architecture (Provisional)	09/08/2000	60/231,391				Foreign filing not pursued.
5707-00201	System and Method for Data Transmission	09/07/2001	09/949,288	08/22/2002	2002-0116561 A1	09/26/2006	7,114,019 Foreign filing not pursued.
5707-00300	Hubless Docking Station Having USB Ports	10/25/2001	09/999,653	05/01/2003	2003-0084222 A1	12/16/2003	6,665,764 Foreign filing not pursued.
5707-00400	A Switchable Hot-Docking Interface for a Portable Computer for Hot-Docking the Portable Computer to a Docking FStation	02/14/2002	10/076,105	08/14/2003	2003-0154338 A1	03/15/2005	6,868,468 EAH PCT and TW apps filed (see 00401 and 00402)
5707-00401 TW	Switched Hot Docking Interface	02/14/2003	092103071	09/01/2003	200303481	10/21/2004	I222591 Annuity due 10/20/11.
5707-00600	Bootable Solid State Floppy Disk Drive	04/18/2002	10/125,697	10/23/2003	2003-0200379 A1	12/01/2009	7,627,464 3.5 Yr. Maint. Fee due 6/01/13. Letters Patent received 12/04/09. Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-00700	Multiple Drive Controller	05/02/2002	10/137,690	11/06/2003	2003-0208651 A1	05/30/2006	7,054,980 3.5 Yr. Maint. Fee paid. Foreign filing not pursued.
5707-00800	Method and Apparatus for Measuring the Rotational Speed of a Fan	07/01/2002	10/188,257	01/01/2004	2004-0001542 A1	08/22/2006	7,096,134 RCS Foreign filing not pursued.
5707-00900	Method and Apparatus for Controlling a Fan	04/10/2002	10/119,983	10/16/2003	2003-0193307 A1	07/11/2006	7,075,261 TAK Foreign filing not pursued.
5707-01100	Power Management of Computer Peripheral Devices Which Determines Non-Usage of a Device Through Usage Detection of Other Devices	02/13/2003	10/366,189			05/22/2007	7,222,252 REH Foreign filing not pursued.
5707-01101	Power Management of Computer Peripheral Devices Which Determines Non-Usage of a Device Through Usage Detection of Other Devices (Continuation of 5707-01100)	02/13/2007	11/674,450	07/12/2007	2007-0162778	03/23/2010	7,685,450 JCH

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-01200	Baseband Filter for Receivers	01/13/2003	10/341,158			03/09/2004	6,703,894 EH 7.5 Yr. Maint. Fee due 09/09/11 Foreign filing not pursued.
5707-01300	Current Controlled Bridge Amplifier	01/31/2003	10/355,859	08/05/2004	2004-0150474	06/14/2005	6,906,587 TAK Foreign filing not pursued.
5707-01500	Selective Implementation of Power Management Schemes Based on Detected Computer Operating Environment	04/09/2003	10/410,089	10/14/2004	2004-0205361 A1	05/30/2006	7,055,047 REH 3.5 Yr. Maint. Fee paid. Foreign filing not pursued.
5707-01600	Crystal Oscillator with Control Feedback to Maintain Oscillation	02/13/2003	10/366,177			11/16/2004	6,819,196 REH Foreign filing not pursued.
5707-01700	Portable RAM Drive	02/11/2003	10/364,583	08/12/2004	2004-0158674 A1	07/19/2005	6,920,527 REH Foreign filing not pursued. 7.5 Yr. Maint. Fee due 01/19/13

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-01800	Double Buffered Flash Programming	02/28/2003	10/376,838	09/02/2004	2004-0172496 A1	10/24/2006	7,127,564 REH/TAK 3.5Yr Main Fee Paid Foreign filing not pursued.
5707-01900	Amplifier Circuit With Common Mode Feedback	12/18/2003	10/739,797	06/23/2005	2005-0134382 A1	08/30/2005	6,937,100 EAH Foreign filing not pursued. 7.5 Yr. Maint. Fee due 02/28/13
5707-02000	Dynamic, Digitally Controlled, Temperature Compensated Voltage Reference	06/02/2003	10/452,697	12/02/2004	US 2004 0243950 A1	04/26/2005	6,885,243 TAK Foreign filing not pursued.
5707-02100	Memory Bus Interface for Use in a Peripheral Device	12/11/2002	10/316,363	06/17/2004	2004-0117565 A1	02/21/2006	7,003,638 BAB/TAK Foreign filing not pursued. 7.5 Yr. Maint. Fee due 8/21/13.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-02200	Universal Serial Bus Hub with Shared High Speed Handler	02/24/2003	10/374,852	08/26/2004	2004-0168009 A1	10/25/2005	6,959,355 BAB/TAK Foreign filing not pursued. 7.5 Yr. Maint. Fee due 04/25/13
5707-02201	Universal Serial Bus Hub With Shared High Speed Handler Implementing Respective Downstream Transfer Rates (Divisional of 5707-02200)	09/09/2005	11/223,570	01/26/2006	2006-0020737 A1	01/27/2009	7,484,018 REH Foreign filing not pursued.
5707-02300	Universal Serial Bus Hub With Shared Transaction Translator Memory	02/24/2003	10/374,162	08/26/2004	2004-0168001 A1	02/27/2007	7,185,126 BAB/TAK Foreign filing not pursued.
5707-02700	Communication Protocol for Personal Computer System Human Interface Devices over a Low Bandwidth, Bi-Directional Radio Frequency Link	04/09/2003	10/410,088	10/14/2004	US 2004 0203388 A1	12/18/2007	7,310.498 REH Foreign filing not pursued. 11/07/2007 Client instructed us not to file continuation or divisional application.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-02900	Parabolic Control of the Duty Cycle of a Pulse Width Modulated Signal	05/19/2003	10/440,606	11/25/2004	US 2004 0232869 A1	08/23/2005	6,933,697 RCS Foreign filing not pursued. 7.5 Yr. Maint. Fee due 02/23/13
5707-03000	All Digital PLL Trimming Circuit	09/2/2003	10/653,614	03/03/2005	US 2005 0046452 A1	05/31/2005	6,900,675 TAK Foreign filing not pursued.
5707-03100	Current-Mode Direct Conversion Receiver	03/08/2004	10/795,740	09/08/2005	US 2005 0197090 A1	08/19/2008	TAK 7,415,260 Foreign filing not pursued.
5707-03200	Temperature-to-Digital Converter	07/22/2003	10/624,394	01/27/2005	US 2005 0017889	01/25/2005	6,847,319 TAK Foreign filing not pursued.
5707-03300	Piecewise Linear Control of the Duty Cycle of a Pulse Width Modulated Signal	05/19/2003	10/440,745	11/25/2004	US 2004 0234376 A1	04/18/2006	7,029,239 RCS 3.5 Yr. Maint. Fee has been paid. Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-03301	Generating a PWM Signal Dependent on a Duty Cycle Having a Piecewise Linear Relationship With Temperature (Continuation)	03/31/2006	11/395,004	08/31/2006	2006-0193729		JCH Reply Brief filed 12/20/10.
5707-03500	Delta Vgs Curvature Correction for Bandgap Reference Voltage Generation	05/29/2003	10/447,569	12/02/2004	US 2004 0239411 A1	02/15/2005	6,856,189 BAB/TAK Foreign filing not pursued.
5707-03600	Efficient Class-G Amplifier with Wide Output Voltage Swing	07/17/2003	10/622,051	01/20/2005	US 2005 0012554 A1	01/04/2005	6,838,942 JDC Foreign filing not pursued.
5707-03700	FSK Modulator Using IQ p-Mixers and Sinewave Coded DACs	09/02/2003	10/653,322	03/03/2005	US 2005 0048931 A1	05/09/2006	7,043,222 TAK 3.5 Yr. Maint. Fee paid. Foreign filing not pursued.
5707-03800	Phase Detector for Low Power Applications	05/23/2003	10/444,670			10/19/2004	6,806.742 JDC 3.5 Yr. Maint. Fee paid. Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-03900	Associative Noise Attenuation	05/06/2003	10/430,863			11/30/2004	6,825,786 BAB/TAK Foreign filing not pursued.
5707-04000	Highly Accurate Switched Capacitor DAC	02/27/2004	10/789,903			08/02/2005	6,924.760 TAK Foreign filing not pursued. 7.5 Yr. Maint. Fee due 02/02/13
5707-04100	Amplifier with Accurate Built-in Threshold	09/22/2003	10/667,535	04/14/2005	US 2005 0077954 A1	06/06/2006	7,057,444 3.5 Yr. Maint. Fee paid. Foreign filing not pursued.
5707-04200	Programmable PWM Stretching for Tachometer Measurement	06/11/2003	10/459,169	12/23/2004	US 2004 0257024 A1	07/19/2005	6,919,703 TAK Foreign filing not pursued.
5707-04300	An Integrated Relaxation Oscillator With Improved Sensitivity to Component Variation Due to Process-Shift	10/10/2003	10/683,621	04/14/2005	US 2005 0077971 A1	08/02/2005	6,924,709 TAK Foreign filing not pursued. 7.5 Yr. Maint. Fee due 01/02/13

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-04400	Mapping a Plurality of Sensors to Respective Zones in a Fan Control System	02/23/2004	10/784,837	08/25/2005	US 2005 0186083 A1	11/13/2007	7,295,897 TAK Counterpart applications filed in Taiwan and Japan (see 04401 and 04402)
5707-04402 TW	Mapping a Plurality of Sensors to Respective Zones in a Fan Control System	02/22/2005	094105310	12/01/2005	200539558	02/29/2008	I298578 TAK Annuity Due 6/30/11.
5707-04500	Method and Apparatus for Handling Interrupts	11/12/2003	10/706,741	05/12/2005	US 2005 0102460 A1	11/21/2006	7,139,857 EAH Foreign filing not pursued.
5707-04700	Accurate Testing of Temperature Measurement Unit	02/18/2004	10/781,063	08/18/2005	US 20050179575 A1	04/18/2006	7,030,793 JDC 3.5 Yr. Maint. Fee has been paid. Foreign filing not pursued. Divisional application not pursued.
5707-04800	Fan Control System with Improved Temperature Resolution	12/01/2003	10/724,927			04/05/2005	6,874,327 TAK Taiwanese counterpart filed (see 04801)

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-04801 TW	Fan Control System with Improved Temperature Resolution	11/30/2004	093136960	07/01/2005	200522498	01/21/2008	I292981 TAK Annuity due 1/20/2011
5707-04900	Method And Apparatus For Generating Accurate Fan Tachometer Readings	08/08/2003	10/637,468	02/24/2005	US 2005 0040777 A1	07/11/2006	7,076,159 TAK Taiwanese counterpart filed. (see 04901)
5707-04901 TW	Method And Apparatus For Generating Accurate Fan Tachometer Readings	08/02/2004	093123051	03/01/2005	200509535		TAK Request for examination filed 04/13/07.Resp to OA filed.
5707-05100	Method And Apparatus To Achieve Accurate Fan Tachometer With Programmable Look-Up Table	09/22/2003	10/668,062	10/27/2005	US 2005 0238336 A1	08/15/2006	7,092,623 TAK Foreign filing not pursued.
5707-05200	Linear Half-Rate Clock and Data Recovery (CDR) Circuit	09/23/2004	10/947,891	03/23/2006	US 2006 0062339 A1	10/07/2008	7,433,442 MJL Foreign filing not pursued. Original Letters Patent received 10/13/08.
5707-05400	Failsafe Slave Mechanism for Mission Critical Applications	08/16/2004	10/919,083	02/16/2006	US 20060036879 A1	12/04/2007	7,305.570 MJL Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-05800	Autofan Combination of Zones	01/16/2004	10/759,796	07/21/2005	US 2005 0156544 A1	06/20/2006	7,064,511 TAK Taiwanese and Japanese counterparts filed (see 05801 and 05802).
5707-05802 TW	Autofan Combination of Zones	01/14/2005	094101196	11/16/2005	200537280	09/01/2007	I286276 TAK Annuity due 08/31/11.
5707-05900	Method and Circuit for Fuse Programming and Endpoint Detection	06/07/2004	10/862,675	12/08/2005	US 2005 0270085 A1	03/07/2006	7,009,443 MJL Foreign filing not pursued.
5707-06000	Peripheral Device Feature Allowing Processors to Enter a Low Power State	01/20/2004	10/762,767			01/09/2007	REH 7,159.766 Taiwanese and Japanese counterpart applications filed (see 06001 and 06002)
5707-06002 TW	Peripheral Device Feature Allowing Processors to Enter a Low Power State	01/19/2005	094101565	01/16/2006	200603001	09/21/2008	I301245 REH Annuity due 9/20/11.
5707-06003	Electrically Disconnecting a Peripheral Device (Continuation of 5707-06000)	09/12/2006	11/530,977	02/01/2007	US 2007 0023499 A1	02/05/2008	7,325,733 JLS

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-06200	Systems and Methods for Power Reduction in Systems Having Removable Media Devices	01/20/2004	10/762,684	07/21/2005	US 2005 0156041 A1	08/08/2006	7,086,583 REH Taiwanese and Japanese counterpart applications (see 06201 and 06202)
5707-06202 TW	Systems and Methods for Power Reduction in Systems Having Removable Media Devices	01/19/2005	094101568	11/01/2005	200535711	12/25/2006	I279730 REH Annuity due April 20, 2011
5707-06203	Systems and Methods for Power Reduction in Systems Having Removable Media Devices (Continuation of 5707-06200)	02/21/2006	11/359,033	06/29/2006	US 2006 0138230 A1	05/01/2007	7,210,619 JLS
5707-06300	Automatic Drive ICON Assignment By Media Type In Single Slot USB Card Readers	01/20/2004	10/762,679			11/07/2006	7,131,595 REH 3.5 Yr Main Fee Paid. Foreign filing not pursued.
5707-06900	Secure Authentication Using A Low Pin Count Based Smart Card Reader	11/22/2004	10/995,000	05/25/2006	US 2006 0112423 A1	12/08/2009	7,631,348 IMF 3.5 Yr. Maint. Fee due 6/08/13. Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-07200	Integrated Resistance Cancellation in Temperature Measurement Systems	08/23/2004	10/924,176	02/23/2006	US 2006 0039445 A1	10/16/2007	TAK 7,281,846 Taiwanese counterpart filed. (see 07201)
5707-07201 TW	Integrated Resistance Cancellation in Temperature Measurement Systems	08/23/2005	094128763	07/16/2006	200624786		Request for examination filed 4/22/08.
5707-07300	Method and Apparatus to Achieve Accurate Fan Tachometer Readings for Fans with Different Speeds	05/11/2004	10/843,199	11/17/2005	US 2005 0256670 A1	06/27/2006	7,069,172 3.5 Yr. Maint. Fee paid. Foreign filing not pursued.
5707-07400	A Method For Maintaining Register Integrity And Receive Packet Protection During ULPI PHY To LINK Bus Transactions	01/27/2005	11/044,446	07/27/2006	US 2006 0168364 A1	03/24/2009	7,509,439 Foreign filing not pursued. Original Letters Patent and soft copies received 3/30/09
5707-07601 TW	Budget Sensor Bus	08/23/2005	094128761	09/01/2006	200630812		TAK Request for examination filed 4/23/08.
5707-07700	Method for Fast Access to Flash-Memory Media	04/04/2005	11/098,707	10/05/2006	US: 2006 0224818-A1	12/07/2010	7,849,253 TAK Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-07900	Programmable Ideality Factor Compensation in Temperature Sensors	11/02/2004	10/979,437	05/04/2006	US 2006 0093016 A1	11/28/2006	7,140,767 TAK Taiwanese counterpart filed. (see 07902)
5707-07901	Not Used						
5707-07902 TW	Programmable Ideality Factor Compensation in Temperature Sensors	11/02/2005	094138491	09/01/2006	200630599		TAK Examination deadline filed 10/23/08.
5707-08001 PCT	Universal Serial Bus Switching Hub	09/09/2005	PCT/US05/32493	03/23/2006	WO 2006/031776		REH Combined International Search Report and Written Opinion issued. Response/demand filed. IPRP issued. PCT complete. National Phase Counterparts filed in EP, JP, KR and SG (see 08004-08007)
5707-08100	Proportional Settling Time Adjustment for Diode Voltage and Temperature Measurements Dependent on Forced Current Level	02/28/2005	11/068,250	08/31/2006	2006-0193370	09/30/2008	TAK 7,429,129 Taiwanese counterpart filed (see 08101)

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-08101 TW	Proportional Settling Time Adjustment for Diode Voltage and Temperature Measurements Dependent on Forced Current Level	02/27/2006	095106644	12/16/2006	2006643390		TAK Request for examination filed 2/27/09.
5707-08102	Proportional Settling Time Adjustment for Diode Voltage and Temperature Measurements Dependent on Forced Current Level (Divisional)	09/16/2008	12/211,673	01/08/2009	2009-0009234		TAK RCE and Response to Final Office Action filed 3/6/12.
5707-08200	Trusted LPC Docking Interface For Docking Notebook Computers To A Docking Station	02/18/2005	11/061,146	08/24/2006	2006-0190653	03/29/2011	7,917,679 TAK Taiwanese counterpart filed (see 08201) Per client, do not file a divisional application.
5707-08201 TW	Trusted LPC Docking Interface For Docking Notebook Computers To A Docking Station	02/17/2006	095105422				TAK Re-exam Brief filed.
5707-08300	Automatic Reference Voltage Trimming Technique	06/06/2005	11/145,906			10/07/2008	7,433,790 TAK Foreign filing not pursued.
5707-08700	Hardware Supported Peripheral Component Memory Alignment Method	11/02/2004	10/979,924	05/04/2006	US 2006 0095611 A1		TAK PCT and Taiwanese counterpart applications filed. (see 08701 and 08702) Allowed. Issue Fee due 4/30/12.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-08701 PCT	Hardware Supported Peripheral Component Memory Alignment Method	11/01/2005	PCT/US05/39360	05/11/2006	WO 2006/050311		TAK Search Report/Written Opinion issued. Response filed. IPRP issued. PCT Complete. Entered national phase in JP, KR and EP (with later validations in DE, FR and UK)
5707-08800	High Voltage Power Supply Clamp Circuitry for Electrostatic Discharge (ESD) Protection	06/06/2005	11/145,903			06/22/2010	7,742,265 TAK Foreign filing not pursued. Allowed. Issue fee paid 5/06/10.
5707-08900	High Speed Ethernet MAC and PHY Apparatus with a Filter Based Ethernet Packet Router with Priority Queuing and Single or Multiple Transport Stream Interfaces (Foxboro)	01/28/2005	11/046,292	08/03/2006	US 2006 0174032 A1		TAK Counterpart PCT, TW, JP and KR cases filed (see 08901 – 08904) RCE and Response to Final Office Action filed 6/15/11.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-08901 PCT	High Speed Ethernet MAC and PHY Apparatus with a Filter Based Ethernet Packet Router with Priority Queuing and Single or Multiple Transport Stream Interfaces	01/04/2006	PCT/US06/00126 Published as WO 2006/083467 on 8/10/06				TAK IPRP issued. PCT Complete. National counterparts filed in SG and EP (later to validate in DE, FR and UK after grant). (See 08905 and 08906)
5707-09000	Power Managed USB for Computing Applications Using A Controller	03/04/2005	11/071,961				REH Reply Brief filed 3/30/09. Taiwanese counterpart filed (see 09001)
5707-09001 TW	Power Managed USB for Computing Applications Using A Controller	03/03/2006	095107320	10/16/2006	200636438.		REH Request for examination filed 3/3/09
5707-09100	Dynamic Hysteresis for Auto Fan Control	12/27/2005	11/318,866	06/28/2007	US 2007 0145934 A1	07/01/2008	TAK 7,394,217 Taiwanese counterpart filed (see 09101)

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-09101 TW	Dynamic Hysteresis for Auto Fan Control	12/27/2006	095149301	09/16/2007	200734860		TAK Request for examination filed 10/7/09
5707-09202 TW	Peripheral Sharing USB Hub	04/06/2006	095112273	03/01/2007	200709519		REH Request for examination filed 3/26/09.
5707-09203 PCT	Peripheral Sharing USB Hub	04/06/2006	PCT/US06/13299			Closed	REH IPRP issued. National counterpart applications filed in EP, JP, KR and SG. (See 09204 through 09207).
5707-09300	Microcontroller-Based Integrated Adaptive PID Controller for PC Cooling Fans (Provisional)	11/24/2004	60/631,058				TAK Foreign filing not pursued.
5707-09301	Adaptive Controller for PC Cooling Fans	11/23/2005	11/286,529	05/25/2006	US 2006 0108962 A1	11/21/2006	7,138,781 TAK Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-09701 TW	Perfectly Curvature Corrected Bandgap Reference	09/01/2006	095132631	08/01/2007	200728950		TA Request for examination due 9/1/09. Exam instructions have been acknowledged.
5707-09800	EMI Rejection for Temperature Sensing Diodes	09/02/2005	11/219,151	03/08/2007	US 2007 0055473 A1	11/24/2009	TAK 7,622,903 3.5 Yr. Maint. Fee due 5/24/13. Taiwanese counterpart filed. (See 09801)
5707-09801 TW	EMI Rejection for Temperature Sensing Diodes	09/01/2006	095132630	09/01/2007	200732636		TAK Request for Exam filed.
5707-09900	Conversion Clock Randomization for EMI Immunity in Temperature Sensors	09/02/2005	11/219,399	03/08/2007	US 2007 0052561 A1	03/20/2007	7,193,543 TAK Taiwanese counterpart filed (see 09901)
5707-09901 TW	Conversion Clock Randomization for EMI Immunity in Temperature Sensors	09/01/2006	095132632	09/01/2007	200732640		TAK Request for examination filed.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-10000	Accurate Temperature Measurement Method for Low Beta Transistors	11/23/2005	11/286,706	05/24/2007	US-2007-0115042	02/19/2008	7,332,952 Taiwanese counterpart filed (see 10001)
5707-10001 TW	Accurate Temperature Measurement Method for Low Beta Transistors	11/23/2006	095143435	08/16/2007	200731661		TAK Request for examination due 11/23/09
5707-10200	Method For a Slave Device to Convey an Interrupt and Interrupt Source Information to a Master Device	02/03/2006	11/3 46,729	08/09/2007	US-2007-0186021	07/01/2008	TAK 7,395,362 Taiwanese counterpart filed (see 10201)
5707-10201 TW	Method For a Slave Device to Convey an Interrupt and Interrupt Source Information to a Master Device	01/24/2007	096102714	02/16/2008	200809515		TAK Request for examination filed 7/11/08.
5707-10300	Method For Changing Ownership Of A Bus Between Master/Slave Devices	02/06/2006	11/348,219	08/09/2007	US-2007-10300		TAK Taiwanese counterpart filed (see 10301) Allowed. Issue Fee due **4/19/12**.
5707-10301 TW	Method For Changing Ownership Of A Bus Between Master/Slave Devices	01/24/2007	096102713	04/16/2008	200817915		TAK Request for examination filed 10/12/09

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-10400	Ramp Rate Closed-Loop Control (RRCC) for PC Cooling Fans (CIP of 5707-09301)	01/30/2006	11/343,637	05/31/2007	US-2007-0124574	09/16/2008	TAK 7,425,812 Taiwanese counterpart filed (see 10401)
5707-10401 TW	Ramp Rate Closed-Loop Control (RRCC) for PC Cooling Fans (CIP of 5707-09301)	11/22/2006	095143284	02/16/2008	200810345		TAK Request for examination due 11/22/09
5707-10500	Transferring System Information Via Universal Serial Bus (USB)	01/24/2006	11/338,924			10/07/2008	7,433,990 REH Foreign filing not pursued.
5707-10600	Fringe Capacitor Using Bootstrapped Non-Metal Layer	03/20/2006	11/384,961	09/20/2007	US-2007-0215928	12/13/2011	8,076,752 TAK Taiwanese and Japanese counterpart filed. (see 10601 and 10602)
5707-10601 TW	Fringe Capacitor Using Bootstrapped Non-Metal Layer	03/20/2007	096109585				TAK Examination filed. Response to OA due 3/3/11 Patent No. I347669 issued 8/21/11

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-10602 JP	Fringe Capacitor Using Bootstrapped Non-Metal Layer	03/20/2007	2007-72142				TAK Examination filed. Awaiting further action.
5707-10603	High-Density Capacitor Configured On a Semiconductor (Divisional of 5707-10600)	11/23/2011	13/303,318				Response to Notice to File Corrected Application Papers filed 12/30/11.
5707-10604	Circuit with High-Density Capacitors Using Bootstrapped Non-Metal Layer (Divisional of 5707-10600)	11/23/2011	13/303,381				Response to Notice to File Corrected Application Papers filed 12/30/11.
5707-10605	Fringe Capacitor Using Bootstrapped Non-Metal Layer (Continuation of 5707-10600)	11/23/2011	13/303,437				Response to Notice to File Corrected Application Papers filed 12/30/11.
5707-10700	Voltage Regulator with Inherent Voltage Clamping	05/05/2006	11/429,098	11/08/2007	US-2007-0257644	10/13/2009	TAK 7,602,161 Foreign filing not pursued.
5707-10800	Virtual FIFO Automatic Data Transfer Mechanism	02/16/2006	11/355,677	08/16/2007	US-2007-0192516		MJL Foreign filing not pursued. Response to Office Action filed 1/17/12.
5707-10900	Current Limiting Circuit	03/10/2006	11/373,390	09/13/2007	US-2007-0210726	10/19/2010	7,816,897 Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-11100	Method for Implementing a Counter in a Memory with Increased Memory Efficiency	02/16/2006	11/355,685	8/16/2007	US-2007-0189082	05/06/2008	JLS 7,369,432 Taiwanese counterpart filed. (See 11101)
5707-11101 TW	Method for Implementing a Counter in a Memory with Increased Memory Efficiency	02/15/2007	096105769	02/16/2008	200809861	09/01/2010	JLS Request for examination filed. Response to Office Action filed. 2nd annuity due 8/31/11. Patent No. I329874 on 9/1/10.
5707-11200	Driver with Variable Output Voltage and Current	06/21/2006	11/425,585	12/27/2007	US-2007-0296463	02/19/2008	7,332,935
5707-11400	Address Assignment Through Device ID Broadcast	05/03/2006	11/417,775	12/20/2007	US-2007-0294443	12/08/2009	MJL 7,631,110 Taiwanese counterpart filed. (See 11401)
5707-11401 TW	Address Assignment Through Device ID Broadcast	05/02/2007	096115623	04/01/2008	200815985		MJL Request for examination filed. Response to Office Action filed.
5707-11500	In-Band Interrupt Polling (Provisional)	05/05/2006	60/798,284				MJL Proceed per MK email.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-11501	In Band Event Polling	08/31/2006	11/469,267	01/03/2008	US-2008-0005379	06/21/2011	7,966,379 Taiwanese counterpart filed. (See 11502)
5707-11502 TW	In Band Event Polling	05/03/2007	096115724	04/16/2008	200817917		MJL I351614 issued on 11/1/11
5707-11600	Method, System, and Apparatus for a Plurality of Slave Devices Determining Whether to Adjust Their Power State Based on Broadcasted Power State Data	05/03/2006	11/417,855	11/0/2007	US-2007-0260901	04/27/2010	7,707,437 Taiwanese counterpart filed. (See 11601)
5707-11601 TW	System Power State Broadcast Through the Use of a Bus Protocol	05/03/2007	096115726	04/01/2008	200815993		MJL Request for examination filed. Response to OA due 2/25/11. Patent No. I347524 issued 8/21/11
5707-11700	Current Limiting Protection Circuit	01/10/2007	11/621,595	07/10/2008	US-2008-0165465	07/28/2009	7,567,119 Foreign filing not pursued.
5707-11800	Resistor/Capacitor Based Identification Detection	07/24/2006	11/459,413	02/21/2008	US-2008-0042701	12/08/2009	7,631,176 TAK 3.5 Yr. Maint. Fee due 6/08/13. Taiwanese counterpart filed. (See 11801)

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-11801 TW	Resistor/Capacitor Based Identification Detection	07/23/2007	096126802	02/21/2008	0042701		TAK Request for examination filed. Awaiting further action.
5707-11900	System and Method for Rapidly Charging a USB Device	08/17/2006	11/465,189	02/21/2008	US-2008-0042616	12/08/2009	7,631,111 JLS Taiwanese counterpart filed. (See 11901) 3.5 Yr. Maint. Fee due 6/08/13. Comment on Notice of Allowability filed 10/26/09.
5707-11901 TW	System and Method for Rapidly Charging a USB Device	08/17/2007	096130589	05/01/2008	200820542		JLS Request for examination filed. Awaiting further action.
5707-12000	System and Method for Universal Serial Bus Hub Port Reversal	04/27/2006	11/412,431	11/01/2007	US-2007-0255885	01/20/2009	7,480,753 JLS Taiwanese, Singapore and Korean counterparts filed. See 12001-12003)

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-12001 TW	System and Method for Universal Serial Bus Hub Port Reversal	04/13/2007	096112956	05/16/2008	200821846		JLS Request for examination filed. Awaiting further action.
5707-12002 SG	System and Method for Universal Serial Bus Hub Port Reversal	04/27/2007	200703057-0				JLS Grant fee due **10/26/09**
5707-12003 KR	System and Method for Universal Serial Bus Hub Port Reversal	04/19/2007	10-2007-38292				JLS Awaiting Letters patent document.
5707-12100	Serialized Secondary Bus Architecture	05/03/2006	11/417,391	11/08/2007	US-2007-0260804		MJL Taiwanese counterpart filed. (See 12101) RCE and FOA filed 2/7/2012.
5707-12101 TW	Serialized Secondary Bus Architecture	05/03/2007	096115725	04/16/2008	200817916		MJL Request for examination filed. Awaiting further action.
5707-12300	Method for Automatically Switching USB Peripherals Between USB Hosts (Provisional)	04/14/2006	60/792,247				JCH This provisional filed on 04/14/06 encompassed subject matter from 12400 as well.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-12301	Method for Automatically Switching USB Peripherals Between USB Hosts	07/13/2006	11/457,389			01/13/2009	7,478,191 TAK PCT and Taiwanese counterpart applications filed. (See 12302-12303)
5707-12303 TW	Method for Automatically Switching USB Peripherals Between USB Hosts	04/14/2007	096113162	04/16/2008	200817973		TAK Request for examination filed. Response to OA filed.
5707-12701	Multi-Host USB Device Controller	06/21/2006	11/425,613			04/21/2009	7,523,246 Taiwanese, Singapore and Korean counterparts filed. (See 12702-12704)
5707-12702 TW	Multi-Host USB Device Controller	04/13/2007	096113030	03/16/2008	200813725	10/27/2010	TAK Request for examination filed. Response to Office Action due 9/17/10. Response to OA filed.
5707-12703 SG	Multi-Host USB Device Controller	04/13/2007	200702711-3	11/29/2007	136906		TAK Response to Examiner's Action Due August 13, 2009. Payment of grant fees due 2/24/10.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-12704 KR	Multi-Host USB Device Controller	04/16/2007	10-2007-0037075				TAK Response to office action filed 6/23/08. Granted; issued fees paid; awaiting letters patent.
5707-12705 KR DIV	Multi-Host USB Device Controller (Divisional of 5707-12704)	11/13/2008	10-2008-112594				TAK Divisional of 12704 Request for exam due 4/16/12
5707-12706	Multi-Host USB Device (Continuation of 5707-12701)	12/22/2008	12/340,957	04/23/2009	US-2009-0106474	12/01/2009	TAK 7,627,708 3.5 Yr. Maint. Fee due 6/01/13. Letters Patent received 12/04/09.
5707-12800	Pad ESD Spreading Technique	01/10/2007	11/621,724	07/10/2008	US-2008-0165459		TAK Allowed. Issue fee paid. Foreign filing not pursued.
5707-12900	Low Power Three-Level Detector	09/29/2006	11/536,241	04/03/2008	US-2008-0079464	01/20/2009	7,479,809 TAK Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-13001 TW	Peripheral Sharing USB Hub for a Wireless Host	06/15/2007	096121987	05/16/2008	200821847		REH Request for examination filed. Awaiting action.
5707-13100	System and Method for Enumerating a USB Device Using Low Power	08/17/2006	11/465,195	05/29/2008	U.S.-2008-0126594-A1	11/24/2009	JLS 7,624,202 Foreign counterpart application filed in Taiwan. (See 13101)
5707-13101 TW	System and Method for Enumerating a USB Device Using Low Power	08/17/2007	096130592	06/16/2008	200825699		JLS Patent No. I356295 issued 1/11/12
5707-13200	Improved Processor Temperature Measurement Through Median Sampling	11/07/2006	11/557,405	05/29/2008	U.S.-2008-0125915-A1	08/02/2011	7,991,514 Foreign counterpart application filed in Taiwan (See 13201)
5707-13201 TW	Improved Processor Temperature Measurement Through Median Sampling	11/07/2007	096142090				TAK Request for examination filed. Awaiting action.
5707-13300	Low Power and Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface (Provisional)	06/07/2006	60/804,141				TAK

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-13301	Low Power and Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	06/30/2006	11/428,211	12/13/2007	US-2007-0288671-A1	04/20/2010	7,702,832 TAK Taiwanese counterpart and PCT filed. (See 13302 and 13303)
5707-13302 PCT	Low Power and Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	06/06/2007	PCT/US07/70521	12/13/2007	WO 2007/143695		TAK Response to Written Opinion filed; IPRP issued 7/25/08. National applications filed in EU, JP, KR and SG
5707-13303 TW	Low Power and Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	06/07/2007	096120566	05/01/2008	200820003		TAK Request for examination filed. Amendments filed Awaiting action. Notice of Allowance received. Cert fee and annuity due 12/28/10.
5707-13304 JP	Low Power and Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	02/09/2009	2009-514514				TAK Patent No. 4918134 issued 02/03/12
5707-13305 KR	Low Power and Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	01/07/2009	10-2009-700286	01/07/2009			TAK Examination due 6/7/12
5707-13306 SG	Low Power and Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	12/02/2008	200808917-9				TAK Granted as patent no. 148370. .Annuity due 6/6/11.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-13307 EP	Low Power and Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	12/29/2008	07812039.1			09/01/2010	TAK Annuity paid Grant fees and divisionals due 8/5/10. Issued under serial no. 2033104 on 9/1/10. Certificate of Grant rec'd 9/13/10.
5707-13308	Digital Device Interconnect System (Continuation of 5707-13301)	04/19/2010	12/762,757	08/15/2010	US-2010-0205337-A1	11/15/2011	8,060,678
5707-13309	Digital Device Interconnect Method (Continuation of 5707-13301)	04/19/2010	12/762,823	08/15/2010	US-2010-0205339-A1	11/08/2011	8,055,825
5707-13310 EP DIV	Low Power And Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	06/14/2010	10165859.9	08/25/2010	2221731	3/14/12	2221731
5707-13311 EP-DE	Low Power And Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	12/29/2008	602007008894.1-08			09/01/2010	Issued under serial no. 2033104. Annuity due 6/6/2011
5707-13312 EP-FR	Low Power And Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	12/29/2008	07812039.1			09/01/2010	Issued under serial no. 2033104. . Annuity due 6/6/11.
5707-13313 EP-GB	Low Power And Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	12/29/2008	07812039.1			09/01/2010	Issued under serial no. 2033104. Annuity due 6/6/11.
5707-13314	Digital Device Interconnect Interface and System (Continuation of 5707-13308)	09/27/2011	13/246,365				TAK Response to Notice to File Corrected Application Papers filed 12/13/11.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-13315 DE	Low Power And Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	06/14/2010	602007021388.6			3/14/12	2221731
5707-13316 FR	Low Power And Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	06/14/2010				3/14/12	2221731
5707-13317 GB	Low Power And Low Pin Count Bi-Directional Dual Data Rate Device Interconnect Interface	06/14/2010				3/14/12	2221731
5707-13401 TW	Plain Language Announcement of Diagnostic and Troubleshooting Information for Users	07/13/2007	096125661	01/17/2008	0016385		JLS Request for examination filed. Awaiting action.
5707-13500	Two-Cycle Return Path Clocking	08/31/2006	11/469,287	03/06/2008	US-2008-0059667-A1	02/15/2011	7,890,684 MJL
5707-13501 TW	Two-Cycle Return Path Clocking	08/31/2007	096132637	07/16/2008	200830108		MJL Request for examination filed. Awaiting action.
5707-13600	Class AB Rail-to-Rail Input and Output Operational Amplifier	04/30/2007	11/742,516	10/30/2008	US-2008-0265993-A1	06/09/2009	7,545,214 Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-14400	Regulator Circuit with Multiple Supply Voltages	01/05/2007	11/620,246	07/10/2008	0164765	01/12/2010	TAK 7,646,115 Foreign filing not pursued. Allowed. Issue fee paid 12/01/09.
5707-14800 (formerly 68987-020)	Method and Apparatus for Power Supply Switching With Logic Integrity Protection	07/23/1996	08/685,376			08/04/1998	5,790,873 08/21/06 Tranferred from Proskauer Rose LLP.
5707-14801 JP (formerly 68987-025)	Method and Apparatus for Power Supply Switching With Logic Integrity Protection	07/23/1997	9-197613	07/10/2008	3950200	4/27/2007	Decision to Grant issued. Annuity due 4/27/11. 08/21/06 Tranferred from Proskauer Rose LLP.
5707-14805 TW (formerly 68987-021)	Method and Apparatus for Power Supply Switching With Logic Integrity Protection	07/14/1997	86109886			09/01/1998	Annuity due 9/1/11. 08/21/06 Tranferred from Proskauer Rose LLP.
5707-14900 (formerly 68987-026)	Method and Apparatus for Power Management in a Multifunction Controller with an Embedded Microprocessor	07/23/1996	08/685,378			12/08/1998	5,848,281 08/21/06 Tranferred from Proskauer Rose LLP.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-15300	Oscillator Stabilized for Temperature and Power Supply Variations	08/24/2007	11/924,826	02/26/2009	US-2009-0051443-A1		TAK Foreign filing not pursued. Allowed. Issue Fee due 5/24/12.
5707-15600	Implementation of One Time Programmable Memory with Embedded Flash Memory in a System-on-Chip	10/26/2007	11/924,826			08/02/2011	7,991,943 Foreign counterpart filed in Taiwan. (See 15601)
5707-15601 TW	Implementation of One Time Programmable Memory with Embedded Flash Memory in a System-on-Chip	10/27/2008	097141206	07/01/2009	200929223		MSW Request for exam due 10/27/11.
5707-15700	Electrical Physical Layer Activity Detector	03/18/2008	12/050,223	09/24/2010	US-2009-0237117-A1	08/02/2011	7,990,182 Foreign counterpart filed in PCT. (See 15701)
5707-15701 PCT	Electrical Physical Layer Activity Detector	03/17/2009	PCT/US09/37367	09/24/2009	2009117394		TAK 30 Month National Counterparts Due 09/18/10. IPRP rec'd 10/13/10.
5707-15702 EP	Electrical Physical Layer Activity Detector	10/18/2010	09723203.7				TAK

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-15703 JP	Electrical Physical Layer Activity Detector	09/21/2010	2011-500891				TAK Filing instructions sent to associate. Translation due 11/18/10.
5707-15704 KR	Electrical Physical Layer Activity Detector	10/18/2010	1020107023284			12/26/11	TAK 10-1101461
5707-15705	Symmetrical Electrical Physical Layer Activity Detector (Divisional of 5707-15700)	07/14/2011	13/182,576	11/03/2011	US-2011-0267110-A1	3/20/12	8,138,802
5707-15800 TW (formerly 68987-033)	Method and Apparatus for the Sharing of a Memory Device by Multiple Processors	07/10/1997	86109707			09/21/1998	Annuity due 9/21/11
5707-15900 TW (formerly 68987-036)	Relocatable Code Storage in an Integrated Circuit with an Embedded Microprocessor	07/14/1997	86109888			09/01/2001	Annuity due 9/01/1
5707-16000	Network Traffic Controller with Multimedia Co-Processor (Provisional)	11/08/2006	60/864,921				TAK **MK: may have been superseded** Foreign counterpart applications filed in PCT and TW (see 16002-16003)

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-16001	Network Traffic Controller (NTC)	10/30/2007	11/928,647	05/08/2008	US-2008-0109562-A1		TAK Foreign counterpart applications filed in PCT and TW (see 16002-16003) RCE and Response to Final Office Action filed 2/23/11.
5707-16002 PCT	Network Traffic Controller	11/08/2007	PCT/US07/84152				TAK PCT complete
5707-16003 TW	Network Traffic Controller	11/08/2007	096142269	10/01/2008	200839535		TAK Request for exam filed. Awaiting action
5707-16004 JP	Network Traffic Controller	11/08/2007	TBA			11/25/2011	TAK Request for Exam filed. Patent No. 4870819
5707-16005 SG	Network Traffic Controller	11/08/2007	200903152-7			10/31/2011	TAK Response to Written Opinion due 3/29/11. Patent No. 152477
5707-16200	Enhancing Security of a System Via Access by an Embedded Controller to A Secure Storage Device	04/10/2007	11/733,599	12/31/2009	US-2009-0327678-A1	03/29/2011	7,917,741 MSW Foreign counterparts filed in TW and CN. (See 16201 and 16202)

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-16201 TW	Enhancing Security of a System Via Access by an Embedded Controller to A Secure Storage Device	04/10/2008	097113121	02/16/2009	200907740		MSW Request for exam filed. Awaiting action.
5707-16202 CN	Enhancing Security of a System Via Access by an Embedded Controller to A Secure Storage Device	04/10/2008	200810091902.5	02/25/2009	101373437		MSW Request for exam filed. Awaiting action.
5707-16400	Firmware ROM Patch Method	01/31/2007	11/669,776	07/31/2008	U.S.-2008-0184072-A1		TAK Foreign counterpart filed in TW. (See 16401) Response to Office Action due 4/24/12.
5707-16401 TW	Firmware ROM Patch Method	01/31/2008	097103810	12/01/2008	200846897		TAK Examination deadline 1/31/11
5707-16500	Delta-Sigma Modulator For A Fan Driver	02/29/2008	12/040,554	09/03/2009	US-2009-0220219-A1	01/04/2011	7,863,849 TAK Foreign counterpart filed in Taiwan (See 16501)
5707-16501 TW	Delta-Sigma Modulator For A Fan Driver	02/28/2009		12/16/2009	200952320		TAK Request for exam filed.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-16600	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System (Provisional)	04/10/2007	60/910,863				MSW
5707-16601	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System	12/18/2007	11/958,601	10/16/2008	US-2008-0256374A-1	04/19/2011	7,930,576 MSW
5707-16602 TW	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System	04/10/2008	097113118	02/16/2009	200907690		MSW Request for exam filed. Awaiting action.
5707-16603 CN	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System	04/10/2008	200810091901.0	05/27/2009	101441607		MSW Response to Office Action filed.
5707-16700	Automatic System Clock Detection System (Provisional)	02/12/2007	60/889,431				TAK. Foreign filing not pursued.
5707-16701	Automatic System Clock Detection System	11/14/2007	11/939,670	08/14/2008	US-2008-0191756-A1	12/01/2009	TAK 7,626,436 3.5 Yr. Maint. Fee due 6/01/13. Letters Patent received 12/04/09. Foreign filing not pursued.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-17400	Level Shifter with Memory Interfacing Two Supply Domains	02/26/2008	12/037,639	08/27/2009	US-2009-0212842-A1	11/24/2009	TAK 7,622,954 3.5 Yr. Maint. Fee due 5/24/13. Foreign filing not pursued.
5707-17500	Memory Protection For Embedded Controllers	08/31/2007	11/848,808	03/05/2009	US-2009-0063799-A1	03/29/2011	7,917,716 MSW Foreign counterpart filed in TW. (See 17501) Allowed. Issue Fee paid 2/22/11.
5707-17501 TW	Memory Protection For Embedded Controllers	08/31/2008	097133504	09/01/2008			MSW Request for exam filed. Awaiting action.
5707-17900	Method for Physical Device (PHY) Support of the USB2.0 Link Power Management Addendum Using a ULPI PHY Interface Standard (Provisional)	06/19/2007	60/945,015				TAK Foreign counterparts filed in Taiwan and PCT. (See 17902 and 17903)

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-17901	Method for Physical Device (PHY) Support of the USB2.0 Link Power Management Addendum Using a ULPI PHY Interface Standard	06/18/2008	12/141,445	12/25/2008	US-2008-0320202-A1	07/20/2010	7,761,645 Foreign counterparts filed in Taiwan and PCT. (See 17902 and 17903). 3.5 Yr Maintenance Fee Due 1/20/14.
5707-17902 TW	Method for Physical Device (PHY) Support of the USB2.0 Link Power Management Addendum Using a ULPI PHY Interface Standard	06/19/2008	097122899	06/19/2008			TAK Request for exam filed. Awaiting action.
5707-17903 PCT	Method for Physical Device (PHY) Support of the USB2.0 Link Power Management Addendum Using a ULPI PHY Interface Standard	06/19/2008	PCT/US08/67536	12/24/2008	WO 2008/157718		TAK 30-month national phase entry due **12/19/09**.
5707-17904 KR	Method for Physical Device (PHY) Support of the USB2.0 Link Power Management Addendum Using a ULPI PHY Interface Standard	01/19/2010	10-2010-7001272				Application filed.
5707-18100	Rate Adaptation for Support of Full-Speed USB Transactions Over a High-Speed USB Interface	08/28/2007	11/846,066	03/05/2009	US-2009-0063717-A1		TAK Foreign counterpart filed in Taiwan. (See 18101) Response to Office Action filed 3/23/12.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-18101 TW	Rate Adaptation for Support of Full-Speed USB Transactions Over a High-Speed USB Interface	08/28/2008	097132946	04/16/2009	200917048		TAK Request for exam filed. Awaiting action.
5707-18200	Configurable Signature for Authenticating Data or Program Code	08/31/2007	11/848,854	03/05/2009	US:-2009-0063865-A1	08/23/2011	8,006,095 Foreign filing not pursued.
5707-18500	Providing a High-Speed Connection Between a Memory Medium of a Mobile Device and an External Device	11/16/2007	11/941,115	05/21/2009	US-2009-0131036-A1	07/26/2011	7,986,962 Foreign counterpart filed in Taiwan. (See 18501)
5707-18501 TW	Providing a High-Speed Connection Between a Memory Medium of a Mobile Device and an External Device	11/14/2008	097144248				JLS Publication on 9/16/2009 Request for Exam due 11/14/11.
5707-18502	Providing a Connection Between a Memory Medium of a Mobile Device and an External Device (CIP of 5707-18500)	10/30/2009	12/609,714			4/3/2012	8,150.452 JLS 3.5 Yr. Maint. Fee due 10/3/15.
5707-18600	RPM Controller Using Drive Profiles	02/26/2009	12/393,571	8/26/2010	US-2010-0215510-A1		TAK Response to Office Action due 2/14/12.
5707-18601 TW	RPM Controller Using Drive Profiles	02/25/2010	099105471				Cn specification rec'd. Req for Exam filed.
5707-18700	Detecting Closure of an Electronic Device Using Capacitive Sensors (Provisional)	08/31/2007	60/969,329				JLS Filing receipt dated 09/13/07 received.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-18701	Detecting Closure of an Electronic Device Using Capacitive Sensors	10/11/2007	11/870,529	03/05/2009	US-2009-0058429-A1	4/3/2012	8,149,000 JLS 3.5 Yr. Maint. Fee due 10/3/15.
5707-18702 TW	Detecting Closure of an Electronic Device Using Capacitive Sensors	09/01/2008	097133503	05/16/2009	200921336		JLS Request for exam filed. Awaiting action.
5707-19200	Metal or Via Programmable Element	02/20/09	12/389,568	08/26/2010	US-2010-0213515-A1	4/10/2012	8,154,053 TAK 3.5 Yr. Maint. Fee due 10/10/15.
5707-19201 TW	Metal or Via Programmable Element	02/22/2010					Cn specification rec'd.
5707-19400	External Direct Memory Access of Embedded Controller Memory	08/05/2008	12/186,373	02/11/2010	US-2010-0036979-A1	07/12/2011	7,979, 601 JLS Foreign filing due 8/5/09; client instructed via email to file in Taiwan only. 2011-09-16 Request for Certificate of Correction filed with USPTO.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-19401 TW	External Direct Memory Access of Embedded Controller Memory	08/05/2009	TBA	04/01/2010	201013408		JLS Request for examination filed. Priority docs filed
5707-19500	Method for Improving Power-Supply Rejection	01/14/2009	12/353,843			03/15/2011	7,907,003 TAK
5707-19501 TW	Method for Improving Power-Supply Rejection	12/02/2009	098141195	08/01/2010	201028814		Application filed. Request for Exam filed 12/2/09.
5707-19600	Structured Virtual Registers for Embedded Controller Devices	02/20/2009	12/389,791	08/26/2010	US-2010-0217957-A1	02/21/2012	Pat No. 8,122,205 Alex Courtade Allowed. Issue Fee filed 1/19/12.
5707-19601	Structured Virtual Registers for Embedded Controller Devices	02/22/2010	099105033	10/01/2010	201035758		Filing Receipt received 4/23/10. Req for Exam filed. Cn specification rec'd.
5707-19700	Direct Slave-to-Slave Data Transfer on a Master-Slave Bus	02/02/2009	12/364,175	08/05/2010	US-2010-0199007-A1	4/10/2012	8,156,274 EAH 3.5 Yr. Maint. Fee due 10/10/15.
5707-19701	Direct Slave-to-Slave Data Transfer on a Master-Slave Bus (TW)	12/02/2009	098141198	08/16/2010	201030525		Filing procedure completed. Request for Exam filed.
5707-19800	USB-I2C Bridge for Soft OSD and FW Upgrade in LCD Displays (Provisional)	02/28/2008	61/032,291				Foreign counterpart filed in Taiwan. (See 19802)

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-19801	Updating Firmware in a Display Device Using a Serial Bus	02/17/2009	12/372,402	09/03/2009	US-2009-0222807-A1		JLS Filing receipt dated 03/06/09 received.
5707-19802 TW	Updating Firmware in a Display Device Using a Serial Bus	02/28/2009	098106515				Examination request filed 10/12/2009
5707-20400	Fast Common Mode Feedback Control for Differential Driver	02/24/2009	12/391,414	08/26/2010	US-2010-0213985-A1	03/15/2011	7,906,994 SH Foreign filing due 2/24/10.
5707-20401 PCT	Fast Common Mode Feedback Control for Differential Driver	02/24/2010	PCT/US2010/25208	09/02/2010	WO 2010/099183		Notice Concerning Submission of Priority Document dated 3/26/10 received.
5707-20402 CN	Fast Common Mode Feedback Control for Differential Driver						
5707-20403 EP	Fast Common Mode Feedback Control for Differential Driver	09/19/2011	10708666.2				Ann Due 2/24/12
5707-20404 JP	Fast Common Mode Feedback Control for Differential Driver	08/24/2011	2011-552125				
5707-20405 KR	Fast Common Mode Feedback Control for Differential Driver	08/24/2011	10-2011-7019688				
5707-20500	Frequency Compensation Scheme for Stabilizing the LDO using External NPN in HV Domain	02/20/2009	12/389,581	08/26/2010	US-2010-0213917-A1	02/22/2011	7,893,670 TAK

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-20501 DE	Frequency Compensation Scheme for Stabilizing the LDO using External NPN in HV Domain	02/22/2010	10 2010 000 498.7				Annuity due 6/30/11
5707-20700	Adaptive Capacitive Sensing (Provisional)	06/27/2008	61/076,482				TAK 06/08/08 Proceed per MK. Awaiting first office action from USPTO.
5707-20702 TW	Adaptive Capacitive Sensing	05/08/2009	098115458	02/16/2010	201007176		TAK Examination deadline 5/8/12
5707-20703 PCT	Adaptive Capacitive Sensing	04/29/2009	PCT/US09/42115	republished on 10/07/2010	WO 2009/158065		TAK 30-month national phase entry deadline 12/27/10. Article 19 amendments due 10/25/10 and Response to Written Opinion due 11/25/10.
5707-20800	Temperature and Supply Independent CMOS Current Source	02/10/2009	12/368,378	08/12/2010	2010-0201406	05/17/2011	7,944.271
5707-21000	USB and Ethernet Controller Combination Device (Provisional)	08/08/2008	61/087,242				TAK Filing receipt dated 08/22/08 received. Foreign filing due 8/8/09; client instructed via email to file PCT and in Taiwan.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-21001	USB and Ethernet Controller Combination Device	02/11/2009	12/369,571	02/11/2010	US-2010-0036992-A1	10/18/2011	8,041,874 TAK 12/09/08 MK authorized us to proceed.
5707-21002 TW	USB and Ethernet Controller Combination Device	08/10/2009	TBA	04/16/2010	201015917		TAK Request for examination filed. Priority docs filed 11/3/2009 Waiting for first office action.
5707-21003 PCT	USB and Ethernet Controller Combination Device	07/31/2009	PCT/US09/52424	02/11/2010	WO 2010/017107		TAK National filing deadline 2/8/11
5707-21004 CN	USB and Ethernet Controller Combination Device						TAK
5707-21005 EP	USB and Ethernet Controller Combination Device						TAK
5707-21006 JP	USB and Ethernet Controller Combination Device						TAK
5707-21007 KR	USB and Ethernet Controller Combination Device						TAK
5707-21008 SG	USB and Ethernet Controller Combination Device						TAK

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-21200	Utilization of Mock USB Device Controller to Obtain USB Bus Power Compliance	02/20/2009	12/389,538	08/26/2010	US-2010-0217911-A1	02/01/2011	7,882,297 Request for Certificate of Correction filed 3/28/11.
5707-21201 TW	Utilization of Mock USB Device Controller to Obtain USB Bus Power Compliance	02/22/2010	099105035	10/16/2010	201037508		Filing Receipt received 4/23/10. Req for Exam filed. Cn specification rec'd.
5707-21300	Single Pin Port Power Control	01/27/2009	12/360,760	04/29/2010	US-2010-0191984-A1	4/10/2012	8,156,352 EAH 3.5 Yr. Maint. Fee due 10/10/15.
5707-21301 TW	Single Pin Port Power Control	12/02/2009	098141196	10/16/2010	201037522		Application filed. Request for Exam filed 12/2/09.
5707-21302	Using a Single Terminal for a Power Enable Output Signal and Detecting an Over-Current Condition (Continuation of 5707-21300)	12/09/2011	13/315,868				JLS
5707-21400	Power-up Control for Very Low-Power Systems	02/13/2009	12/371,375	08/19/2010	US-2010-0207596-A1	4/10/2012	8,154,270 TAK 3.5 Yr. Maint. Fee due 10/10/15.
5707-21401 TW	Power-up Control for Very Low-Power Systems	02/06/2010	099103675	11/16/2010	201041307		CN Specification received.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-21500	Low Cost Fingerprint Sensor System (Provisional)	08/15/2008	61/089,259				SJC Filing receipt dated 08/27/08 received. Foreign filing due 8/15/09; file in Taiwan only per client's email of 6/23/09
5707-21501	Low Cost Fingerprint Sensor System	01/23/2009	12/359,056	02/18/2010	US-2010-0039121-A1	4/3/2012	8,149,001 SJC File in Taiwan only per client's email of 6/23/09. 3.5 Yr. Maint. Fee due 10/3/15.
5707-21502 TW	Low Cost Fingerprint Sensor System			03/16/2010	201011660		SJC
5707-21600	Sensor-less, Brushless, Three Phase Motor Drive (Provisional)	10/24/2008	61/108,320				09/09/08 On hold per MK. 10/23/08 MK instructed us to file ASAP. Foreign filing due **10/24/09.** Client instructions of 9/08/09 file in Taiwan.
5707-21601	Brushless, Three Phase Motor Drive	02/26/2009	12/393,996	04/29/2010	US-2010-0102766-A1	11/08/2011	8,054,033
5707-21602	Brushless, Three Phase Motor Drive (TW)						Received Chinese specification as filed.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-21603	Brushless Three Phase Motor Drive Control based on a Delta Zero Crossing Error (Continuation of 5707-21601)	09/28/2011	13/246,973		US-2012-0013280-A1	01/19/2012	BPLS
5707-21700	USB Port Overvoltage Protection (Provisional)	09/19/2008	61/098,561				SH Foreign filing due **09/26/09**
5707-21701	USB Port Overvoltage Protection	02/02/2009	12/364,144	03/25/2010	US-2010-073837-A1		SH 12/09/08 MK authorized us to proceed. Response to Office Action filed 1/11/12.
5707-21702	USB Port Overvoltage Protection	09/18/2009	098131678	06/01/2010	201021344		SH Request for Exam filed 10/26/2009.
5707-21900	Reporting a Faulty Charging Device	01/27/2009	12/360,245	07/29/2010	US-2010-0188237-A1	03/06/2012	8,130,110
5707-21901 TW	Reporting a Faulty Charging Device	12/02/2009	098141194	08/16/2010	201030512		Filing procedure completed. Request for Exam filed.
5707-22000	Power-up Control for Very Low-Power Systems	02/06/2009	12/367,242	08/12/2010	US-2010-0201410-A1	05/31/2011	7,952,402
5707-22001 DE	Power-up Control for Very Low-Power Systems	02/05/2010	10 2010 000 318.2	11/04/2010	102010000318.2		Request for Exam filed. Revised German translation received.
5707-22100	Bistone Port Power Controller for USB Hubs with Legacy Battery Charge Support	02/06/2009	12/367,009	08/12/2010	US-2010-0205463-A1	11/08/2011	8,055,919

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-22101 TW	Port Power Controller for USB Hubs with Legacy Battery Charge Support	02/06/2010	099103676	10/01/2010	201035727		Chinese specification received.
5707-22600	System and Method for Inducing Rotation of a Rotor in a Sensorless Motor	11/18/2009	12/620,656	05/19/2011	US-20 11-0115421-A 1		BPLS Filing Receipt dated 12/04/09 received. 2009-06-02 On hold per Mark Koffsky. Authorized to proceed on 9/1/09; should be completed by 11/30/09.
5707-22601	System and Method for Inducing Rotation of a Rotor in a Sensorless Motor	11/18/2010	099139806				
5707-22700	System and Method for Aligning a Rotor to a Known Position	11/18/2009	12/620,679	05/19/2011	US-20 11-0115419-A 1		BPLS 2009-06-02 On hold per Mark Koffsky. Authorized to proceed on 9/1/09; should be completed by 11/30/09.
5707-22701	System and Method for Aligning a Rotor to a Known Position	11/18/2010	099139763				
5707-22800	Brushless, Three Phase Motor Drive	11/18/2009	12/620,726	05/19/2011	US-20 11-0115423-A 1		BPLS 2010-11-16 Preliminary Amendment filed.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-22801	Brushless, Three Phase Motor Drive	11/18/2010	099139801				
5707-22900	Generating a Nonlinear Function for Fan Control	05/27/2010	12/788,590	12/01/2011	US-2011-0295442-A1		JLS 2009-06-02 On hold per Mark Koffsky. 2010-04-14 Mark Koffsky authorized us to proceed.
5707-22901 TW	Generating a Nonlinear Function for Fan Control						JLS
5707-23200	Drive Method to Minimize Vibration and Acoustics in Three Phase Brushless DC (TPDC) Motors (Provisional)	06/12/2009	61/186,623				TAK Foreign filing deadline 06/12/10.
5707-23201	Drive Method to Minimize Vibration and Acoustics in Three Phase Brushless DC (TPDC) Motors	12/07/2009	12/632,495	12/16/2010	US-2010-0315029-A1		TAK
5707-23202 TW	Drive Method to Minimize Vibration and Acoustics in Three Phase Brushless DC (TPDC) Motors	06/03/2010	099117983				Filed. Req for Exam filed. CN specification rec'd 10/15/10.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-23300	Driver Output Slope Control	Closed					BPLS 2009-08-03 On hold per Mark Koffsky. Authorized to proceed on 9/1/09; should be completed by 11/30/09. 2009-11-24 We are recommending not pursuing.
5707-23400	Analog-to-Digital Converter in a Motor Control Device	11/30/2009	12/627,734	06/02/2011	US-2011-0128085-A1		BPLS Response to Office Action filed 12/27/11. Response to Final Action filed 3/30/12. Notice of Appeal due 4/24/12.
5707-23401 TW	Analog-to-Digital Converter in a Motor Control Device	11/30/2010	099141608				
5707-23500	Bi-Directional High Side Current Sense Measurement	05/27/2010	12/788,896	12/01/2011	US-2011-0291675-A 1		MKB 2009-08-20 On hold per Mark Koffsky. 2010-04-14 Mark Koffsky authorized us to proceed.
5707-23501 TW	Bi-Directional High Side Current Sense Measurement						MKB

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5707-23600	Driver with Accurately Controlled Slew Rate and Limited Current	05/27/2010	12/789,005	12/01/2011	US-2011-0291707-A1		MKB 2009-08-26 On hold per Mark Koffsky. 2010-04-14 Mark Koffsky authorized us to proceed. Response to Notice to File Corrected Application Papers filed 6/21/10.
5707-23601 WO	Driver with Accurately Controlled Slew Rate and Limited Current	05/06/2011	PCT/US11/354				MKB
5707-23900	Improved Method for Aligning and Starting a BLDC Three Phase Motor	05/28/2010	12/790,161	12/01/2011	US-2011-0291597-A1		TYE 2009-10-29 On hold per Mark Koffsky. 2010-04-14 Mark Koffsky authorized us to proceed.
5707-24000	Low Power Regulator (Provisional)	05/26/2010	61/348,587				TAK 2009-10-29 On hold per Mark Koffsky. 2010-04-14 Mark Koffsky authorized us to proceed.
5707-24001	Low Power Regulator	05/18/2011	13/110,317	12/01/2011	US-2011-0291625-A1		TAK
5707-24002 TW	Low Power Regulator (TW)						
5707-24300	USB Hub Supporting High Speed and Super Speed Devices (Provisional)	01/19/2010	61/296,338				JLS

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5707-24301	USB Hub Apparatus Supporting Multiple High Speed Devices and a Single Super Speed Device	05/27/2010	12/788,385	07/21/2011	US-2011-0179201-A1	3/13/12	8,135,883
5707-24302 PCT	USB Hub Apparatus Supporting Multiple High Speed Devices and a Single Super Speed Device	12/20/2010	PCT/US10/61281				
5707-24303 TW	USB Hub Apparatus Supporting Multiple High Speed Devices and a Single Super Speed Device						
5707-24400	USB to SDIO Bridge (Provisional)	02/01/2010	61/300,350				
5707-24401	USB to SD Bridge	05/26/2010	12/787,730	08/04/2011	US-2011-0191499-A1		JLS 2010-04-14 Mark Koffsky authorized us to proceed. Response to Final Office Action due **3/14/12**.
5707-24402 TW	USB to SD Bridge						
5707-24500	Firmware Flashing of Portable Device Using A Serial Bus Hub (Provisional)	03/12/2010	61/313,350				MSW

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-24501	Firmware Flashing of Portable Device Using A Serial Bus Hub	04/22/2010	12/765,233	09/15/2011	US-2011-1225349-A1		MSW Filing Receipt dated 5/4/10 received.
5707-24600	Sharing Non-Sharable Elements Between an Embedded Controller and A Processor in a Computer System (CIP of 5707-16601)						MSW
5707-24700	Driving Low Voltage Brushless Direct Current (BLDC) Three Phase Motors from Higher Voltage Sources	08/31/2010	12/872,834	3/01/2012	US-2012-0049776-A1		TAK
5707-24800	Improved Natural Commutation for Three Phase Brushless Direct Current (BLDC) Motors	09/1/2010	12/874,187	3/01/2012	US-2012-0049777-A1		TAK
5707-25300	Display Port Docking Mechanism (Provisional)	09/10/2010	61/381,698				MSW
5707-25301	Monitor Chaining and Docking Mechanism	09/1/2011	13/223,730	3/15/2012	US-2012-0062800-A1		MSW Response to Missing Parts filed 9/29/11.
5707-25302	Display Port Docking Mechanism (PCT)	09/1/2011	PCT/US11/50208				

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5707-25303	Display Port Docking Mechanism	09/09/2011	100132691				
5707-25400	Geometrically Based Button Discrimination in Capacitive Sensing Applications	03/17/2011	13/049,932				BLPS
5707-25500	High Speed USB Hub with Full Speed to High Speed Transaction Translator	07/07/2011	13/177,591				JLS Response to Office Action due 6/29/12.
5707-25700	MAC Filtering on Ethernet PHY for Wake-on-LAN	02/11/2011	13/025,818				TAK Response to Missing Parts filed 3/4/11.
5707-25701	MAC Filtering on Ethernet PHY for Wake-on-LAN	01/20/2012	PCT/US12/21992				TAK
5707-25702	MAC Filtering on Ethernet PHY for Wake-on-LAN						TAK
5707-25900	Adjusting Delivery of Current in a Connection Based on Temperature	05/17/2011	13/109,446				JLS

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
5707-26000	USB Switch Which Allows Primary USB Connection Upon USB Signaling	05/31/2011	13/149,184				JLS Response to Restriction Requirement filed 2/28/12.
5707-26200 Patent Litigation	Reexam of USPN 7,930,576	06/21/211	90/011,754				AMP Response to Office Action due 4/23/12.

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File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-00401 U.S. (formerly 42133-0018)	Directly Tuned Filter and Method of Directly Tuning a Filter	09/17/2002	10/244,558			01/03/2006	6,983,136 7/3/2013 2nd Maint Fee Due 7/3/2017 3rd Maint Fee Due
6428-00500 U.S. (formerly 42133-0024)	Frequency Synchronization	06/01/2007	11/809,796			05/04/2010	7,711,078 11/4/2013 1st Maint Fee Due 11/4/2017 2nd Maint Fee Due 11/4/2021 3rd Maint Fee Due
6428-00501 Canada (formerly 42133-0056)	Frequency Synchronization	05/29/2008	2,689,300				5/29/2011 Annuity Due 5/29/2013 Request Exam/5 Yrs
6428-00503 Europe (formerly 42133-0055)	Frequency Synchronization	05/29/2008	08 757 163.4				Published 5/29/2012 Annuity Due
6428-00504 Japan (formerly 42133-0058)	Frequency Synchronization	05/29/2008	2010-509646				Pending

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-00505 South Korea (formerly 42133-0059)	Frequency Synchronization	05/29/2008	2009-7027490				Pending 5/29/2013 Request Examination
6428-00600 U.S. (formerly 42133-0011)	High Quality, Low Power, Wireless Audio System	02/25/2005	11/065,995			06/02/2009	7,542,794 12/2/2012 1st Maint Fee Due 12/2/2016 2nd Maint Fee Due 12/2/2020 3rd Maint Fee Due
6428-00602 China (formerly 42133-0032)	High Quality, Low Power, Wireless Audio System	02/22/2006	200680009682.6				Published
6428-00603 Europe (formerly 42133-0031)	High Quality, Low Power, Wireless Audio System	02/22/2006	06705208.4				Pending 2/22/2012 Annuity Due
6428-00604 Japan (formerly 42133-0034)	High Quality, Low Power, Wireless Audio System	02/22/2006	2007-556469			08/12/2011	Patent no. 4797123
6428-00605 South Korea (formerly 42133-0033)	High Quality, Low Power, Wireless Audio System	02/22/2006	2007-7021655				Pending
6428-00700 Canada (formerly 42133-0012)	Injection Locking Using Direct Digital Tuning	08/11/2003	2,493,942				Pending 8/11/2011 Annuity Due

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-00701 China (formerly 42133-0015)	Injection Locking Using Direct Digital Tuning	08/11/2003	03818996.8			08/19/2009	ZI 03818996.8 8/11/2011 Annuity Due 8/19/2012
6428-00702 Germany (formerly 42133-0041)	Injection Locking Using Direct Digital Tuning	08/11/2003	03783879.4			10/03/2007	60316695.4 8/11/2011 Annuity Due
6428-00703 Europe (formerly 42133-0013)	Injection Locking Using Direct Digital Tuning	08/11/2003	03783879.4			10/03/2007	1535395 Issued
6428-00708 Japan (formerly 42133-0014)	Injection Locking Using Direct Digital Tuning	08/11/2003	2004-526550			10/02/2009	4384036 10/2/2012 Annuity Due
6428-00709 South Korea (formerly 42133-0016)	Injection Locking Using Direct Digital Tuning	08/11/2003	2005-7002218				Pending
6428-00711 U.S. (formerly 42133-0005)	Injection Locking Using Direct Digital Tuning	08/11/2003	10/639,543			11/08/2005	6,963,249 5/8/2013 2nd Maint Fee Due 5/8/2017 3rd Maint Fee Due
6428-00802 U.S. (formerly 42133-0001)	Signal Sampling Method and Circuit for Improved Hold Mode Isolation	08/12/2003	10/639,544			12/28/2004	6,836,158 6/28/2012 2nd Maint Fee Due 6/28/2016 3rd Maint Fee Due

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-00903 U.S. (formerly 42133-0019)	Power Down System And Method For Integrated Circuits	07/28/2003	10/629,138			03/29/2005	6,873,215 9/29/2012 2nd Maint Fee Due 9/29/2016 3rd Maint Fee Due
6428-01000 U.S. (formerly 42133-0023)	RF-to-Baseband Receiver Architecture	03/13/2006	11/374,571			05/26/2009	7,539,476 11/26/2012 1st Maint Fee Due 11/26/2016 2nd Maint Fee Due 11/26/2020 3rd Maint Fee Due
6428-01001 Canada (formerly 42133-0049)	RF-to-Baseband Receiver Architecture	02/22/2007	2,643,096			01/25/2011	2,643,096 2/22/2012 Annuity Due
6428-01002 China (formerly 42133-0051)	RF-to-Baseband Receiver Architecture	02/22/2007	200780009247.8				Published
6428-01003 Europe (formerly 42133-0050)	RF-to-Baseband Receiver Architecture	02/22/2007	07 701 817.4				Published 2/22/2012 Annuity Due
6428-01004 Japan (formerly 42133-0053)	RF-to-Baseband Receiver Architecture	02/22/2007	2008-55897				Published
6428-01005 South Korea (formerly 42133-0052)	RF-to-Baseband Receiver Architecture	02/22/2007	2008-7022280				2/22/2012 Request Examination

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-01100 U.S. (formerly 42133-0025)	Wireless Communications System and Channel-Switching Method	04/18/2008	12/106,098	10/22/2009	US 2009-0262709 A1		RCE and Response to Final Office Action filed 9/15/11.
6428-01101 Europe (formerly 42133-0063)	Wireless Communications System And Channel-Switching Method	04/16/2009	09732651.6				Published 4/16/2011 Annuity Due 7/5/2011 Examination Fee 7/5/2011 Record In Hong Kong
6428-01102 Japan (formerly 42133-0061)	Wireless Communications System And Channel-Switching Method	04/16/2009	2011-504292				4/16/2012 Request Examination
6428-01103 South Korea (formerly 42133-0062)	Wireless Communications System And Channel-Switching Method	04/16/2009	2010-7025852				4/16/2014 Request Examination
6428-01300	Reducing Spurs in Injection-Locked Oscillators	04/29/2011	13/097,671				TAK Response to Missing Parts filed 7/15/11.
6428-01400	Low-Power Class D Amplifier Using Multistate Analog Feedback Loops	04/29/2011	13/097,690				TAK Response to Missing Parts filed 8/15/11.
6428-01500	Transmit Power Control Algorithms for Sources and Sinks in a Multi-Link Session	04/29/2011	13/097,736				TAK Response to Missing Parts filed 7/13/11.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-01600	Reducing Power Consumption in Sink Devices by Having Sinks Receive Only Left Audio Channel or Right Audio Channel	04/29/2011	13/097,757				TAK Response to Missing Parts filed 7/13/11.
6428-02002 (formerly BCO-001B)	Multi-Portal Bridge for Providing Network Connectivity	02/16/2001	09/784,831	11/01/2001	US 2001-0037422 A1	08/03/2004	6,772,267 7.5 year maintenance fee due **2/3/12**.
6428-02003 (formerly BCO-001A)	Reference Time Distribution Over A Network	02/16/2001	09/785,598	09/27/2001	US 2001-0024455 A1	09/06/2011	8,014,423 3.5 year maintenance fee due **3/6/15**.
6428-02004 PCT (formerly BCO-001B PC)	Multi-Portal Bridge for Providing Network Connectivity (PCT)	02/16/2001	PCT/1B01/00433				
6428-02005 PCT (formerly BCO-001A PC)	Reference Time Distribution Over A Network (PCT)	02/16/2001	PCT/1B01/00368				
6428-02006 EP (formerly BCO-001A EP)	Reference Time Distribution Over A Network (EP)	02/16/2001	01910090.8			04/08/2009	1256197
6428-02007 FR (formerly BCO-001A FR)	Reference Time Distribution Over A Network (FR)	02/16/2001	01910090.8			04/08/2009	1256197

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-02008 DE (formerly BCO-001A DE)	Reference Time Distribution Over A Network (DE)	02/16/2001	01910090.8			04/08/2009	1256197
6428-02009 GB (formerly BCO-001A GB)	Reference Time Distribution Over A Network (GB)	02/16/2001	01910090.8			04/08/2009	1256197
6428-02010 EP (formerly BCO-001B EP)	Multi-Portal Bridge for Providing Network Connectivity (EP)	02/16/2001	01912070.8			09/05/2007	1256207
6428-02011 FR (formerly BCO-001B FR)	Multi-Portal Bridge for Providing Network Connectivity (FR)	02/16/2001	01912070.8			09/05/2007	1256207
6428-02012 DE (formerly BCO-001B DE)	Multi-Portal Bridge for Providing Network Connectivity (DE)	02/16/2001	01912070.8			09/05/2007	1256207
6428-02013 GB (formerly BCO-001B GB)	Multi-Portal Bridge for Providing Network Connectivity (GB)	02/16/2001	01912070.8			09/05/2007	1256207

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-02101 PCT (formerly BCO-002 PC)	Method for Synchronization in Networks (PCT)	10/25/2002	PCT/CH02/00580				
6428-02102 (formerly BCO-002)	Method for Synchronization in Networks	06/05/2003	10/496,367	02/10/2005	US 2005-0033862 A1	05/11/2010	7,716,375 3.5 year maintenance fee due **11/11/13**.
6428-02103 EP (formerly BCO-002 EP)	Method for Synchronization in Networks (EP)	10/25/2002	02774228.7			04/26/2006	1449317
6428-02104 DE (formerly BCO-002 DE)	Method for Synchronization in Networks (DE)	10/25/2002	02774228.7			04/26/2006	1449317
6428-02105 GB (formerly BCO-002 GB)	Method for Synchronization in Networks (GB)	10/25/2002	02774228.7			04/26/2006	1449317
6428-02106 (formerly BCO-002 C1)	Method for Synchronization in Networks	03/26/2010	12/732,654	04/21/2011	US 2011-0090925 A1		Awaiting First Office Action from the USPTO.
6428-02201 PCT (formerly BCO-003 PC)	Digitally-Controlled Oscillator (PCT)	06/23/2003	PCT/CH03/00405				

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-02202 (formerly BCO-003)	Digitally-Controlled Oscillator	07/21/2005	10/518,874	03/16/2006	US 2006-0055471 A1	11/07/2006	7,132,895 7.5 year maintenance fee due 5/7/14.
6428-02203 EP (formerly BCO-003 EP)	Digitally-Controlled Oscillator (EP)	06/23/2003	03729767.8			06/23/2012	1525662
6428-02204 DE	Digitally-Controlled Oscillator (DE)	06/23/2003	03729767.8			06/23/2012	1525662
6428-02205 FR	Digitally-Controlled Oscillator (FR)	06/23/2003	03729767.8			06/23/2012	1525662
6428-02206 GB	Digitally-Controlled Oscillator (GB)	06/23/2003	03729767.8			06/23/2012	1525662
6428-02301 PCT (formerly BCO-004 PC)	Processor with Different Types of Control Units for Jointly Used Resources (PCT)	03/01/2004	PCT/CH04/000106				
6428-02302 EP (formerly BCO-004 EP)	Processor with Different Types of Control Units for Jointly Used Resources (EP)	03/01/2004	04715865.4			02/18/2009	1599794
6428-02303 DE (formerly BCO-004 DE)	Processor with Different Types of Control Units for Jointly Used Resources (DE)	03/01/2004	04715865.4			02/18/2009	1599794

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-02304 FR (formerly BCO-004 FR)	Processor with Different Types of Control Units for Jointly Used Resources (FR)	03/1/2004	04715865.4			02/18/2009	1599794
6428-02305 GB (formerly BCO-004 GB)	Processor with Different Types of Control Units for Jointly Used Resources (GB)	03/1/2004	04715865.4			02/18/2009	1599794
6428-02501 (formerly BCO-006)	Very-Long Instruction Word Architecture with Multiple Processing Units	09/08/2009	12/555,146	04/01/2010	US 2010-0082947 A1		Awaiting First Office Action from USPTO.
6428-02502 PCT (formerly BCO-006 PC)	Very-Long Instruction Word Architecture with Multiple Data Queues (PCT)	09/08/2009	PCT/IB09/06886				
6428-02503 EP (formerly BCO-006 EP)	Very-Long Instruction Word Architecture with Multiple Data Queues (EP)	09/08/2009	09747916.6				
6428-02801 (formerly BCO-009)	Profile for Media/Audio User Preferences Database	03/31/2011	13/076,661				Awaiting First Office Action from USPTO.
6428-02802 PCT (formerly BCO-009 PC)	Profile for Media/Audio User Preferences Database (PCT)	03/31/2011	PCT/US11/30657				

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-02901 (formerly BCO-010)	Methods and Systems for Wi-Fi Setup Configuration	05/02/2011	13/098,779	11/24/2011	US-2011-0289229-A1		Response to Missing Parts filed 8/5/11. Assigned directly to SMSC Holdings S.à r.l.
6428-02902 PCT (formerly BCO-010 PC)	Methods and Systems for Wi-Fi Setup Configuration (PCT)	05/2/2011	PCT/US11/034775				
6428-03001 (formerly BCO-011)	Systems and Methods for Operating Media Devices	05/12/2011	13/106,135	12/15/2011	US-2011-0304443-A1		Response to Missing Parts filed 8/25/11. Assigned directly to SMSC Holdings S.à r.l
6428-03002 PCT (formerly BCO-011 PC)	Systems and Methods for Operating Media Devices (PCT)	05/12/2011	PCT/US11/036219	11/17/2011	2011143403		
6428-03100 (formerly BCO-012 PR)	Seamless Transfer of Media Streams (Provisional)	05/27/2010	61/348,927				
6428-03101 (formerly BCO-012)	Seamless Transfer of Media Streams	05/26/2011	13/116,369	12/01/2011	US-2011-0295974-A1		Response to Missing Parts filed 8/15/11. Assigned directly to SMSC Holdings S.à r.l
6428-03102 PCT (formerly BCO-012 PC)	Seamless Transfer of Media Streams (PCT)	05/26/2011	PCT/US11/038137				

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-03400	Gesturing Architecture Using Proximity Sensing	12/22/2011	13/334,477				BPLS Response to NFCAP filed 1/20/12.
6428-03500	Overcoming Limited Common-Mode Range for USB Systems	01/25/2012	13/357,987				TAK
6428-03700	Alignment of Optical Sensors (Provisional)	09/16/2011	61/535,817				
6428-03701	Optimized Alignment of Optical Sensors	02/28/2012	13/406,629				
6428-03800	Device Charging Over USB Using a Plurality of Handshakes	10/31/2011	13/285,202				
6428-03900	Enhancing Security of Sensor Data for a System Via an Embedded Controller (Provisional)	3/19/2012	61/612,875				MSW
6428-03900	Enhancing Security of Sensor Data for a System Via an Embedded Controller						MSW
6428-04201	Resistive Touch Panel with Improved Termination (Provisional)	01/17/2012	61/587,446				
6428-04202	Resistive Touch Panel with Improved Termination						BPLS 2011-01-18 Client instructed us to base utility filing date off of 6428-04200. Must be filed before 9/6/12. 2012-01-25 Mark Koffsky asked us to wait to prepare.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6428-04600	Serial Peripheral Interface Between a Plurality of Integrated Circuits within a Single Fiber Optic Receive/Transmit Housing	02/28/2012	13/406,721				~~Must be filed before 9/16/12.~~
6428-04700	Optical Power Information Passed between two Integrated Circuits within a Single Fiber Optic Receive/Transmit	02/28/2012	13/406,785				~~Must be filed before 9/16/12.~~
6428-04900	Method and Apparatus for Port Power Switch Based Lead Compensation	02/28/2012	13/407,153				TAK
6428-05000	Method for Detecting Type of the Device Connected to the USB Charging Port	03/06/2012	13/413,146				BPLS Needs Chinese foreign filing license-done ~~Target filing date is 2/15/12.~~
6534-00200 (formerly 70596.3 (M-17481US))	Methods and Systems For Interfacing Bus Powered Devices With Host Devices Providing Limited Power Levels	11/6/2008	12/266,335				Allowed. Issue Fee due **4/24/12**.
6534-00300 (formerly 70596.4 (M-17508US))	Device Identification Using Frequency Modulated Signal Bursts	1/28/2009	12/360,984				Response to Final Office Action filed 8/16/11.
6534-00400 (formerly 70596.5 (M-17511US))	Shared Buffer For Data Communications Routed Through Hub	10/2/2009	12/573,019				Waiting for Office Action.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6534-00500 (formerly 70596.7 (M-17544US))	Multi-Port Device With Controller For Storage Media Device Port	6/24/2010	12/822,956				Response to Office Action ~~due 2/23/12~~; response filed 2/23/12.
6534-00700 (formerly 70596.9)	Sample Time Correction For Multiphase Clocks	4/13/2010	12/759,574				Waiting for Office Action.
6534-00800 (formerly 70596.10)	Fingerprint Sensor and Interface	8/2/2007	11/832,763			7/12/11	7,978,884
6534-00900 (formerly 70596.11)	Fingerprint Sensor and Method of Transmitting a Sensor Image To Reduce Data Size And Data Rate	8/12/2007	11/837,532			3/29/11	7,916,908
6534-01000 (formerly 70596.12)	Clocking Scheme For Bridge System	2/2/2010	12/698,752				Waiting for Office Action.
6534-01100 (formerly 70596.13)	High Frequency And Idle Communication Signal State Detection	3/10/2010	12/721,333				Waiting for Office Action.
6534-01200 (formerly 70596.14)	Low Frequency Communication Signal State Detection	3/10/2010	12/721,365				Waiting for Office Action.
6534-01300 (formerly 70596.15)	Detection System and Methods	3/10/2010	12/721,268				Waiting for Office Action.
6534-01400 (formerly 70596.16)	High Speed Low Power Cell Providing Serial Differential Signals	3/10/2010	12/721,418			8/2/2011	7,990,296

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6534-01500 (formerly 70596.17)	Efficient Data Transfers Over Serial Data Streams	9/1/2010	12/874,070				Response to Office Action filed 1/19/12.
6534-01600 (formerly 70596.18)	Systems and Methods For Locking An Oscillator To An Incoming Data Signal	3/10/2010	12/721,432				Waiting for Office Action.
6534-01700 (formerly 70596.19)	Clock Signal Generation For A Plurality Of Communication Ports Using A Single Reference Clock	3/10/2010	12/721,447				Waiting for Office Action.
6534-01800 (formerly 70596.20)	Methods and Systems For Performing Serial Data Communication (Provisional)	6/11/2010	61/354,035				Foreign filing deadline **6/11/11**.
6534-01801	Methods and Systems For Performing Serial Data Communication	5/31/2011	13/149,103	12/22/2011	US-2011-0314196-A1		Response to Missing Parts filed 9/8/11.
6534-01900 (formerly 70596.21)	Systems and Methods for High Speed Data Recovery With Free Running Sampling Clock	2/25/2011	13/035,213				Assigned to SMSC S.a r.l. Corrected Application Papers (drawings) filed 5/11/11. Foreign filing deadline **2/25/12**.
6534-02000 (formerly 70596.22)	Multiphase Clock Generation And Calibration	2/25/2011	13/035,331				Assigned to SMSC S.a r.l. Corrected Application Papers (drawings) filed 5/10/11. Foreign filing deadline **2/25/12**.

File No.	Title of Application/ Patent	Date Filed	Serial No.	Publication Date	Publication No.	Date Issued	Patent No./Status
6534-02100 (formerly 70596.23)	Internal Cable Calibration And Compensation	2/25/2011	13/035,710				Assigned to SMSC S.a r.l. Corrected Application Papers (drawings) filed 5/13/11. Foreign filing deadline 2/25/12.
6534-02200 (formerly 21065US01)	Efficient Use of Flash Memory in Flash Drives	12/14/2009	12/637,322				Waiting for Office Action.
6534-02201 (formerly 21065WO01)	Efficient Use of Flash Memory in Flash Drives	12/14/2010	PCT/US2010/060284				
6534-02300 (formerly 22874US01)	Software Controlled Power Limiting in USB to SATA Bridge	12/20/2010	12/972,773				Assigned to Symwave, Inc. and SMSC S.a r.l. Waiting for Office Action.
6534-02400 (formerly 22875US01)	Speculative Read-Ahead for Improving System Throughput	2/16/2011	13/028,762				Response to Office Action due 3/28/12.

S.No	Ulx Reference No.	SMSC Reference No.	Application No.	Patent No.	Filing Date	Issue Date	Country	Title	SMSC assignee (entity)	"Ulex Status (Pending, Approved, Issued, Lapsed, Abandoned)
1	SMC-PDR-1001	UL-0100	12883149		15-Sep-10		US	METHOD AND SYSTEM FOR TRANSFERRING HIGH-SPEED DATA WITHIN A PORTABLE DEVICE	Standard Microsystems Corporation	Filed
	SMC-PDR-1001	UL-0100	100133055		14-Sep-11		Taiwan	METHOD AND SYSTEM FOR TRANSFERRING HIGH-SPEED DATA WITHIN A PORTABLE DEVICE	Standard Microsystems Corporation	Filed
2	SMC-PDR-1002	UL-0200	12868724		26-Aug-10		US	METHOD AND SYSTEM FOR SECURING ACCESS TO A STORAGE DEVICE	Standard Microsystems Corporation	Filed
	SMC-PDR-1002	UL-0200	100130668		16-Sep-11		Taiwan	METHOD AND SYSTEM FOR SECURING ACCESS TO A STORAGE DEVICE	Standard Microsystems Corporation	Filed

S.No	Ulx Reference No.	SMSC Reference No.	Application No.	Patent No.	Filing Date	Issue Date	Country	Title	SMSC assignee (entity)	"Ulex Status (Pending, Approved, Issued, Lapsed, Abandoned)
3	SMC-PDR-1003	UL-0300	12884154		16-Sep-10		US	METHOD AND SYSTEM FOR TRANSFERRING DATA BETWEEN A HOST DEVICE AND AN EXTERNAL DEVICE	Standard Microsystems Corporation	Filed
	SMC-PDR-1003	UL-0300	100133056		14-Sep-11		Taiwan	METHOD AND SYSTEM FOR TRANSFERRING DATA BETWEEN A HOST DEVICE AND AN EXTERNAL DEVICE	Standard Microsystems Corporation	Filed
4	SMC-PDR-1004	UL-0400	13166849		23-Jun-11		US	METHOD AND SYSTEM FOR PREVENTING EXECUTION OF MALWARE	Standard Microsystems Corporation	Filed
5	SMC-PDR-1005	UL-0500	12978371		23-Dec-10		US	METHOD AND SYSTEM FOR DETERMINING AN ARBITRARY CHARGING PROTOCOL IN USB CHARGING PORTS	Standard Microsystems Corporation	Filed

S.No	Ulx Reference No.	SMSC Reference No.	Application No.	Patent No.	Filing Date	Issue Date	Country	Title	SMSC assignee (entity)	"Ulex Status (Pending, Approved, Issued, Lapsed, Abandoned)
	SMC-PDR-1005	UL-0500	1000147512		20-Dec-11		Taiwan	METHOD AND SYSTEM FOR DETERMINING AN ARBITRARY CHARGING PROTOCOL IN USB CHARGING PORTS	Standard Microsystems Corporation	Filed
6	SMC-PDR-1006	UL-0600	13004890		12-Jan-11		US	METHOD AND SYSTEM FOR IMPLEMENTING BUS OPERATIONS WITH PRECISE TIMING	Standard Microsystems Corporation	Filed
	SMC-PDR-1006	UL-0600	101100228		12-Jan-12		Taiwan	METHOD AND SYSTEM FOR IMPLEMENTING BUS OPERATIONS WITH PRECISE TIMING	Standard Microsystems Corporation	Filed
	SMC-PDR-1006	UL-0600	PCT/US12/21147		12-Jan-12		PCT	METHOD AND SYSTEM FOR IMPLEMENTING BUS OPERATIONS WITH PRECISE TIMING	Standard Microsystems Corporation	Filed

S.No	Ulx Reference No.	SMSC Reference No.	Application No.	Patent No.	Filing Date	Issue Date	Country	Title	SMSC assignee (entity)	"Ulex Status (Pending, Approved, Issued, Lapsed, Abandoned)
7	SMC-D-PDR-1007	UL-0700	13149529		31-May-11		US	METHOD AND SYSTEM FOR DETERMINING WHETHER A PORTABLE DEVICE IS CHARGING	Standard Microsystems Corporation	Filed
8	SMC-D-PDR-1008	UL-0800	13173287		30-Jun-11		US	METHOD AND SYSTEM FOR SAMPLING MULTIPLE PROFILES IN A CHARGING PORT WITHOUT HOST INTERVENTION	Standard Microsystems Corporation	Filed
9	SMC-D-PDR-1010	UL-1000	13233949		15-Sep-11		US	METHOD AND SYSTEM FOR OPTIMIZING CURRENT LIMITING BEHAVIOR OF CHARGER	Standard Microsystems Corporation	Filed
10	SMC-D-PDR-1011	UL-1100	13232965		14-Sep-11		US	METHOD AND SYSTEM FOR POWER SWITCH TEMPERATURE REGULATION	Standard Microsystems Corporation	Filed

S.No	Ulx Reference No.	SMSC Reference No.	Application No.	Patent No.	Filing Date	Issue Date	Country	Title	SMSC assignee (entity)	"Ulex Status (Pending, Approved, Issued, Lapsed, Abandoned)
11	SMC-D-PDR-1012	UL-1200	13157282		9-Jun-11		US	METHOD AND SYSTEM FOR RATIONING CHARGE OR ENERGY PROVIDED TO A PORTABLE DEVICE	Standard Microsystems Corporation	Filed
12	SMC-D-PDR-1013	UL-1300	13183441		15-Jul-11		US	METHOD AND SYSTEM FOR CONTROLLING ACCESS TO EMBEDDED NONVOLATILE MEMORIES	Standard Microsystems Corporation	Filed
13	SMC-D-PDR-1014	UL-1400	13406533		28-Feb-12		US	EXTENSIBLE HARDWARE DEVICE CONFIGURATION USING MEMORYY	Standard Microsystems Corporation	Filed
14	SMC-D-PDR-1016	UL-1600	13407783		29-Feb-12		US	METHOD AND SYSTEM FOR PORT POWER SWITCH PROFILE BASED CURRENT LIMITING	Standard Microsystems Corporation	Filed

S.No	Ulx Reference No.	SMSC Reference No.	Application No.	Patent No.	Filing Date	Issue Date	Country	Title	SMSC assignee (entity)	"Ulex Status (Pending, Approved, Issued, Lapsed, Abandoned)
15	SMC-D-PDR-1018	UL-1800	13307018		30-Nov-11		US	METHOD AND SYSTEM FOR HIGH GAIN AUTO-ZEROING SCHEME FOR ELECTRONIC CIRCUITS	Standard Microsystems Corporation	Filed
16	SMC-D-PDR-1019	UL-1900	13303176		23-Nov-11		US	METHOD AND SYSTEM FOR ATTACHMENT AND REMOVAL INDICATION FOR BATTERY CHARGING DEVICES	Standard Microsystems Corporation	Filed
17	SMC-D-PDR-1020	UL-2000	13354362		20-Jan-12		US	METHODS AND SYSTEMS FOR IMPROVING TOUCH SENSITIVITY OF TOUCH-BASED DEVICES	Standard Microsystems Corporation	Filed
18	SMC-D-PDR-1021	UL-2100	13301809		22-Nov-11		US	METHOD AND SYSTEM FOR AUTHENTICATING COMMUNICATION	Standard Microsystems Corporation	Filed

S.No	Ulx Reference No.	SMSC Reference No.	Application No.	Patent No.	Filing Date	Issue Date	Country	Title	SMSC assignee (entity)	"Ulex Status (Pending, Approved, Issued, Lapsed, Abandoned)
19	SMC-D-PDR-1022	UL-2200	13407786		29-Feb-12		US	FLEXIBLE WIRELESS CONNECTIVITY FOR MULTIMEDIA SYSTEMS	Standard Microsystems Corporation	Filed
20	SMC-D-PDR-1023	UL-2300	13307022		30-Nov-11		US	AUTO-RANGING SAR ADC FOR CURRENT SENSE APPLICATIONS	Standard Microsystems Corporation	Filed

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor

ALL PATENTS ON THIS LIST ARE OWNED BY STANDARD MICROSYSTEMS CORPORATION UNLESS OTHERWISE NOTED
Note: The dates appearing beneath the serial numbers and patent numbers are the dates of application and/or issuance of the patents.

07/965,145 (10/22/92) 0420-144 (CIP of File 0420-142) (See Continuation under Serial No. 08/503,136 - 0420-144A)	5,434,976 (7/18/95) EXPIRES 9-28-12				METHOD AND APPARATUS FOR PROCESSING DATA WITHIN STATIONS OF A COMMUNICATION NETWORK
08/088,008 (7/6/93) 0420-145	5,448,598 (9/5/95) EXPIRES 7-6-13	No Foreign Filing			IMPROVED PLL CLOCK RECOVERY CIRCUIT AND INTEGRATED CIRCUIT TRANSCEIVER CHIP EMPLOYING THE SAME
		INVENTOR:	IAN HARRIS		
08/541,642 (10/10/95) 0420-158	5,708,819 1/13/98 EXPIRES 10-10-15	Taiwan	85112275 (10/10/96)	108433 (09/02/99)	PROCESS AND APPARATUS FOR GENERATING POWER MANAGEMENT EVENTS IN A COMPUTER SYSTEM
08/774,626 (12/30/96)	5,892,943 4/6/99				SHARED BIOS ROM WARM BOOT

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
	EXPIRES 12-30-16				
0420-160		Taiwan	86119599	104641 12/1/99 (EXPIRES 12-22-17)	
08/766,496 (12/13/96)	5,953,372 (9/14/99) EXPIRES 12-13-16	NO FOREIGN FILING			METHOD AND APPARATUS FOR LOOPBACK TRANSMISSION TESTING IN A COMMUNICATIONS DEVICE
0420-164					
08/799,253 CIRCUIT (2/14/97)	5,774,009 (6/30/98) EXPIRES 2-14-17	NO FOREIGN FILING			RTC OSCILLATOR AMPLIFIER WITH IMPROVED NOISE IMMUNITY
0420-165					
08/802,335 COMMUNICATIONS (2/11/97) DETECTION	5,898,513 4/27/99 EXPIRES 2-11-17	NO FOREIGN FILING			CONSUMER INFRARED RECEIVER CARRIER RANGE CIRCUIT
0420-166					
08/008,669	5,311,083				VERY LOW VOLTAGE INTER-

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
(1/25/93)	(5/10/94) EXPIRES 1-25-13				CHIP CMOS LOGIC SIGNALING FOR LARGE NUMBERS OF HIGH-SPEED OUTPUT LINES EACH ASSOCIATED WITH LARGE CPACITANCE LOADS
0420-174 SS-595-05					
08/134,571 (10/8/93)	5,500,610 (3/19/96) EXPIRES 10-8-13	No Foreign Filing			VERY HIGH CURRENT INTEGRATED CIRCUIT OUTPUT BUFFER WITH SHORT CIRCUIT PROTECTION AND REDUCED POWER BUS SPIKES
68987-002 3633-2					
08/126,176 (9/23/93)	5,544,323 (8/6/96) EXPIRES 9-23-13	No Foreign Filing			HIGH BIT RATE CSMA/CD USING MULTIPLE PAIRS
68987-003 3633-3 (See continuation under File No. 3633-3.1)					
08/719,310 (9/24/96)	5,687,201 (11/11/97)	No Foreign Filing			PHASE-LOCKED-LOOP WITH LINEAR COMBINATION OF CHARGE PUMP

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
	EXPIRES 3-21-15				AND CURRENT CONTROLLED OSCILLATOR
68987-011 3633-6.1 (Continuation of File No. 3633-6)					
08/403,931 (3/14/95)	5,612,648 (3/18/97) EXPIRES 3-14-15	No Foreign Filing			TRANSCONDUCTANCE-CAPACITANCE FILTER WITH EXTENDED CONTROL RANGE
68987-012 3633-7					
08/388,234 (2/13/95)	5,555,524 9/10/96 EXPIRES 2-13-15	No Foreign Filing			SEMI-SYNCHRONOUS DUAL PORT FIFO
68987-013 3633-8					
08/555,369 (11/8/95)	5,744,990 (4/28/98) EXPIRES 11-8-15	No Foreign Filing			ENHANCED POWER-ON-RESET/ LOW VOLTAGE DETECTION CIRCUIT
68987-016 3633-11					
08/741,741 (10/31/96)	5,847,586 (12/8/98) EXPIRES 11-8-15	No Foreign Filing			ENHANCED POWER-ON-RESET/ LOW VOLTAGE DETECTION CIRCUIT

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
68987-017 3633-11.1 (Continuation in part of File No. 3633-11)					
08/661,128 (6/10/96)	5,826,105 (10/20/98) EXPIRES 6-10-16	No Foreign Filing		SYSTEM FOR USING AN EXTERNAL CPU	TO ACCESS MULTIFUNCTION CONTROLLERS CONTROL REGISTERS VIA CONFIGURATION REJEISTERS THEREOF AFTER DISABLING THE EMBEDDED MICROPROCESSOR (ORIGINALLY ENTITLED: BRIDGE MODE)
68987-018 3633-12					
08/683,547 (7/16/96)	5,907,862 (5/25/99) EXPIRES 7-16-16	Taiwan ~~3707-13800~~ **68987-033**	86109707 (7/10/97)	098339 (9/21/98)	METHOD AND APPARATUS FOR THE SHARING OF A MEMORY DEVICE BY MULTIPLE PROCESSORS 3633-16 68987-032
08/714,952 (9/17/96)	6,192,469 2/20/01 EXPIRES 9-17-16	Taiwan ~~3707-13900~~ **68987-036**	86109888 (7/14/97)	120495 9/1/00	RELOCATABLE CODE STORAGE IN AN INTEGRATED CIRCUIT WITH AN EMBEDDED MICROPROCESSOR
3633-18 68987-035					
08/846,882 MICROCONTROLLER	6,185,641				USB PERIPHERAL

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
(5/1/97)	(2/6/01)				HABANERO
3633-20 **68987-038**	EXPIRES 5-1-17				
09/711,486 (11-13-00) **Bryan Cave No. 118983**	6,429,685 (8/6/02) EXPIRES 11-13-20				Integrated Circuit and Method of Controlling Output Impedance
10/081,821 (2/20/02) CIP of 09/711,486 **Bryan Cave No. 130349**	6,753,699 6-22-04 EXPIRES 11-13-20 Publication No. US 2002/0089351 A1 (7-11-02)				Integrated Circuit and Method of Controlling Output Impedance
09/711,420 (11-13-00) **Bryan Cave No. 120609**	6,788,506 9-7-04 EXPIRES 11-13-20				Integrated Circuit and Method of Operation

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
09/711,482 (11-13-00) **Bryan Cave No. 120610**	6,362,613 3-26-02 EXPIRES 11-13-20				Integrated Circuit and Method of Operation
09/321,064 (5-27-99) **Perkins Coie 59178-8001.US01**	6,184,750 (2-6-01) EXPIRES 5-27-19 SMSC MONITORS				Control Circuit Driven by a Differential Input Voltage and Method for Controlling Same
09/516,008 (2-29-00) **Perkins Coie 59178-8003.US01** **Joint w/ Seiko**	6,366,167 4-2-02 EXPIRES 2-29-20 SMSC MONITORS	Japan Seiko monitors Japanese Application	2001-54673 (2/29/00) allowed	4578703 09-03-10	Low Voltage Rail-to-Rail CMOS Input Stage

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
10/013,581 (12-10-01) **Perkins Coie** **59178-8003.US02** **Joint w/ Seiko**	6,870,422 3-22-05 Publication No. US-2002-0053948-A1 (5-9-02) EXPIRES 12-10-21 SMSC MONITORS				Low Voltage Rail-to-Rail CMOS Input Stage
09/515,961 (2-29-00) **Perkins Coie** **59178-8004.US01** **Joint w/ Seiko**	6,353,363 3-5-02 EXPIRES 2-29-20 SMSC MONITORS	Japan .JP01 Seiko monitors Japanese Application	2001-54672 (2/29/00) Allowed	4672883 1-28-2011	Low Voltage Rail-to-Rail CMOS Output Stage
09/439,583 (11-12-99) [continuation of 09/144,214] **Perkins Coie** **59305-8033.US02** Joint w/ Maxim	6,181,204 (1-30-01) EXPIRES 8-31-18				Linear and Multi-Sinh Transconductance Circuits

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
09/729,749 (12-5-00) **Perkins Coie** **59305-80033.US03** *Joint w/ Maxim*	6,489,848 (12-3-02) EXPIRES 11-12-19				Linear and Multi-Sinh Transconductance Circuits
09/881/596 (6-14-01) **Perkins Coie** **59305-8071.US01** Joint w/ Maxim	6,586,987 (7-1-03) EXPIRES 6-14-21				Circuit with Source Follower Output Stage and Adaptive Current Mirror Bias
666,859 (6-19-96) Joint w/ Maxim	5,736,900 (4-7-98) EXPIRES 6-19-16	EPO			Method and Apparatus for Amplifying an Electrical Signal
684,193 (7-19-96) Joint w/ Maxim	5,736,902 (4-7-98) EXPIRES 7-19-16	Taiwan	86110166	125591 (5-14-01)	High-Gain Common-Emitter Output Stage

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
665,370 (6-19-96)	5,754,066 (5-19-98) EXPIRES 6-19-16				Output Stage for Buffering an Electrical Signal and Method for Performing the Same
Joint w/ Maxim					
09/252,317 (2-18-99) Continuation of 09/177,926 (abandoned)	6,020,785 (2-1-00) EXPIRES 2-18-19	Japan EP			Fixed Gain Operational Amplifiers
Joint w/ Maxim					
09/313,151 (5-17-99)	6,121,764 (9-19-00) EXPIRES 5-17-19				Current Source Having High Impedance Current Output and Method Therefor
Joint w/ Maxim					
09/163,891 (9-30-98) **Perkins Coie** **59305-8034.US01**	6,188,281 (2-13-01) EXPIRES 9-30-18	EP .EP01 JP .JP01	999 49749.8 (9-21-99) 2000-272996 (9-21-99)		Linear Transconductance Circuits Having Class AB Amplifiers Parallel Coupled with Concave Compensation Circuits
Joint w/ Maxim					

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
09/261,070 (3-2-99) Joint w/ Maxim	6,208,196 (3-27-01) EXPIRES 3-2-19				Current Mode Charge Pumps
08/752,605 (11-18-96) MAX1P017 Joint w/ Maxim	5,907,262 (5-25-99) EXPIRES 11-18-16	Taiwan Japan PCT	86117019 PCT/US97/21822	111514 (6-3-00)	Folded-Cascade Amplifier Stage
09/204,322 (12-2-98) *Perkins Coie* **59305-8031.US01** Joint w/ Maxim	6,166,603 (12-26-00) EXPIRES 12-2-18	EPO .EP01 Japan .JP01	96-922602.6-1270 Abandoned per PC listing 2000-585996 (8/2/00)		Class-AB Output Stages with Improved Distortion Performance

Serial Number Attorney File #	U.S. Patent #	Foreign	Serial Number	Patent #	Title/Inventor
11/729,999 03-29-07					FAN CONTROLLER WITH DUTY CYCLE COMPARATOR
ANDIGILOG-019					
11/730,000 03-29-07	7,667,512 03-29-07 EXPIRES 03-29-2027				DUTY CYCLE COMPARATOR
ANDIGILOG-021					
10/739,797 12/18/03	6,937,100 8-30-05 EXPIRES 12-19-2023				CIRCUIT AND METHOD FOR COMMON MODE FEEDBACK
PUB. NO. US-2005-0134382-A1 PUB. DATE 6-23-05					
JOINT W/ NEW JAPAN RADIO (NJR)					
5707-01900					

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-00100/ United States of America	ORD	08/486690 07-Jun-1995		5654711 05-Aug-1997	Granted 07-Jun-2015

Owner Name: Asai Kasei Microsystems Co. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: Analog-to-Digital Converter with Local Feedback Amended
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-00200/ United States of America	ORD	08/558636 13-Nov-1995		5826072 20-Oct-1998	Granted 13-Nov-2015

Owner Name: OADI ***Attorney(s):*** KLD LJM
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: A Pipelined Signal Processor and Signal Processing System Employing Same
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-00303/ United States of America	CPA	08/580272 27-Dec-1995		5835390 10-Nov-1998	Granted 27-Dec-2015

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: Merged Multi-Stage Comb Filter With Reduced Operational Requirements
Resp. Office: AUSTIN

Note: For Docket Numbers that begin with "5104", the present owner is Standard Microsystems Corporation (SMSC) except those dockets that have Asai Kasei Microsystems Co. (Asai) as Owner Name. In those cases, the patent is jointly owned by Asai and SMSC.

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-01400/	ORD	09/025157		6057791	Granted
United States of America		18-Feb-1998		02-May-2000	18-Feb-2018

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: APPARATUS AND METHOD FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE TO ENHANCE DIGITAL OPERATION AND REDUCE ANALOG SAMPLING ERROR
Resp. Office: AUSTIN

5104-01402/	EPC	99907000.6	1057261	1057261	Granted
Germany		12-Feb-1999	06-Dec-2000	21-Apr-2004	12-Feb-2019

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: Apparatus and Method for Clocking Digital And Analog Circuits On A Common Substrate To Enhance Digital Operation And Reduce Analog Sampling Error
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-01403/ Japan	ORD	2000-532917 12-Feb-1999		4091254 07-Mar-2008	Granted 12-Feb-2019

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 13889-B
Title: Apparatus and Method for Clocking Digital And Analog Circuits On A Common Substrate To Enhance Digital Operation And Reduce Analog Sampling Error
Resp. Office: AUSTIN

5104-01404/ Germany	EDV	69933063.7 12-Feb-1999	1414156 28-Apr-2004	1414156 30-Aug-2006	Granted 12-Feb-2019

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: APPARATUS AND METHOD FOR CLOCKING DIGITAL AND ANALOG CIRCUITS ON A COMMON SUBSTRATE TO ENHANCE DIGITAL OPERATION AND REDUCE ANALOG SAMPLING ERROR
Resp. Office: Austin

5104-01500/ ited States of America	ORD	08/582644 04-Jan-1996		5721547 24-Feb-1998	Granted 04-Jan-2016

Owner Name: OADI ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: Analog-To-Digital Converter With DC Offset Cancellation
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-01600/ United States of America	ORD	08/630436 10-Apr-1996		5729232 17-Mar-1998	Granted 10-Apr-2016

Owner Name: Asahi Kasei & Oasis Design ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: Combination Shared Capacitor Integrator & Digital-to-Analog Converter Circuit With Data Dependency Cancellation
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-01700/ United States of America	ORD	08/630390 10-Apr-1996		5790064 04-Aug-1998	Granted 10-Apr-2016

Owner Name: Asahi Kasei & Oasis ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:*** P96035-US
Agent Name: ***Agent Ref:***
Title: An Apparatus & Method For Switching Capacitors Within ASwitched Capacitor Circuit At Times Selected To Avoid Data Dependent Loading Upon Reference Voltage Supplies
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02000/ United States of America	ORD	08/951650 16-Oct-1997		6049254 11-Apr-2000	Granted 16-Oct-2017

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: PHASE-LOCKED LOOP WHICH CAN AUTOMATICALLY ADJUST TO AND LOCK UPON VARIABLE INPUT FREQUENCY
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02002/ Germany	EPC	98953611.5 16-Oct-1998	1023776 02-Aug-2000	1023776 30-Jul-2003	Granted 16-Oct-2018

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: A Phase-Locked Loop Which Can Automatically Adjust To & Lock Upon A Variable Input Frequency
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02002/ Sweden	EPC	98953611.5 16-Oct-1998	1023776 02-Aug-2000	1023776 30-Jul-2003	Granted 16-Oct-2018

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: A Phase-Locked Loop Which Can Automatically Adjust To & Lock Upon A Variable Input Frequency
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02002/ United Kingdom	EPC	98953611.5 16-Oct-1998	1023776 02-Aug-2000	1023776 30-Jul-2003	Granted 16-Oct-2018

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: A Phase-Locked Loop Which Can Automatically Adjust To & Lock Upon A Variable Input Frequency
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02100/ United States of America	ORD	08/951796 16-Oct-1997		6005904 21-Dec-1999	Granted 16-Oct-2017

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: A PHASE-LOCKED LOOP WITH PROTECTED OUTPUT DURING INSTANCES WHEN THE PHASE-LOCKED LOOP IS UNLOCKED
Resp. Office: AUSTIN

5104-02102/ Germany	EPC	98951043.3 13-Oct-1998	1012979 28-Jun-2000	1012979 30-Jul-2003	Granted 13-Oct-2018

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: A PHASE-LOCKED LOOP WITH PROTECTED OUTPUT DURING INSTANCES WHEN THE PHASE-LOCKED LOOP IS UNLOCKED
Resp. Office: AUSTIN

5104-02102/ Sweden	EPC	98951043.3 13-Oct-1998	1012979 28-Jun-2000	1012979 30-Jul-2003	Granted 13-Oct-2018

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: A PHASE-LOCKED LOOP WITH PROTECTED OUTPUT DURING INSTANCES WHEN THE PHASE-LOCKED LOOP IS UNLOCKED
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02102/ United Kingdom	EPC	98951043.3 13-Oct-1998	1012979 28-Jun-2000	1012979 30-Jul-2003	Granted 13-Oct-2018

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: A PHASE-LOCKED LOOP WITH PROTECTED OUTPUT DURING INSTANCES WHEN THE PHASE-LOCKED LOOP IS UNLOCKED
Resp. Office: AUSTIN

5104-02103/ Japan	ORD	2000-517487 17-Apr-2000		4034515 02-Nov-2007	Granted 13-Oct-2018

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 13508-B
Title: A PHASE-LOCKED LOOP WITH PROTECTED OUTPUT DURING INSTANCES WHEN THE PHASE-LOCKED LOOP IS UNLOCKED
Resp. Office: AUSTIN

5104-02104/ Germany	EDV	03007754.9 13-Oct-1998	69834354.9 06-Aug-2003	1333580 06-Apr-2006	Granted 13-Oct-2018

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: PHASE-LOCKED LOOP AND INTEGRATED CIRCUIT THEREFORE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02104/ United Kingdom	EDV	03007754.9 13-Oct-1998	1333580 06-Aug-2003	1333580 26-Apr-2006	Granted 13-Oct-2018

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: PHASE-LOCKED LOOP AND INTEGRATED CIRCUIT THEREFORE
Resp. Office: Austin

5104-02602/ Germany	EPC	00911928.0 22-Feb-2000	60028313 26-Oct-2006	1086534 31-May-2006	Granted 22-Feb-2020

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM EMPLOYING A NETWORK OF POWER MANAGED TRANSCEIVERS THAT CAN GENERATE A CLOCKING SIGNAL OR ENABLE DATA BYPASS OF A DIGITAL SYSTEM ASSOCIATED WITH EACH TRANSCEIVER
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02602/	EPC	00911928.0		1086534	Granted
Sweden		22-Feb-2000		31-May-2006	22-Feb-2020

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM EMPLOYING A NETWORK OF POWER MANAGED TRANSCEIVERS THAT CAN GENERATE A CLOCKING SIGNAL OR ENABLE DATA BYPASS OF A DIGITAL SYSTEM ASSOCIATED WITH EACH TRANSCEIVER
Resp. Office: AUSTIN

5104-02602/	EPC	00911928.0		1086534	Granted
United Kingdom		22-Feb-2000		31-May-2006	22-Feb-2020

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM EMPLOYING A NETWORK OF POWER MANAGED TRANSCEIVERS THAT CAN GENERATE A CLOCKING SIGNAL OR ENABLE DATA BYPASS OF A DIGITAL SYSTEM ASSOCIATED WITH EACH TRANSCEIVER
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02603/	ORD	2000-387942		4672137	Granted
Japan		20-Oct-2000		28-Jan-2011	20-Dec-2020

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** 14256-B
Title: COMMUNICATION SYSTEM EMPLOYING A NETWORK OF POWER MANAGED TRANSCEIVERS THAT CAN GENERATE A CLOCKING SIGNAL OR ENABLE DATA BYPASS OF A DIGITAL SYSTEM ASSOCIATED WITH EACH TRANSCEIVER
Resp. Office: AUSTIN

5104-02604/	CPA	09/253469		6763060	Granted
United States of America		23-Dec-2002		13-Jul-2004	19-Feb-2019

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM EMPLOYING A NETWORK OF POWER MANAGED TRANSCEIVERS THAT CAN GENERATE A CLOCKING SIGNAL OR ENABLE DATA BYPASS OF A DIGITAL SYSTEM ASSOCIATED WITH EACH TRANSCEIVER
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02605/	EDV	60038989.8	1648094	1648094	Granted
Germany		22-Feb-2000	19-Apr-2006	21-May-2008	22-Feb-2020

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM EMPLOYING A NETWORK OF POWER MANAGED TRANSCEIVERS THAT CAN GENERATE A CLOCKING SIGNAL OR ENABLE DATA BYPASS OF A DIGITAL SYSTEM ASSOCIATED WITH EACH TRANSCEIVER
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02605/	EDV	06001159.0	1648094	1648094	Granted
Sweden		22-Feb-2000	19-Apr-2006	21-May-2008	22-Feb-2020

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM EMPLOYING A NETWORK OF POWER MANAGED TRANSCEIVERS THAT CAN GENERATE A CLOCKING SIGNAL OR ENABLE DATA BYPASS OF A DIGITAL SYSTEM ASSOCIATED WITH EACH TRANSCEIVER
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02607/ Japan	DIV	2010-278127 14-Dec-2010			Pending

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** 19099-B
Title: COMMUNICATION SYSTEM EMPLOYING A NETWORK OF POWER MANAGED TRANSCEIVERS THAT CAN GENERATE A CLOCKING SIGNAL OR ENABLE DATA BYPASS OF A DIGITAL SYSTEM ASSOCIATED WITH EACH TRANSCEIVER
Resp. Office: AUSTIN

5104-02608/ Japan	DIV	2010-278130 14-Dec-2010			Pending

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 19100-B
Title: COMMUNICATION SYSTEM EMPLOYING A NETWORK OF POWER MANAGED TRANSCEIVERS THAT CAN GENERATE A CLOCKING SIGNAL OR ENABLE DATA BYPASS OF A DIGITAL SYSTEM ASSOCIATED WITH EACH TRANSCEIVER
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02800/ United States of America	ORD	09/710220 10-Nov-2000		6437710 20-Aug-2002	Granted 10-Nov-2020

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS
Resp. Office: AUSTIN

5104-02802/ European Patent Convention	ORD	01997044.1 05-Nov-2001		1336284 01-Oct-2008	Granted 05-Nov-2021

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** OA 2003/17 EUP
Title: ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02802/ France	EPC	01997044.1 05-Nov-2001		1336284 01-Oct-2008	Granted 05-Nov-2021

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS
Resp. Office: AUSTIN

5104-02802/ Germany	EPC	01997044.1 05-Nov-2001	60136004.4	1336284 01-Oct-2008	Granted 05-Nov-2021

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02802/	EPC	01997044.1		1336284	Granted
Sweden		05-Nov-2001		01-Oct-2008	05-Nov-2021

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS
Resp. Office: AUSTIN

5104-02802/	EPC	01997044.1		1336284	Granted
United Kingdom		05-Nov-2001		01-Oct-2008	05-Nov-2021

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-02804/	ORD	1020037006380		10-0849427	Granted
Korea, Republic of		05-Nov-2001		24-Jul-2008	05-Nov-2021

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: Origin Int'l Patent & Law Firm ***Agent Ref:*** IP20033436US
Title: ENCODER WITHIN A COMMUNICATION SYSTEM THAT AVOIDS ENCODED DC ACCUMULATION AND CAN USE CODING VIOLATIONS TO SYNCHRONIZE A DECODER AND DETECT TRANSMISSION ERRORS
Resp. Office: AUSTIN

5104-03100/	ORD	10/180696	04-0001495	7327742	Granted
United States of America		26-Jun-2002	01-Jan-2004	05-Feb-2008	10-Apr-2025

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM AND METHOD FOR SENDING ISOCHRONOUS STREAMING DATA WITHIN A FRAME SEGMENT USING A SIGNALING BYTE
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-03101/	DIV	11/961047	08/0095190	7809023	Granted
United States of America		20-Dec-2007	24-Apr-2008	05-Oct-2010	28-Apr-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM AND METHOD FOR SENDING ISOCHRONOUS STREAMING DATA WITHIN A FRAME SEGMENT USING A SIGNALING BYTE
Resp. Office: AUSTIN

5104-03102/	DIV	11/961086	08/0095191	7801159	Granted
United States of America		20-Dec-2007	24-Apr-2008	21-Sep-2010	22-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM AND METHOD FOR SENDING ISOCHRONOUS STREAMING DATA WITHIN A FRAME SEGMENT USING A SIGNALING BYTE
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-03400/	ORD	10/180741	04-0003109	7164691	Granted
United States of America		26-Jun-2002	01-Jan-2004	16-Jan-2007	21-Aug-2024

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATIONS SYSTEM AND METHOD FOR SENDING ISOCHRONOUS STREAMING DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A CODING VIOLATION TO SIGNIFY INVALID OR EMPTY BYTES WITHIN THE FRAME SEGMENT
Resp. Office: AUSTIN

5104-03500/	ORD	10/157673	03-0225951	6874048	Granted
United States of America		29-May-2002	04-Dec-2003	29-Mar-2005	07-Oct-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM AND METHODOLOGY FOR SENDING A DESIGNATOR FOR AT LEAST ONE OF A SET OF TIME-DIVISION MULTIPLEXED CHANNELS FORWARDED ACROSS A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-03600/	ORD	10/157097	03-0225953	6922747	Granted
United States of America		29-May-2002	04-Dec-2003	26-Jul-2005	24-Jul-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM AND METHODOLOGY FOR ADDRESSING AND SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

5104-03602/	EPC	DE 60304178	1512253	1512253	Granted
Germany		28-May-2003	09-May-2005	22-Mar-2006	28-May-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-03602/	EPC	03729146.5	1512253	1512253	Granted
Italy		28-May-2003	09-Mar-2005	22-Mar-2006	28-May-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

5104-03602/	EPC	03729146.5	1512253	1512253	Granted
Sweden		28-May-2003	09-Mar-2005	22-Mar-2006	28-May-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

5104-03602/	EPC	03729146.5	1512253	1512253	Granted
United Kingdom		28-May-2003	09-Mar-2005	22-Mar-2006	28-May-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-03603/	DIV	06000673.1	1646187	1646187	Granted
European Patent Convention		28-May-2003	12-Apr-2006	20-May-2009	28-May-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

5104-03603/	EDV	06000673.1	1646187	1646187	Granted
Germany		28-May-2003	12-Apr-2006	20-May-2009	28-May-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

5104-03603/	EDV	06000673.1	1646187	1646187	Granted
Sweden		28-May-2003	12-Apr-2006	20-May-2009	28-May-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-03603/	EDV	06000673.1	1646187	1646187	Granted
United Kingdom		28-May-2003	12-Apr-2006	20-May-2009	28-May-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DATA OF DISSIMILAR TYPE AND SIZE ACROSS CHANNELS FORMED WITHIN A LOCALLY SYNCHRONIZED BUS
Resp. Office: AUSTIN

5104-04000/	ORD	10/180729	04-0003108	7283564	Granted
United States of America		26-Jun-2002	01-Jan-2004	16-Oct-2007	14-Jul-2024

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM AND METHOD FOR SENDING ASYNCHRONOUS DATA AND/OR ISOCHRONOUS STREAMING DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A CODING VIOLATION TO SIGNIFY AT LEAST THE BEGINNING OF A DATA TRANSFER
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04002/	EPC	60311991.3	1525691	1525691	Granted
Germany		04-Jun-2003	27-Apr-2005	21-Feb-2007	04-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY DATA TRANSFERS WITHIN THE FRAME SEGMENT
Resp. Office: Austin

5104-04002/	EPC	03736882.6	1525691	1525691	Granted
Sweden		04-Jun-2003	27-Apr-2005	21-Feb-2007	04-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY DATA TRANSFERS WITHIN THE FRAME SEGMENT
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04002/	EPC	03736882.6	1525691	1525691	Granted
United Kingdom		04-Jun-2003	27-Apr-2005	21-Feb-2007	04-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY DATA TRANSFERS WITHIN THE FRAME SEGMENT
Resp. Office: Austin

5104-04003/	ORD	2004-517617		4272150	Granted
Japan		04-Jun-2003		06-Mar-2009	04-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 16463-B
Title: COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY DATA TRANSFERS WITHIN THE FRAME SEGMENT
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04004/	DIV	07003305.5	1783936	1783936	Granted
European Patent Convention		04-Jun-2003	09-May-2007	11-May-2011	04-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: Patentanwaltskanzlei Dr. Lohr ***Agent Ref:*** OA 2004/01 EP T
Title: COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY DATA TRANSFERS WITHIN THE FRAME SEGMENT
Resp. Office: Austin

5104-04004/	EDV	60337111.6	1783936	1783936	Granted
Germany		04-Jun-2003	09-May-2007	11-May-2011	04-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY DATA TRANSFERS WITHIN THE FRAME SEGMENT
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04004/	EDV	07003305.5	1783936	1783936	Granted
Sweden		04-Jun-2003	09-May-2007	11-May-2011	04-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY DATA TRANSFERS WITHIN THE FRAME SEGMENT
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04004/	EDV	07003305.5	1783936	1783936	Granted
United Kingdom		04-Jun-2003	09-May-2007	11-May-2011	04-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY DATA TRANSFERS WITHIN THE FRAME SEGMENT
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04005/	DIV	2008-303840		4709269	Granted
Japan		04-Jun-2003		25-Mar-2011	04-Jun-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 18369-B
Title: COMMUNICATION SYSTEM FOR SENDING DISSIMILAR TYPES OF DATA ACROSS A SYNCHRONOUS NETWORK WITHIN A FRAME SEGMENT USING A SIGNALING BYTE OR CODING VIOLATIONS TO SIGNIFY DATA TRANSFERS WITHIN THE FRAME SEGMENT
Resp. Office: Austin

5104-04100/	ORD	10/218351	04-0032922	7158596	Granted
United States of America		14-Aug-2002	19-Feb-2004	02-Jan-2007	11-Aug-2024

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM AND METHOD FOR SENDING AND RECEIVING DATA AT A HIGHER OR LOWER SAMPLE RATE THAN A NETWORK FRAME RATE USING A PHASE LOCKED LOOP
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04200/	ORD	10/218349	04-0032350	7106224	Granted
United States of America		14-Aug-2002	19-Feb-2004	12-Sep-2006	14-Nov-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM AND METHOD FOR SAMPLE RATE CONVERTING DATA ONTO OR FROM A NETWORK USING A HIGH SPEED FREQUENCY COMPARISON TECHNIQUE
Resp. Office: AUSTIN

5104-04300/	ORD	10/218361	04-0032883	7272202	Granted
United States of America		14-Aug-2002	19-Feb-2004	18-Sep-2007	08-Sep-2025

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM AND METHOD FOR GENERATING SLAVE CLOCKS AND SAMPLE CLOCKS AT THE SOURCE AND DESTINATION PORTS OF A SYNCHRONOUS NETWORK USING THE NETWORK FRAME RATE
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04302/ European Patent Convention	ORD	03788391.5 12-Aug-2003	1530841 18-May-2005		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: Patentanwaltskanzlei Dr. Lohr ***Agent Ref:*** OA 2004/02 EP
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

5104-04303/ Japan	ORD	2004-529312 12-Aug-2003		4558486 30-Jul-2010	Granted 12-Aug-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 16567-B
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04304/ Korea, Republic of	ORD	1020057002525 12-Aug-2003			Pending

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** IP2005531/US
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04305/ China (Peoples Republic)	ORD	03822944.7 12-Aug-2003	1689258A 26-Oct-2005	1689258B 11-May-2011	Granted 12-Aug-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: Shanghai Patent & Trademark Law Office ***Agent Ref:*** USDM-0002
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04307/ Korea, Republic of	DIV	1020107013238 14-Feb-2005		10-1113305 31-Jan-2012	Granted 12-Aug-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** IP20101557/US
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

5104-04308/ Korea, Republic of	DIV	1020107013239 14-Feb-2005		10-1033545 29-Apr-2011	Granted 12-Aug-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: Origin Int'l Patent & Law Firm ***Agent Ref:*** IP20101558/US
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04309/ Korea, Republic of	DIV	1020107013240 14-Feb-2005		10-1052898 25-Jul-2011	Granted 12-Aug-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: Origin Int'l Patent & Law Firm ***Agent Ref:*** IP20101559/US
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04310/ Korea, Republic of	DIV	1020107013241 14-Feb-2005		10-1052900 25-Jul-2011	Granted 12-Aug-2023

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: Origin Int'l Patent & Law Firm ***Agent Ref:*** IP20101560/US
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04311/ China (Peoples Republic)	DIV	201010275933 12-Aug-2003	102013932 13-Apr-2011		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

5104-04312/ European Patent Convention	DIV	10183313.5 12-Aug-2003			Pending

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: COMMUNICATION SYSTEM FOR SENDING AND RECEIVING DATA ONTO AND FROM A NETWORK AT A NETWORK FRAME RATE USING A PHASE LOCKED LOOP, SAMPLE RATE CONVERSION, OR SYNCHRONIZING CLOCKS GENERATED FROM THE NETWORK FRAME RATE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04400/	ORD	10/253681	04-0057542	7664214	Granted
United States of America		24-Sep-2002	25-Mar-2004	16-Feb-2010	25-Jun-2025

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SYSTEM AND METHOD FOR TRANSFERRING DATA AMONG TRANSCEIVERS SUBSTANTIALLY VOID OF DATA DEPENDENT JITTER
Resp. Office: AUSTIN

5104-04402/	ORD	03799288.0	1547296		Published
European Patent Convention		24-Sep-2003	29-Jun-2005		

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SYSTEM AND METHOD FOR TRANSFERRING DATA AMONG TRANSCEIVERS SUBSTANTIALLY VOID OF DATA DEPENDENT JITTER
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04700/	ORD	10/655265	05-0053179	7609797	Granted
United States of America		04-Sep-2003	10-Mar-2005	27-Oct-2009	27-Oct-2026

Owner Name: Oasis Design, Inc. ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE
Resp. Office: AUSTIN

5104-04701/	EPC	04020230.1	1513284	1513284	Granted
Germany		26-Aug-2004	09-Mar-2005	08-Oct-2008	26-Aug-2024

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04701/	EPC	04020230.1	1513284	1513284	Granted
Sweden		26-Aug-2004	09-Mar-2005	08-Oct-2008	26-Aug-2024

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE
Resp. Office: Austin

5104-04701/	EPC	04020230.1	1513284	1513284	Granted
United Kingdom		26-Aug-2004	09-Mar-2005	08-Oct-2008	26-Aug-2024

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-04702/	ORD	2004-258166		4855663	Granted
Japan		06-Sep-2004		04-Nov-2011	06-Sep-2024

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 16303-B
Title: CIRCUIT, SYSTEM, AND METHOD FOR PREVENTING A COMMUNICATION SYSTEM ABSENT A DEDICATED CLOCKING MASTER FROM PRODUCING A CLOCKING FREQUENCY OUTSIDE AN ACCEPTABLE RANGE
Resp. Office: Austin

5104-04900/	ORD	10/651884		7268368	Granted
United States of America		29-Aug-2003		11-Sep-2007	06-Jul-2024

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SEMICONDUCTOR PACKAGE HAVING OPTICAL RECEPTICALS AND LIGHT TRANSMISSIVE/OPAQUE PORTIONS AND METHOD OF MAKING SAME
Resp. Office: AUSTIN

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05000/ United States of America	ORD	10/859470 02-Jun-2004	05-0271068 08-Dec-2005	7702405 20-Apr-2010	Granted 17-Feb-2029

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SYSTEM AND METHOD FOR TRANSFERRING NON-COMPLIANT PACKETIZED AND STREAMING DATA INTO AND FROM A MULTIMEDIA DEVICE COUPLED TO A NETWORK ACROSS WHICH COMPLIANT DATA IS SENT
Resp. Office: Austin

5104-05001/ European Patent Convention	ORD	05011315.8 25-May-2005	1603284 07-Dec-2005		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SYSTEM AND METHOD FOR TRANSFERRING NON-COMPLIANT PACKETIZED AND STREAMING DATA INTO AND FROM A MULTIMEDIA DEVICE COUPLED TO A NETWORK ACROSS WHICH COMPLIANT DATA IS SENT
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05002/	ORD	2005-161054		4751107	Granted
Japan		01-Jun-2005		27-May-2011	01-Jun-2025

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 16697-B
Title: SYSTEM AND METHOD FOR TRANSFERRING NON-COMPLIANT PACKETIZED AND STREAMING DATA INTO AND FROM A MULTIMEDIA DEVICE COUPLED TO A NETWORK ACROSS WHICH COMPLIANT DATA IS SENT
Resp. Office: Austin

5104-05003/	DIV	12/698296	10/0135309		Published
United States of America		02-Feb-2010	03-Jun-2010		

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SYSTEM AND METHOD FOR TRANSFERRING NON-COMPLIANT PACKETIZED AND STREAMING DATA INTO AND FROM A MULTIMEDIA DEVICE COUPLED TO A NETWORK ACROSS WHICH COMPLIANT DATA IS SENT
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05004/ Japan	DIV	2011-082563 04-Apr-2011			Pending

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SYSTEM AND METHOD FOR TRANSFERRING NON-COMPLIANT PACKETIZED AND STREAMING DATA INTO AND FROM A MULTIMEDIA DEVICE COUPLED TO A NETWORK ACROSS WHICH COMPLIANT DATA IS SENT
Resp. Office: Austin

5104-05100/ United States of America	ORD	10/966254 15-Oct-2004	06-0083328 20-Apr-2006	7634694 15-Dec-2009	Granted 16-Dec-2026

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SELECTIVE SCRAMBLER FOR USE IN A COMMUNICATION SYSTEM AND METHOD TO MINIMIZE BIT ERROR AT THE RECEIVER
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05101/ European Patent Convention	ORD	05021620.9 04-Oct-2005	1648128 19-Apr-2006		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SELECTIVE SCRAMBLER FOR USE IN A COMMUNICATION SYSTEM AND METHOD TO MINIMIZE BIT ERROR AT THE RECEIVER
Resp. Office: Austin

5104-05102/ Japan	ORD	2005-301432 17-Oct-2005			Pending

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 16855-B
Title: SELECTIVE SCRAMBLER FOR USE IN A COMMUNICATION SYSTEM AND METHOD TO MINIMIZE BIT ERROR AT THE RECEIVER
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05300/	ORD	11/421947	07/0280705	7912381	Granted
United States of America		02-Jun-2006	06-Dec-2007	22-Mar-2011	21-Oct-2029

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSION EFFICIENCY
Resp. Office: Austin

5104-05302/	ORD	07757128.9	0989802		Published
European Patent Convention		16-Feb-2007	12-Nov-2008		

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSION EFFICIENCY
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05303/ Japan	ORD	2008-555521 16-Feb-2007			Pending

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** 18242-B
Title: TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSION EFFICIENCY
Resp. Office: Austin

5104-05304/ Korea, Republic of	ORD	1020087022732 16-Feb-2007	08/0144739 31-Dec-2008		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** IP20081190/US
Title: TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSION EFFICIENCY
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05305/ China (Peoples Republic)	ORD	200780005794 16-Feb-2007	101385264 11-Mar-2009		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: Shanghai Patent & Trademark Law Office ***Agent Ref:*** USDM-0033
Title: TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSION EFFICIENCY
Resp. Office: Austin

5104-05307/ United States of America	DIV	12/961668 07-Dec-2010	11/0076014 31-Mar-2011	8103174 24-Jan-2012	Granted 02-Jun-2026

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSION EFFICIENCY
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05308/ China (Peoples Republic)	DIV	201110084988 16-Feb-2007	102176686 07-Sep-2011		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: Receiver Circuit, Transmitter Circuit and Communication Network
Resp. Office: Austin

5104-05309/ Japan	DIV	2011-158710 16-Feb-2007			Pending

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** 19291-B
Title: TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSION EFFICIENCY
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05310/ Japan	DIV	2012-006992 16-Feb-2007			Pending

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: TRANSMISSION NETWORK HAVING AN OPTICAL RECEIVER THAT UTILIZES DUAL POWER PINS AND A SINGLE STATUS PIN TO LOWER POWER CONSUMPTION, LOWER MANUFACTURING COST, AND INCREASE TRANSMISSION EFFICIENCY
Resp. Office: Austin

5104-05400/ United States of America	ORD	11/676001 16-Feb-2007	07/0255855 01-Nov-2007		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05402/ European Patent Convention	ORD	07757129.7 16-Feb-2007	1989847 12-Nov-2008		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** OA 2007/03 EP
Title: SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS
Resp. Office: Austin

5104-05403/ Japan	ORD	2008-555522 16-Feb-2007			Pending

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** 18241-B
Title: SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05404/ Korea, Republic of	ORD	1020087022734 16-Feb-2007	0102400 25-Nov-2008		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:*** IP20081191/US
Title: SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS
Resp. Office: Austin

5104-05405/ China (Peoples Republic)	ORD	200780005885 16-Feb-2007	101385294 11-Mar-2009	 07-Dec-2011	Granted 16-Feb-2027

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: Shanghai Patent & Trademark Law Office ***Agent Ref:*** USDM-0032
Title: SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5104-05406/ China (Peoples Republic)	DIV	201110138200 16-Feb-2007	102255796 23-Nov-2011		Published

Owner Name: ***Attorney(s):*** KLD
Client: OASIS SILICON SYSTEMS ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: SYSTEM AND METHOD FOR TRANSFERRING DIFFERENT TYPES OF STREAMING AND PACKETIZED DATA ACROSS AN ETHERNET TRANSMISSION LINE USING A FRAME AND PACKET STRUCTURE DEMARCATED WITH ETHERNET CODING VIOLATIONS
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5159-00100/ United States of America	ORD	12/360467 27-Jan-2009			Pending

Owner Name: ***Attorney(s):*** KLD
Client: SMSC Holdings S.a r.l. ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: Fault Tolerant Network Utilizing Bi-directional Point-to-Point Communications Links Between Nodes
Resp. Office: Austin

5159-00101/ United States of America	DIV				Unfiled

Owner Name: ***Attorney(s):*** KLD
Client: SMSC Holdings S.a r.l. ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: Fault Tolerant Network Utilizing Bi-directional Point-to-Point Communications Links Between Nodes
Resp. Office: Austin

5159-00102/ Patent Cooperation Treaty	PCT	PCTUS10000219 26-Jan-2010	10/098811 02-Sep-2010		Natl Phase

Owner Name: ***Attorney(s):*** KLD
Client: SMSC Holdings S.a r.l. ***Client Ref:***
Agent Name: ***Agent Ref:***
Title: Fault Tolerant Network Utilizing Bi-directional Point-to-Point Communications Links Between Nodes
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5159-00103/ Japan	ORD	2011-547972 26-Jan-2010			Pending

Owner Name: ***Attorney(s):*** KLD
Client: SMSC Holdings S.a r.l. ***Client Ref:***
Agent Name: YAMAKAWA Int'l Patent Office ***Agent Ref:*** 19290-B
Title: Fault Tolerant Network Utilizing Bi-directional Point-to-Point Communications Links Between Nodes
Resp. Office: Austin

5159-00104/ Korea, Republic of	ORD	1020117019985 26-Jan-2010			Pending

Owner Name: ***Attorney(s):*** KLD
Client: SMSC Holdings S.a r.l. ***Client Ref:***
Agent Name: Origin Int'l Patent & Law Firm ***Agent Ref:*** IP20111795/US
Title: Fault Tolerant Network Utilizing Bi-directional Point-to-Point Communications Links Between Nodes
Resp. Office: Austin

5159-00105/ European Patent Convention	ORD	10746522.1 26-Jan-2010			Pending

Owner Name: ***Attorney(s):*** KLD
Client: SMSC Holdings S.a r.l. ***Client Ref:***
Agent Name: Patentanwaltskanzlei Dr. Lohr ***Agent Ref:*** FIR 2011/01 EP
Title: Fault Tolerant Network Utilizing Bi-directional Point-to-Point Communications Links Between Nodes
Resp. Office: Austin

Docket No./Subcase Country Name	Case Type	Application Number/Date	Publication Number/Date	Patent Number/Date	Status Expiration Date
5159-00200/ United States of America	ORD	13/408431 29-Feb-2012			Pending

Owner Name:
Client: SMSC Holdings S.a r.l.
Agent Name:
Title: Flicker Reduction Algorithm
Resp. Office: Austin

Attorney(s): KLD
Client Ref:
Agent Ref: