

PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
	Name	Execution Date
	PANASONIC CORPORATION	12/26/2017
RECEIVING PARTY DATA		
Name:	TESSERA ADVANCED TECHNOLOGIES, INC.	
Street Address:	3025 ORCHARD PARKWAY	
City:	SAN JOSE	
State/Country:	CALIFORNIA	
Postal Code:	95134	
PROPERTY NUMBERS Total: 6		
Property Type	Number	
Application Number:	09345485	
Application Number:	10352070	
Application Number:	10820033	
Application Number:	10864814	
Application Number:	11004909	
Application Number:	11131385	
CORRESPONDENCE DATA		
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ATTORNEY DOCKET NUMBER:	ACQ-PANASONIC-3	
NAME OF SUBMITTER:	JENNIFER KOSTIC	
SIGNATURE:	/Jennifer Kostic/	
DATE SIGNED:	02/21/2018	
Total Attachments: 5		
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SCHEDULE B

**[TRANSFER DOCUMENTS]
DEED OF ASSIGNMENT**

THIS DEED OF ASSIGNMENT ("Assignment"), EFFECTIVE AS OF December 26, 2017, IS MADE BY AND BETWEEN

Panasonic Corporation, a Japanese corporation having a place of business at 1006 Oaza, Kadoma, Kadoma City, Osaka 571-8501, Japan (hereinafter "ASSIGNOR"); and

Tessera Advanced Technologies, Inc. (hereinafter "TATI"), a Delaware corporation having a place of business at 3025 Orchard Parkway, San Jose, California 95134, United States.

WHEREAS:

- A** **ASSIGNOR** is the sole owner in respect of the patents and patent applications listed in the attached Appendix (hereinafter "the **PATENTS**"); and
- B** **TATI** is desirous of acquiring all of the worldwide right, title and interest in and to the **PATENTS** and the inventions disclosed therein.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, **ASSIGNOR** has sold, assigned and transferred, and does hereby sell, assign and transfer to **TATI** all of the worldwide right, title and interest in (i) each of the patents and patent applications set forth in Schedule A, whether or not pending or issued, and all patentable inventions originally disclosed therein to the extent necessary to claim priority before the patent office in the relevant country, and (ii) all reissues, divisionals, continuations, continuations-in-part, reexaminations and foreign counterparts thereof, and all other patents and patent applications that claim priority to patents or patent applications listed in Schedule A (iii), all rights corresponding to any of the foregoing throughout the world (including the right to claim the priority date of any of the **PATENTS** and the right to sue for and recover damages for any past, present or future infringement of the Patents), the same to be held and enjoyed by **TATI** for its own use and enjoyment, and for the use and enjoyment of its successors, assigns and other legal representatives, to the end of the term or terms of said **PATENTS** granted or reissued or reexamined as fully and entirely as the same would have been held and enjoyed by **ASSIGNOR**, if this assignment and sale had not been made.

IN WITNESS WHEREOF, **ASSIGNOR** has caused these presents to be signed by its duly appointed trustee having full authority to convey its property; and **TATI** has caused these presents to be signed by its duly appointed trustee.

And if the issue date and/or patent number of any of the **PATENTS** is unknown to **ASSIGNOR** and **TATI** at the time this Assignment is executed, **ASSIGNOR** does hereby authorize its attorneys to insert on this Assignment the issue date and patent number of said any patent when known.

ASSIGNOR hereby declares that **TATI** may take the steps for recordal of this assignment in the sole name of **TATI**.

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EXECUTION VERSION

ASSIGNOR hereby undertakes that it shall, without further consideration, but at the expense of TATI, execute all documents and do all such acts and things as TATI may in its absolute discretion consider necessary or desirable to enable Letters Patent or any other form of protection to be issued in respect of any of said PATENTS and the patentable inventions originally disclosed therein.

SIGNED for and on behalf of,

ASSIGNOR

by

(Signature)

on

(Date)

Hiroki Nishida Authorized signing officer
(Print Name and Title)

County of Japan

On this 26th day of December, 2017 before me, Yuji Kusakawa, personally appeared Hiroki Nishida, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

SIGNED for and on behalf of

TATI

by

(Signature)

on

(Date)

Paul Davis, SVP and
(Print Name and Title) General Counsel

SCHEDULE A
ASSIGNED PATENTS

A-1. United States Listed Issued Patents and Pending Patent Applications

US Issued Patents

Patent Number	Filing Date	Application Number	Issue Date	Publication Number	Title
6532581	07/01/1999	09/345,485	03/11/2003		Method for designing layout of semiconductor device, storage medium having stored thereon program for executing the layout designing method, and semiconductor device
7038962	12/07/2004	11/004,909	05/02/2006	20050128844	Semiconductor integrated circuit
7038967	06/10/2004	10/864,814	05/02/2006	20050052923	Semiconductor apparatus capable of performing refresh control
7072241	05/18/2005	11/131,385	07/04/2006	20050205983	Semiconductor memory device and multi-chip module comprising the semiconductor memory device
7312649	04/08/2004	10/820,033	12/25/2007	20040207458	Voltage booster power supply circuit

US Pending Applications

None.

A-2. Foreign Listed Issued Patents and Pending Patent Applications

Foreign Issued Patents

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
4158856	JP	04/17/2003	2003-112248	07/25/2008	2004-319011	Voltage booster power supply circuit
4211922	JP	06/13/2003	2003-169826	11/07/2008	2005-4929	Semiconductor device
4598470	JP	10/01/2004	2004-289874	10/01/2010	2005-101620	Semiconductor device

CONFIDENTIAL

EXECUTION VERSION

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
ZL200410035047.8	CN	04/19/2004	200410035047.8	04/28/2010	1538453	Booster power circuit

Foreign Pending Applications

None.

A-3. US and Foreign Listed Abandoned/Expired Patents and Applications

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
	US	01/28/2003	10/352,070		20030156442	Semiconductor memory device and multi-chip module comprising the semiconductor memory device
	CN	12/15/2004	200410101954.8		1629981	Semiconductor integrated circuit
	JP	07/03/1998	10-188696			
	JP	06/28/1999	11-182181		2000-82093	Semiconductor device and its layout design method and recording medium recording layout design program
4054200	JP	02/19/2002	2002-41108	12/14/2007	2003-242774	Semiconductor memory device and multi-chip module
	JP	12/15/2003	2003-415831		2005-174504	Semiconductor integrated circuit

A-4. Foreign Listed Patents and Applications – Status Unknown

None

The maintenance status of all US Assigned Patents listed above is as reported by the United States Patent and Trademark Office ("USPTO") as of the Effective Date of this Agreement. Such status information is available on the USPTO "Public Patent Application Information Retrieval" website. The maintenance status of all foreign counterpart Assigned Patents listed above is available directly from the patent authorities of the foreign jurisdictions in which such foreign counterpart Assigned Patents have been registered. Purchaser accepts the maintenance status of the Assigned Patents as being that reported by the patent authorities noted above and has

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thus been made aware of the maintenance status of the Assigned Patents with regard to those that have lapsed, expired, been reinstated, and for which the fee window is open as of the Effective Date. No other representations about the maintenance status of the Assigned Patents is made herein no matter what jurisdiction is associated with the Assigned Patent in question.