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CONVEYING PARTY DATA

Name	Execution Date
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PROPERTY NUMBERS Total: 2

Property Type	Number
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Application Number:	15815267

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ELLIS TERRY

Ali Abdolkhani

POWERBYPROXI LIMITED

ASSIGNMENT OF INTELLECTUAL PROPERTY RIGHTS

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PARTIES

Ali Abdolkhani, an Iran citizen of c\-111 Franklin Road, Freemans Bay, Auckland, 1011, New Zealand **(Assignor)**

PowerbyProxi Limited, a New Zealand company (No. 1967622) whose registered office is located at **111** Franklin Road, Freemans Bay, Auckland, **1011**, New Zealand **(Assignee)**

INTRODUCTION

A. The Assignor has devised or contributed to the Invention either during the course of employment with the Assignee or under a commission from the Assignee.

B. The Assignor acknowledges that the Assignee is or should be the legal and beneficial owner of the Invention and the Intellectual Property Rights.

C. The Assignor has agreed to assign the Invention, the Know How and the Intellectual Property Rights to the Assignee subject to the terms and conditions of this assignment.

COVENANTS

1. DEFINITIONS

1.1 In this assignment, including the Introduction, the following terms will have the following meanings:

Copyright means:

(a) all copyrights and all rights in the nature of copyright, in any original artistic, literary and other works; and

(b) any database rights,

comprising or relating to the Invention, that exist or may in the future exist anywhere in the world;

Design Rights means all rights in and to the designs to be applied to articles of, or relating to, the Invention, that exist or may in the future exist anywhere in the world including, but not limited to:

(a) the right to apply for and obtain protection for such designs in relation to such articles and the rights conferred by such protection when granted;

(b) the right to claim priority under any international convention or agreement, including the Paris Convention (as amended), from any such application referred to in paragraph (a) above;

(c) all unregistered design rights arising from the Invention; and

(d) all semi-conductor topography or integrated circuit layout rights arising from the Invention;

Improvement means an improvement in, modification of, or addition to:

(a) the Invention;

(b) any original artistic, literary or other works relating to the Invention; or

(c) any designs to be applied to articles of or relating to the Invention,

devised, created, designed, contributed to or acquired by the Assignor, while the Assignor is employed by the Assignee, or under any commission from the Assignee;

Intellectual Property Rights means all industrial and intellectual property rights (whether protectable by statute, at common law or in equity) in and to the Invention that exist or may in the future exist anywhere in the world and whether or not registered or registrable, including the Patent Rights, Copyright and Design Rights;

Invention means any and all inventions described in the Schedule (as improved, modified, developed or amended at any time before execution of this assignment by the Assignor);

Know-How means any information, knowledge, experience, data and designs in the possession of the Assignor that are confidential and that relate to the invention or the process for making or using it; and

Patent Applications means the patent applications identified in the Schedule; and

Patent Rights means all patent rights in and to the Invention that exist or may in the future exist anywhere in the world including, but not limited to:

(a) the right to apply for and obtain patents or other similar forms of protection for the Invention in any country;

(b) the right to claim priority under any international convention or agreement, including the Paris Convention (as amended) from any application referred to in paragraph (a) above;

(c) all rights conferred by any patents or similar forms of protection obtained from any applications referred to in paragraphs (a) and (b) above and

(d) the Patent Applications together with:

(i) any patents that may be granted pursuant to the Patent Applications; and

(ii) any future patent(s) and patent application(s) that are based on or derive priority from or have equivalent claims to the Patent Applications in any country in the world (including divisionals, continuations, continuations in part, patents of addition, supplementary protection certificates, reissues, extensions, innovation patents, utility models and petty patents).

2. ASSIGNMENT

2.1 **Assignment:** In consideration of the sum of NZ$1.00 paid by the Assignee to the Assignor, the receipt and sufficiency of which is hereby acknowledged by the Assignor, the Assignor assigns to the Assignee absolutely all of the Assignor's rights, title and interest in and to:

(a) the Invention;

(b) the Intellectual Property Rights; and

(c) the Know-How, including:

(i) the exclusive and worldwide right to use, copy, modify and disclose the Know-How for any purpose whatsoever; and

(ii) the right to file patent and design applications over any part of the Know-How.

2.2 **Rights of action:** The assignments effected by clause 2.1 include:

(a) the assignment and transfer of:

(i) the right to sue for damages for infringement or misuse of the Intellectual Property Rights; and

(ii) all other rights of action, powers, legal and equitable remedies, and benefits arising from ownership of the Intellectual Property Rights,

in relation to all causes of action arising before, on or after the date of this assignment; and

(b) the assignment and transfer of any materials that form part of the Know-How.

2.3 **Moral rights:** The Assignor:

(a) waives all of the Assignor's moral rights arising from the Invention throughout the world; and

(b) consents to all uses and treatments of the Invention and the Intellectual Property Rights,

to the extent that the Assignor may lawfully do so.

2.4 **Authority to add application particulars:**

(a) The Assignor acknowledges that it is the intention of the Assignee to file one or more patent applications in various countries around the world in respect of the Invention. The Assignor hereby irrevocably authorises the Assignee or its agent to add in the Schedule particulars of any patent applications in respect of the Invention that may be filed following the date of execution by the Assignor of this assignment.

(b) The Assignor agrees and acknowledges that any addition under clause 2.4(a) will be valid and binding upon the Assignor as if the addition had been made prior to execution by the Assignor of this assignment.

3. KNOW-HOW

3.1 The Assignor will, at the request of the Assignee and to the extent it has not already done so:

(a) disclose all Know-How to the Assignee in writing;

(b) provide all other reasonable assistance and information that may be reasonably necessary to assist the Assignee, or its nominee, to develop and to make or use the Invention; and

(c) where possible, provide all original versions of the Invention and any materials that form part of the Know-How.

4. CONFIDENTIALITY

4.1 **Confidentiality obligations:** The Assignor agrees to treat all information relating to the Invention, the Know-How and the Intellectual Property Rights as secret and confidential. The Assignor will not use, disclose or publish such information without the Assignee's prior written consent.

4.2 **Exceptions to confidentiality:** The obligations of confidentiality in clause 4.1 do not extend to any information that is or becomes generally available to the public through no act or default of the Assignor.

However, the Assignor will promptly advise the Assignee if the Assignor becomes aware of any actual or potential loss of secrecy or confidentiality of the information referred to in clause 4.1.

5. IMPROVEMENTS

5.1 **Disclosure:** The Assignor will immediately disclose to the Assignee all Improvements as and when such Improvements arise.

5.2 **Ownership of Improvements:**

(a) The Assignee will exclusively own all Improvements and all intellectual property rights in those Improvements.

(b) If any Improvements or intellectual property rights in those improvements are not owned by the Assignee on their creation but are owned by the Assignor, the Assignor will hold those Improvements and intellectual property rights on trust for the Assignee.

(c) The Assignor will at any time reasonably requested by the Assignee, and at the Assignee's expense, appropriately execute all documents necessary to:

(i) confirm the Assignee's ownership of the Improvements and all intellectual property rights in those Improvements; or

(ii) file, prosecute and defend any protective application for the Improvements and all intellectual property rights in those Improvements.

6. EXECUTION OF DOCUMENTS AND FURTHER ACTIONS

6.1 **Further actions:** If requested by the Assignee the Assignor will, at the Assignee's expense, execute all documents, give such assistance and do all other acts and things that the Assignee considers necessary or desirable to:

(a) apply for and obtain, or (if the Assignee thinks fit) join with the Assignee in applying for and obtaining, protection of the Intellectual Property Rights. The Assignor acknowledges that all rights, title and interest in and to such applications and any granted protection will be owned by the Assignee;

(b) vest in the Assignee ownership of any protection referred to in paragraph (a) above;

(c) amend, maintain, or renew any protection referred to in paragraph (a);

(d) enforce any of the Intellectual Property Rights (including by obtaining any remedies that may be available for infringement of the Intellectual Property Rights);

(e) defeat any challenge to the validity of any of the Intellectual Property Rights;

(f) defend any opposition proceedings brought by a third party in relation to the Intellectual Property Rights;

(g) conduct opposition proceedings regarding any application for intellectual property protection by a third party, where such application may adversely affect the Assignee's ability to exploit the Intellectual Property Rights; and

(h) otherwise implement and carry out the Assignor's obligations under this assignment.

6.2 **Recordal:** The Assignor authorises and requests the Commissioner of Patents and Trademarks of the United States, and any official of any other country or state, whose duty it is to issue patents, to issue the same to the Assignee in accordance with this assignment.

6.3 **Power of attorney:** The Assignor irrevocably appoints the Assignee as the Assignor's attorney with full power to act in the Assignor's name and on the Assignor's behalf to do any of the things required to be done by the Assignor under clause 6.1 and 6.2:

(a) to the extent that the Assignor fails to do any of those things within a reasonable time after being called upon to do so by the Assignee; or

(b) if the Assignee is unable, after making reasonable and proper inquiries, to locate the Assignor to ask the Assignor to do those things.

7. GENERAL

7.1 **Assignment binding and delivered:** this assignment:

(a) is intended to be immediately and unconditionally binding upon the Assignor as soon as the Assignor executes and delivers this assignment; and

(b) without limiting any other mode of delivery, will be delivered by the Assignor immediately upon the earlier of:

(i) physical delivery of an original form of this assignment executed by the Assignor; or

(ii) transmission (whether by facsimile or email) of a copy of this assignment executed by the Assignor,

to the Assignee or its solicitor, patent attorney, or agent.

7.2 **Waiver:** No failure or delay by any party in exercising any right, power or privilege under this assignment will operate as a waiver of such right, power or privilege, nor will any single or partial exercise preclude any other or further exercise of any right, power or privilege under this assignment.

7.3 **Counterparts:**

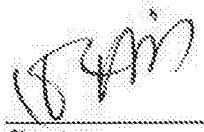
(a) This assignment may be executed in any number of counterparts (including facsimile or electronically scanned copies) all of which, when taken together, will constitute one and the same instrument.

(b) A party may enter into this assignment by executing any counterpart. The parties acknowledge that this assignment may be executed on the basis of an exchange of facsimile or electronically scanned copies and confirm that their respective execution of this assignment by such means will be a valid and sufficient execution.

7.4 **Governing law:** The formation, validity, construction and performance of this assignment will be governed by and construed in accordance with the laws of New Zealand. The parties irrevocably agree that the Courts of New Zealand will have non-exclusive jurisdiction to hear and determine all disputes under or in connection with this assignment. The parties irrevocably waive any objections to New Zealand as the forum for proceedings on the grounds of forum non-conveniens or any similar grounds.

SIGNED

Ali Abdolkhani in the presence of:



Signature

18 Nov 2016 NZDT

Date

WITNESS

Signature:

Name: GEOFF CHISLETT

Address: AUCKLAND

Occupation: PLUMBER

SCHEDULE

INVENTION

The invention entitled "INDUCTIVE POWER RECEIVER" described in the specification sent to the Assignee by email dated 18 November 2016 New Zealand Daylight Time.

INDUCTIVE POWER RECEIVER

FIELD OF THE INVENTION

This invention is in the field of inductive power transfer (IPT). More particularly, the invention relates to receivers for use in IPT systems.

BACKGROUND OF THE INVENTION

Electrical converters are found in many different types of electrical systems. Generally speaking, a converter converts a supply of a first type to an output of a second type. Such conversion can include DC-DC, AC-AC and DC-AC electrical conversions. In some configurations a converter may have any number of DC and AC 'parts', for example a DC-DC converter might incorporate an AC-AC converter stage in the form of a transformer.

One example of the use of converters is in inductive power transfer (IPT) systems. IPT systems are a well-known area of established technology (for example, wireless charging of electric toothbrushes) and developing technology (for example, wireless charging of handheld devices on a 'charging mat').

IPT systems will typically include an inductive power transmitter and an inductive power receiver. The inductive power transmitter includes a transmitting coil or coils, which are driven by a suitable transmitting circuit to generate an alternating magnetic field. The alternating magnetic field will induce a current in a receiving coil or coils of the inductive power receiver. The received power may then be used to charge a battery, or power a device or some other load associated with the inductive power receiver. Further, the transmitting coil and/or the receiving coil may be connected to a resonant capacitor to create a resonant circuit. A resonant circuit may increase power throughput and efficiency at the corresponding resonant frequency.

Typically, receivers used in IPT systems consist of a power receiving coil and a circuit topology configured to convert the induced power from AC to DC and to regulate the voltage of the power ultimately provided to a load.

A common problem with receivers used in IPT systems is that switched-mode regulators may include a DC inductor. The DC inductor acts as an energy store so that power can be suitably regulated. Such DC inductors can be a bulky circuit component, significantly affecting the total size occupied by the receiver. This can be a particular problem in applications where it is preferable that the receiver be as small as possible (for example, receivers used with mobile devices).

Another problem with known receivers is that they can include a substantial number of components. For switched-mode regulators this can include multiple switches. This adds to the bulk and complexity, and ultimately cost, of the receiver. As there is a growing desire to adopt IPT systems in consumer devices (such as smartphones), such increased bulk, complexity and cost presents a barrier to wide spread adoption that needs to be minimised.

It is therefore an object of the invention to provide a receiver for an IPT system that minimises component count, of at least provides the public with a useful choice.

SUMMARY OF THE INVENTION

According to one exemplary embodiment there is provided an inductive power receiver, comprising: a receiving coil; a bridge circuit configured to connect to the receiving coil comprising: a first branch including a first semiconductor device; a second branch including a second semiconductor device; a third branch including a first capacitor; and a forth branch including a second capacitor, and a controller configured to control at least one of the first semiconductor device and the second semiconductor device to regulate power provided to a load.

It is acknowledged that the terms "comprise", "comprises" and "comprising" may, under varying jurisdictions, be attributed with either an exclusive or an inclusive meaning. For the purpose of this specification, and unless otherwise noted, these

terms are intended to have an inclusive meaning—i.e. they will be taken to mean an inclusion of the listed components which the use directly references, and possibly also of other non-specified components or elements.

Reference to any prior art in this specification does not constitute an admission that such prior art forms part of the common general knowledge.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings which are incorporated in and constitute part of the specification, illustrate embodiments of the invention and, together with the general description of the invention given above, and the detailed description of embodiments given below, serve to explain the principles of the invention.

Figure 1 shows a block diagram of an IPT system;

Figures 2 shows a circuit diagram for a receiver topology according to one embodiment of the present invention;

Figures 3A to 3C show effective circuit diagrams corresponding to the different stages of operation of the receiver of Figure 2 according to one embodiment;

Figure 4 shows a block diagram of a controller according to one embodiment of the present invention;

Figure 5 shows a timing diagram corresponding to a control strategy according to one embodiment of the present invention;

Figures 6A to 6B show circuit diagrams for receiver topologies according to further embodiments of the present invention;

Figure 7 shows a circuit diagram for a receiver topology according to one embodiment of the present invention;

Figures 8A to 8C show effective circuit diagrams corresponding to the different stages of operation of the receiver of Figure 7 according to one embodiment; and

Figure 9 shows a circuit diagram for a receiver topology according to a further embodiment of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

An inductive power transfer (IPT) system 1 is shown generally in Figure 1. The IPT system includes an inductive power transmitter 2 and an inductive power receiver 3. The inductive power transmitter 2 is connected to an appropriate power supply 4 (such as mains power or a battery). The inductive power transmitter 2 may include transmitter circuitry having one or more of a converter 5, e.g., an AC-DC converter (depending on the type of power supply used) and an inverter 6, e.g., connected to the converter 5 (if present). The inverter 6 supplies a transmitting coil or coils 7 with an AC signal so that the transmitting coil or coils 7 generate an alternating magnetic field. In some configurations, the transmitting coil(s) 7 may also be considered to be separate from the inverter 5. The transmitting coil or coils 7 may be connected to capacitors (not shown) either in parallel or series to create a resonant circuit.

A controller 8 may be connected to each part of the inductive power transmitter 2. The controller 8 may be adapted to receive inputs from each part of the inductive power transmitter 2 and produce outputs that control the operation of each part. The controller 8 may be implemented as a single unit or separate units, configured to control various aspects of the inductive power transmitter 2 depending on its capabilities, including for example: power flow, tuning, selectively energising transmitting coils, inductive power receiver detection and/or communications.

The inductive power receiver 3 includes a power pick up stage 9 connected to power conditioning circuitry 10 that in turn supplies power to a load 11. The power pick up stage 9 includes inductive power receiving coil or coils 13. When the transmitting coil(s) 7 of the inductive power transmitter 2 and the receiving coil(s) 13 inductive

power receiver 3 are suitably coupled, the alternating magnetic field generated by the transmitting coil or coils 7 induces an alternating current in the receiving coil or coils 13. The receiving coil or coils 13 may be connected to capacitors (not shown) either in parallel or series to create a resonant circuit. Some inductive power receivers may include a controller 12 which may control tuning of the receiving coil or coils 13, operation of the power conditioning circuitry 10 and/or communications.

The term "coil" may include an electrically conductive structure where an electrical current generates a magnetic field. For example inductive "coils" may be electrically conductive wire in three dimensional shapes or two dimensional planar shapes, electrically conductive material fabricated using printed circuit board (PCB) techniques into three dimensional shapes over plural PCB 'layers', and other coil-like shapes. Other configurations may be used depending on the application. The use of the term "coil", in either singular or plural, is not meant to be restrictive in this sense.

Referring to Figure 2, there is shown an inductive power receiver 200 for use in an IPT system according to an example embodiment of the present invention. The receiver includes a receiving coil 202. The receiving coil 202 is connected between the branches of a bridge circuit 204 (which in this embodiment is an H-bridge circuit). The bridge circuit 204 comprises four branches: a first branch 206 and a second branch 208 stemming from one end of the receiving coil 202; and a third branch 210 and a fourth branch 212 stemming from the other end of the receiving coil 202.

The first branch 206 includes a first semiconductor device 220 (which in this embodiment is a semiconductor switch) and the second branch includes a second semiconductor device 222 (which in this embodiment is a diode). The semiconductor switch is a low-side controlled switch. In one embodiment, the semiconductor switch may be a MOSFET switch.

The third branch 110 includes a first capacitor 224 and the fourth branch 212 includes a second capacitor 226. In this embodiment, the first capacitor 224 and

second capacitor 226 provide resonance to the receiving coil 202. The values of the receiving coil 202 and the capacitors 224 226 will impact the resonant frequency of the receiver 200. Therefore, the receiving coil 202 and the capacitors 224 226 may be selected so as to resonate at the operating frequency of at the operating frequency of the IPT system.

The bridge circuit 204 is connected to a load 214. The load 214 may be any suitable load, such as the battery charging circuit of a mobile device. The load 214 is connected in parallel to a smoothing capacitor 216. Finally, the receiver 200 includes a controller 218 (represented as a block). As will be described in more detail below, the controller is configured to control at least one of the first semiconductor device 220 and the second semiconductor device 222 to regulate the power provided to the load 214.

Having described an example embodiment of the topology of the present invention, its operation will be described, with reference to Figures 3A to 3C. Upon the inductive power receiver 200 being suitably coupled with an inductive power transmitter, an AC voltage will be induced across the receiving coil 202 such that the receiving coil acts as an AC voltage source.

A first half cycle is shown in Figure 3A. During the first half cycle, current I_s flows though the receiving coil 202 from the semiconductor switch 220 to the first and second capacitors 224 226. The semiconductor switch 220 is shown as closed, thereby permitting current flow through the first branch 206. However, it will be appreciated that even if the semiconductor switch 220 were open current would flow as shown in Figure 3A due to the semiconductor switch's body diode (not shown). Conversely, the orientation of the diode 222 prevents current flow through the second branch 208. Power is supplied to the load 214 (and the smoothing capacitor 216 is charged).

A second half cycle is shown in Figures 3B and 3C, in which current I_s flows through the receiving coil 202 in the reverse direction. If the voltage across the load (V_{load}) is higher than a specified reference voltage (V_{ref}), then the semiconductor switch is

controlled so that the switch is closed for an interval t_{2a}, as shown in Figure 3B. Since the semiconductor switch 220 is closed, current flows through the first branch 206, and 're-circulated' through the first capacitor 224 and the smoothing capacitor 216. As a result, power from the receiving coil 202 is effectively not supplied to the load 216.

Once interval t_{2a} has elapsed, the semiconductor switch is controlled so that the switch is open, as shown in Figure 3C. Since the semiconductor switch 220 is open, current flow though the first branch 206 is prevented. As a result current flows through the second branch 208 (the orientation of the diode 222 being such that current flow is now permitted) and power is supplied to the load 214.

Thus, by controlling whether semiconductor switch 220 is open or closed during the second half cycle, it is possible to control whether power is supplied to the load (Figure 3C) or not (Figure 3B), thereby regulating the power provided to the load. It will also be appreciated that the output provided to the load 214 is DC. Therefore, the proposed topology achieves both regulation and rectification with one stage. This eliminates that need for distinct rectification and regulation stages, thereby minimising component count and cost.

Another feature shown by Figures 3A to 3C, is that for the first cycle and the first part of the second cycle (Figures 3A and 3B) the first capacitor 224 is in parallel with the receiving coil 202 and the second capacitor 226 and the smoothing capacitor 216 are in parallel with the receiving coil 202. Provided the smoothing capacitor 216 is relatively large compared to the first capacitor 224 and the second capacitor 226, then analysis of the parallel capacitance shows that the resulting capacitance is simply the sum of the capacitances of the first capacitor 224 and the second capacitor 226. By the same analysis as above, for the second part of the second cycle (Figure 3C) the resulting capacitance is simply the sum of the capacitance of the first capacitor 224 and the second capacitor 226. Therefore, the resonance of the receiver 200 for the full cycle is determined by the first capacitor 224 and the second capacitor 226 (and the receiving coil 202). As such, the proposed topology shown in

this embodiment does not need a separate resonant capacitor to satisfy the requirement for resonance, further minimising component count and cost.

Figure 4 shows an example embodiment of a controller 218, suitable for controlling the semiconductor switch 220 in the receiver 200 described in relation to Figures 2 to 3C above. The controller 218 includes a comparator 402, which compares V_{load} with V_{ref}. The output of the comparator is connected to a PID controller 404, which generates a DC signal proportional to the difference between V_{load} and V_{ref}. The controller also includes a phase detection module 406 for detecting the phase of the receiving coil current I_s (for example by detecting the zero points of I_s). It will be appreciated that other parameters of the circuit may be used to determine phase, for example, voltage. The output of the phase detection module 406 is supplied to an in-phase ramp generator 408, which generates a ramp signal in phase with the receiving coil current I_s. The DC signal is compared to the output of the ramp signal by a further comparator 410, generating a switch control signal. The switch control signal is then supplied to the semiconductor switch 220, thereby controlling the switch to achieve the regulation described in relation to Figures 3B and 3C.

Figure 5 illustrates a timing diagram corresponding to the control strategy described in relation to Figures 3A to 3C and the controller 218 described in Figure 4. The timing diagram shows the AC receiving coil current I_s and the resulting output of the phase detection module 504. During the first half cycle t_1, since the receiving coil current I_s is negative, the output of the phase detection module 504a is zero, and therefore the ramp signal 506a is also zero. In Figure 5, during the first half cycle t_1, the DC signal 508a is a non-zero value. Since the DC signal 508a is greater than the ramp signal 506a, the switch control signal is ON, therefore the semiconductor switch 220 is closed, as is shown in Figure 3A.

During the second half cycle t_2, since the receiving coil I_s is positive, the output of the phase detection module 504b is non-zero, and therefore the ramp signal 506b begins to ramp upwards. During the first part of the second half cycle t_{2a}, since the DC signal 508b is greater than the ramp signal 506b, the switch control signal is ON.

Therefore, the semiconductor switch 220 is closed resulting in current re-circulation, as described in relation to Figure 3B. However, once the ramp signal 506c is greater than the DC signal 508c (i.e. during the second part of the second half cycle t_{2b}), the switch control signal is OFF. Therefore, the semiconductor switch 220 is opened, resulting in current being provided to the load, as described in relation to Figure 3C.

It will be appreciated from Figure 5 that the amount of energy recirculation is related to the proportion of the second half cycle t_2 of which the semiconductor switch 220 is closed (i.e. interval t_{2a}). The duration of interval t_{2a} (and therefore the amount of energy recirculation) is dependent on the relative magnitude of the DC signal compared to the amplitude of the ramp signal. Thus, if the DC signal is relatively small compared to the amplitude of the ramp signal, then this would result in a relatively short interval t_{2a} and a smaller amount of energy recirculation. Conversely, if the DC signal is similar to or larger than the amplitude of the ramp signal (indicating that V_{out} is higher than V_{ref}), then this would result in a relatively long interval t_{2a}. This would give a larger amount of energy recirculation, as is needed since V_{out} is higher than V_{ref}. The controller 218 can therefore be calibrated so as to achieve the desired amount of energy recirculation for the particular receiver 200. The controller 218 may be calibrated by adjusting the relative amplitudes of the DC signal and the ramp signal. In one embodiment, the controller 218 may be configured such that for full load conditions, interval t_{2a} is essentially zero (i.e. the semiconductor switch 220 would operate at 50% duty cycle), and under no load conditions, interval t_{2a} equals t_1 (i.e. the semiconductor switch 220 would operate at 100% duty cycle).

It will also be appreciated from Figure 5, that the semiconductor switch 220 is closed (i.e. that switch signal is ON) when the current through the semiconductor switch 220 is zero. This results in zero-current switching and minimised losses.

In another embodiment of the receiver 200 described in relation to Figures 2 to 5, the diode 222 may be replaced by a further semiconductor switch. The further semiconductor switch would need to be controlled such that it is closed during

interval t_{2b} (permitting current flow through the second branch 208, as shown in Figure 3C) and open at all other times (preventing current flow through the second branch, as shown in Figure 3A). Such operation could be achieved using a signal that is the negation of the switch control signal. Such a signal is also shown on Figure 5.

In another variation of the inductive power receiver 200 shown in Figure 2, the receiving coil 202 may be connected with a dedicated resonant capacitor. Figure 6A shows an embodiment in which the receiving coil 202 is connected in parallel with a resonant capacitor 228. A benefit of this embodiment is that the smoothing capacitor is eliminated, with the first capacitor 224 and second capacitor 226 acting as smoothing capacitors. Figure 6B shows another embodiment in which the receiving coil is connected as part of an LCL topology including a resonant capacitor 228 and a further inductor 230. Again, the first capacitor 224 and second capacitor 226 act as smoothing capacitors, eliminating the need for a separate smoothing capacitor.

In a further variation of the inductive power receiver 200 shown in Figure 2, the first branch 206 may include a further semiconductor switch connected in series with the semiconductor switch 220. The further semiconductor switch may be orientated such that its body diode is opposite to the body diode of the semiconductor switch 220. The combination of switches in the first branch 206 can then be controlled using an open circuit control strategy during the first part of the cycle.

Figure 7 shows another embodiment of the receiver 200 in which the receiving coil 202 is connected in series with a resonant capacitor 228. The first branch 206 includes a further diode 232 connected in series with the first semiconductor switch 220. It should be noted that the polarity of the first semiconductor switch 220 has been reversed (as compared to the embodiment described in relation to Figure 2). It will be appreciated that the further diode 232 prevents current flow in the reverse direction through the first branch 206, thereby effecting the operation of the circuit, as will be described with reference to Figures 8A to 8C.

A first half cycle is shown in Figures 8A and 8B. During the first half cycle, current I_s flows though the receiving coil 202 from the semiconductor switch 220 to the second capacitor 226. The semiconductor switch 220 is controlled so that the switch is closed for an interval t_{1a}, as shown in Figure 8A. Since the semiconductor switch 220 is closed, current is permitted to flow through the first branch 206. The orientation of the diode 222 prevents current flow through the second branch 208. Power is supplied to the load 214.

If the voltage across the load (V_{load}) is higher than a specified reference voltage (V_{ref}), then the semiconductor switch 220 is controlled so that the switch is open for an interval t_{1b}, as shown in Figure 8B. This prevents current flow through the first branch and the receiving coil 202, and no power is supplied to the load. It will be appreciated that the orientation of the semiconductor switch 220 is such that switch's body diode (not shown) also prevents current flow.

A second half cycle is shown in Figure 8C, in which current I_s flows through the receiving coil 202 in the reverse direction. Current flows through the second branch 208 and power is provided to the load 214. The semiconductor switch 220 is shown as open. However, it will be appreciated that even if the semiconductor switch 220 were closed current would not flow on account of the further diode 232.

Thus, by controlling whether semiconductor switch 220 is open or closed during the first half cycle, it is possible to control whether power is supplied to the load (Figure 8A) or not (Figure 8B), thereby regulating the power provided to the load. Those skilled in the art how the controller of Figure 4 may be adapted to implement the power control strategy described in relation to Figures 8A to 8C.

In yet a further variation of the inductive power receiver 200 shown in Figure 2, the third branch 210 may include a further semiconductor switch connected in parallel with the first capacitor 224. The further semiconductor switch can then be controlled so as to achieve closed circuit control during the first part of the cycle by selectively shorting the receiving coil 202.

Figure 9 shows a further variation of the receiver 200 shown in Figure 2. In some embodiments, it may be desirable to have less current flowing through the receiving coil 202 (for example, under light load conditions when the power demand is low). To decrease the current, the receiver 200 may include a detuning network 230. The detuning network 230 is configured to allow the receiving coil 202 to be selectively detuned, thereby decreasing the amount of power received by the receiving coil 202 and the current provided to the load 214. For example, the detuning network may comprise a detuning component (e.g. a capacitor or an inductor) connected in parallel with a detuning switch. Such a detuning network may be positioned in series with other components in the receiver 200 (for example, the first capacitor 224 in the third branch 210 or the receiving coil 202 itself). In the embodiment shown in Figure 6, the detuning network comprises a detuning capacitor 232 connected in parallel with a detuning switch 234. The detuning network 230 is part of the third branch and connected in series with the first capacitor 224. Under normal operations, the detuning switch is closed. However, when the detuning switch is closed, the detuning component is introduced into the resonant circuit and the receiving coil 202 is detuned, reducing the current through the load. The switch may be controlled by a controller, configured to detect the current through the load 214, and open or close the detuning switch accordingly. For example, if the load current falls below a particular threshold, the detuning switch may be opened to detune the receiving coil and decrease the current provided to the load. One particular advantage of a detuning network is that upon startup of the receiver 200, the receiving coil 202 can be initially detuned, limiting the current supplied to the load, which eliminates the possibility of voltage overshoots. Once the power demand exceeds a certain threshold, the receiving coil may then be tuned so that the power demand can be met.

While the present invention has been illustrated by the description of the embodiments thereof, and while the embodiments have been described in detail, it is not the intention of the Applicant to restrict or in any way limit the scope of the appended claims to such detail. Additional advantages and modifications will readily appear to those skilled in the art. Therefore, the invention in its broader aspects is

not limited to the specific details, representative apparatus and method, and illustrative examples shown and described. Accordingly, departures may be made from such details without departure from the spirit or scope of the Applicant's general inventive concept.

CLAIMS

1. An inductive power receiver, comprising:

    a. a receiving coil;

    b. a bridge circuit configured to connect to the receiving coil comprising:

        i. a first branch including a first semiconductor device;

        ii. a second branch including a second semiconductor device;

        iii. a third branch including a first capacitor; and

        iv. a forth branch including a second capacitor, and

    c. a controller configured to control at least one of the first semiconductor device and the second semiconductor device to regulate power provided to a load.

2. The inductive power receiver as claimed in claim 1, wherein the first semiconductor device is a first semiconductor switch.

3. The inductive power receiver as claimed in claim 2, wherein the second semiconductor device is a diode.

4. The inductive power receiver as claimed in any one of claims 1 to 2, wherein the second semiconductor device is a second semiconductor switch.

5. The inductive power receiver as claimed in any preceding claim, wherein the receiver includes a smoothing capacitor connected in parallel across the load.

6. The inductive power receiver as claimed in any preceding claim, wherein the bridge circuit is an H-bridge circuit.

7. The inductive power receiver as claimed in any preceding claim, wherein the receiving coil is connected to a resonant capacitor.

8. The inductive power receiver as claimed in claim 7, wherein the resonant capacitor is connected in series with the receiving coil.

9. The inductive power receiver as claimed in any preceding claim, wherein the first branch includes a further semiconductor switch connected in series with the first semiconductor switch.

10. The inductive power receiver as claimed in any preceding claim, wherein the receiver includes a detuning network, comprising a detuning component and a detuning switch, the detuning switch controlled so as to detune to receiving coil.

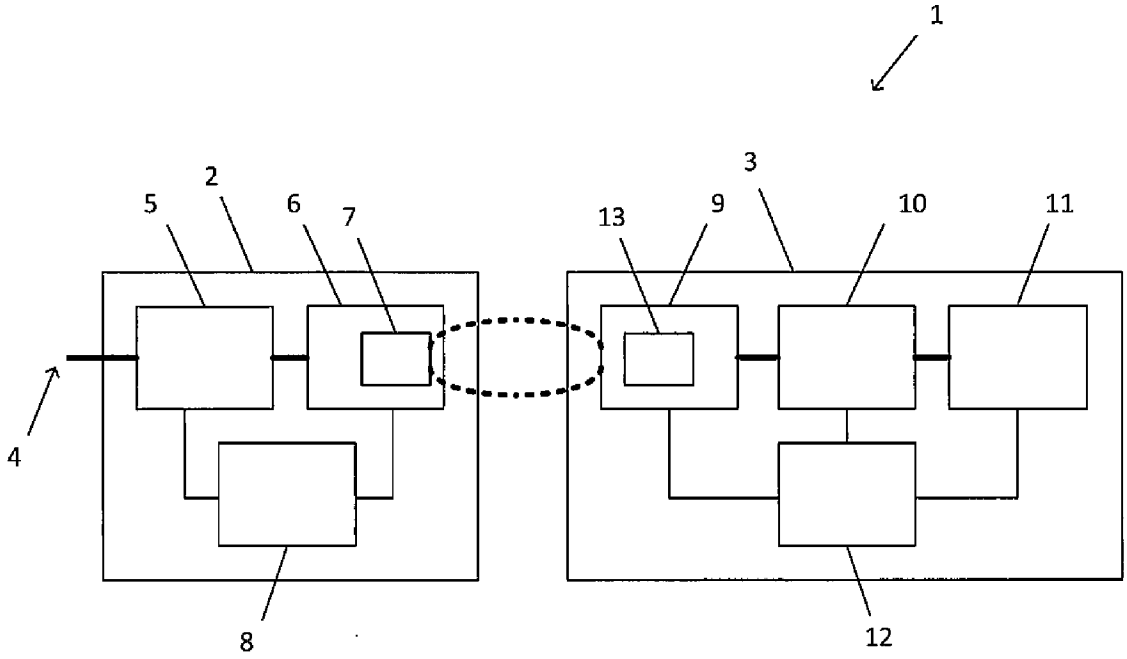


Figure 1

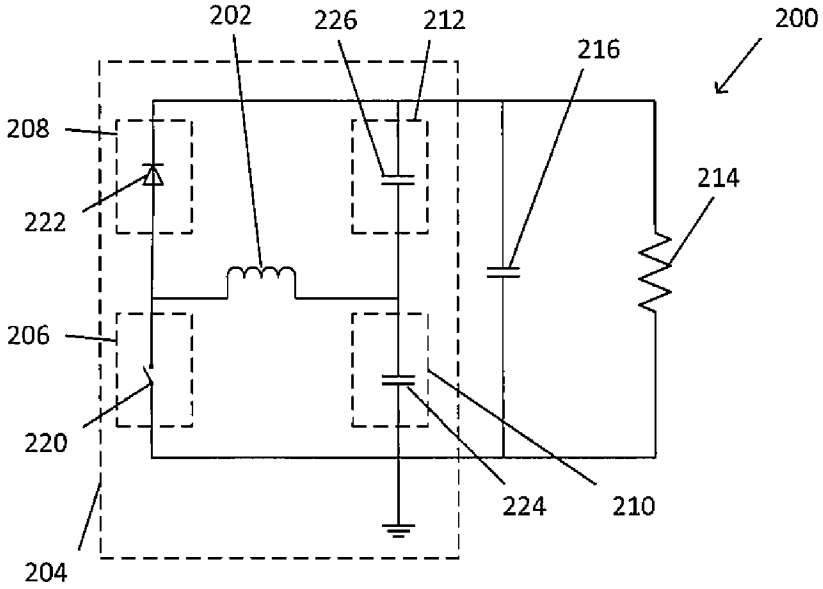


Figure 2

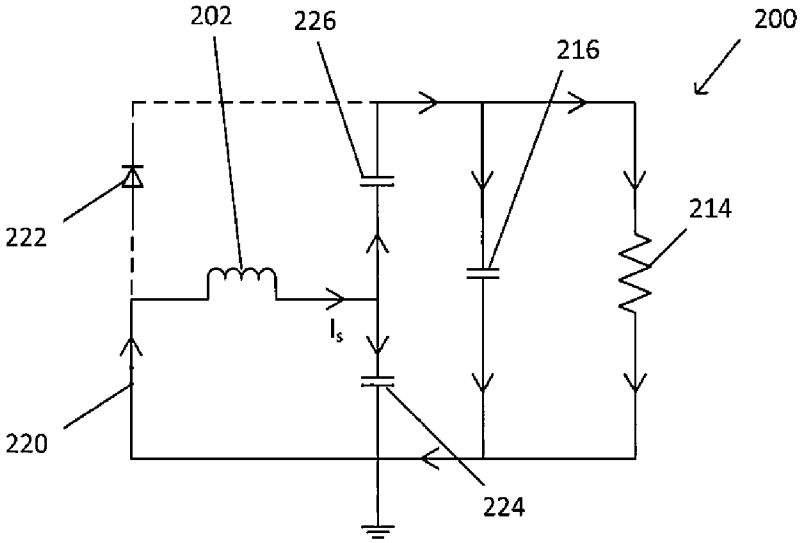


Figure 3A

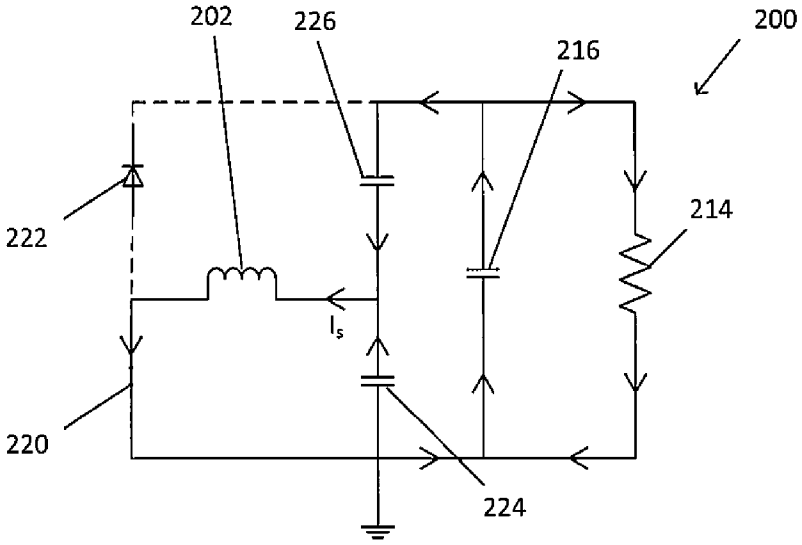


Figure 3B

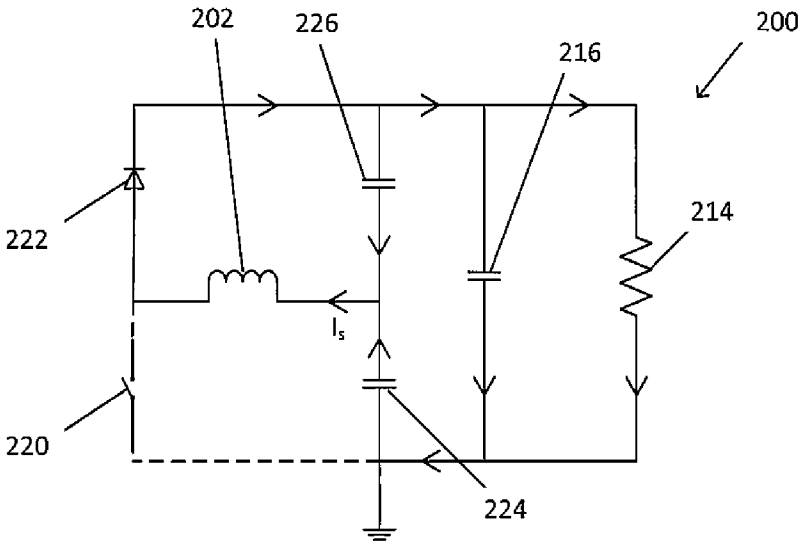


Figure 3C

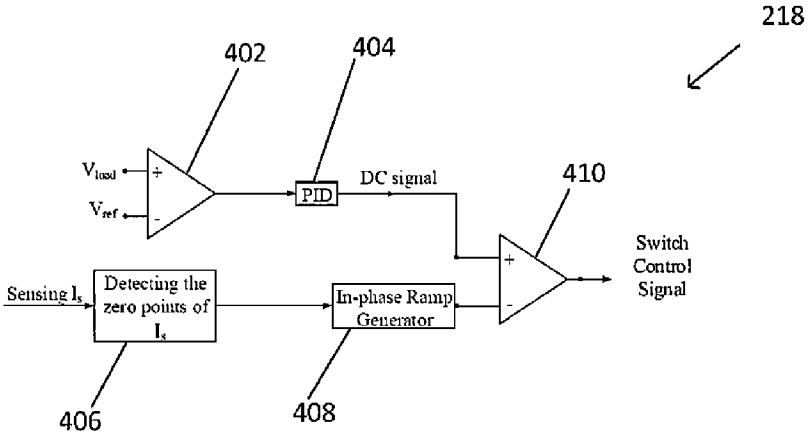


Figure 4

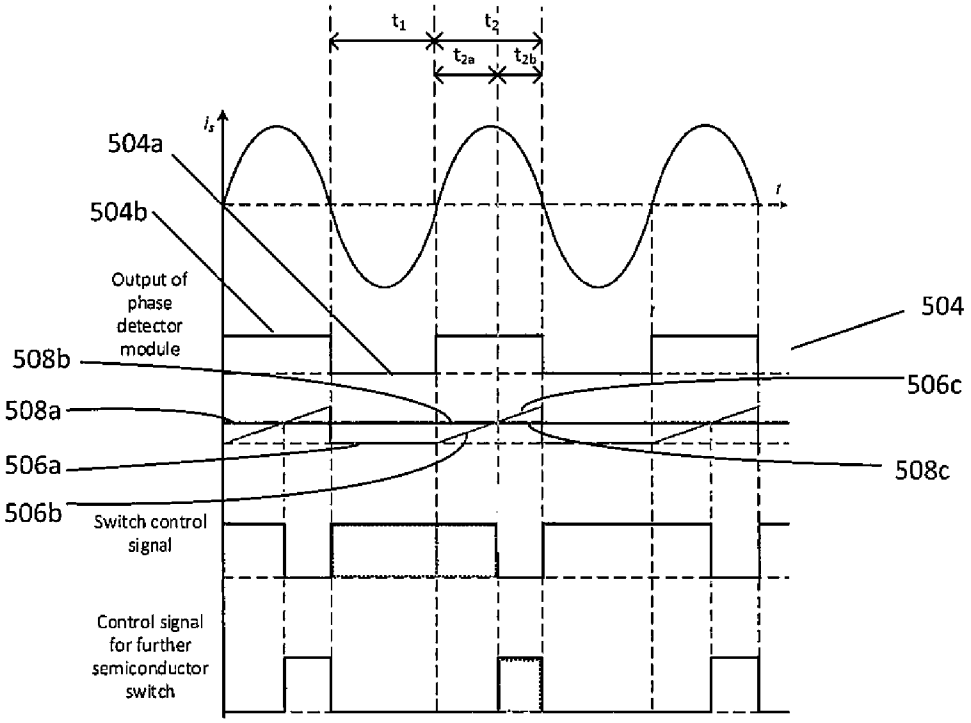


Figure 5

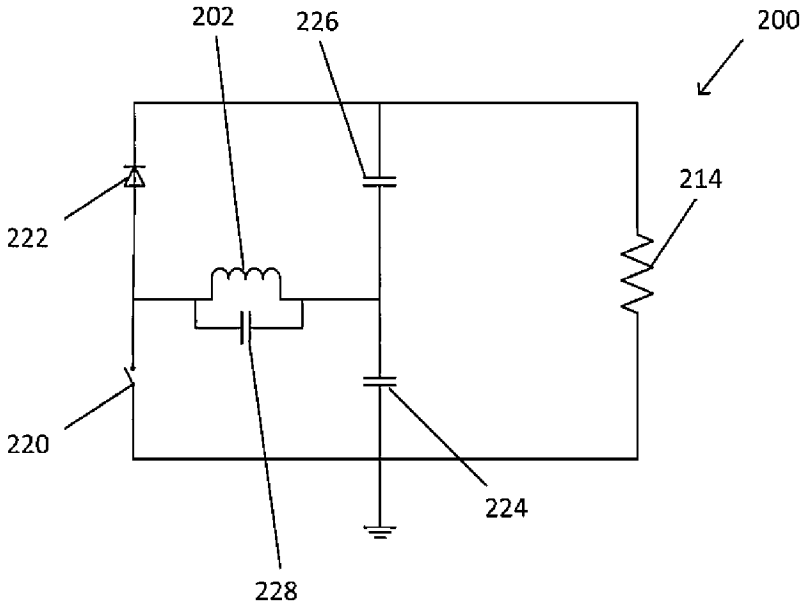


Figure 6A

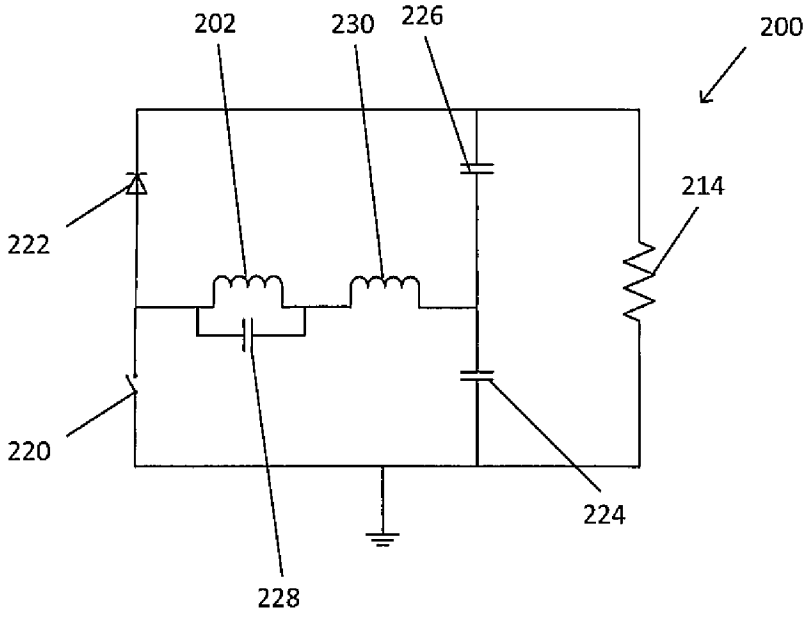


Figure 6B

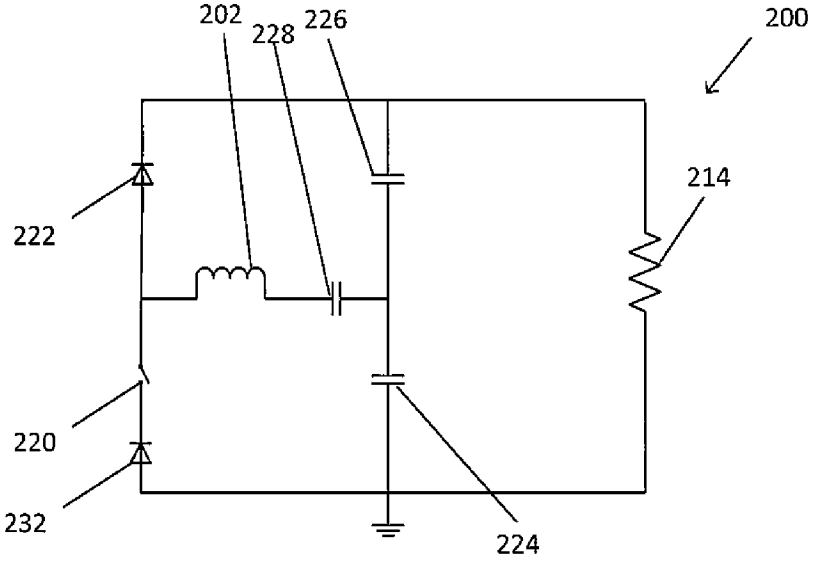


Figure 7

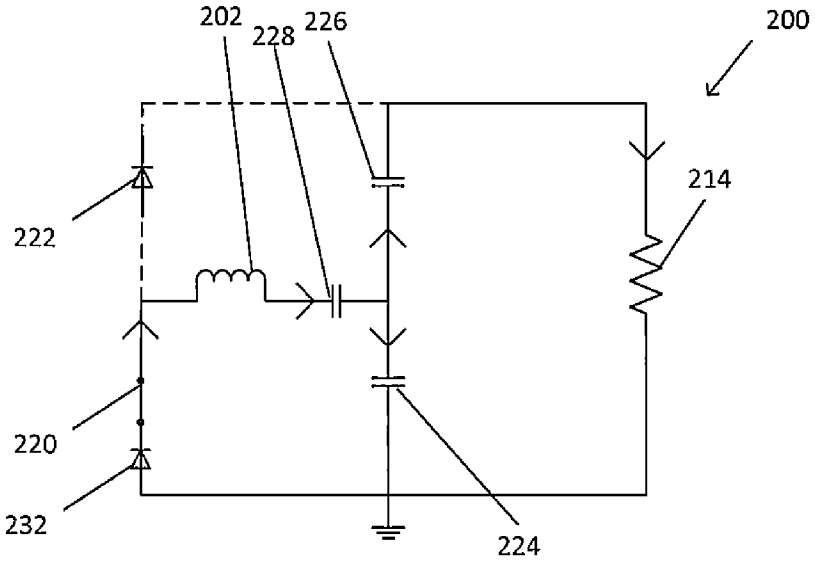


Figure 8A

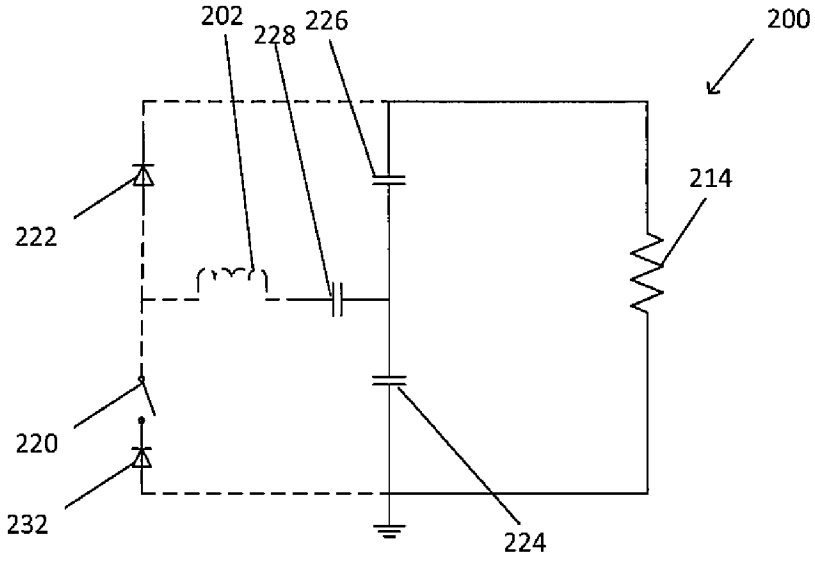


Figure 8B

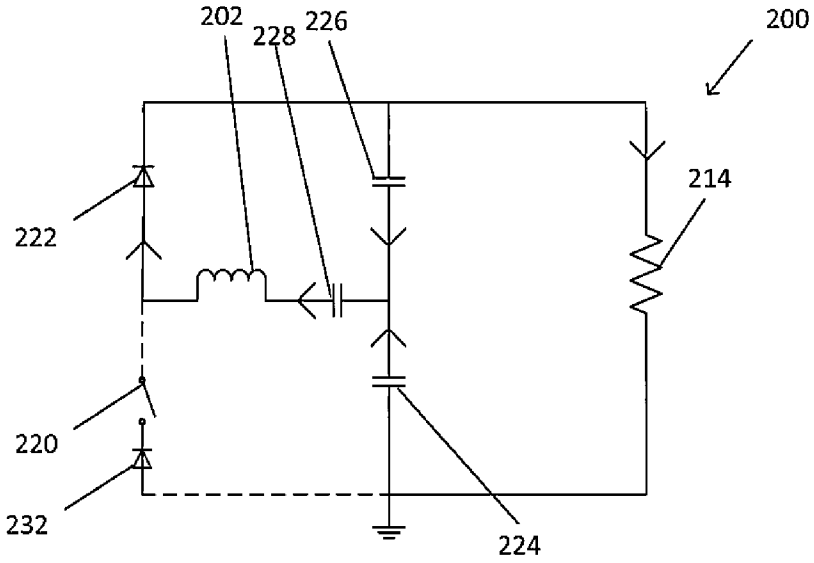


Figure 8C

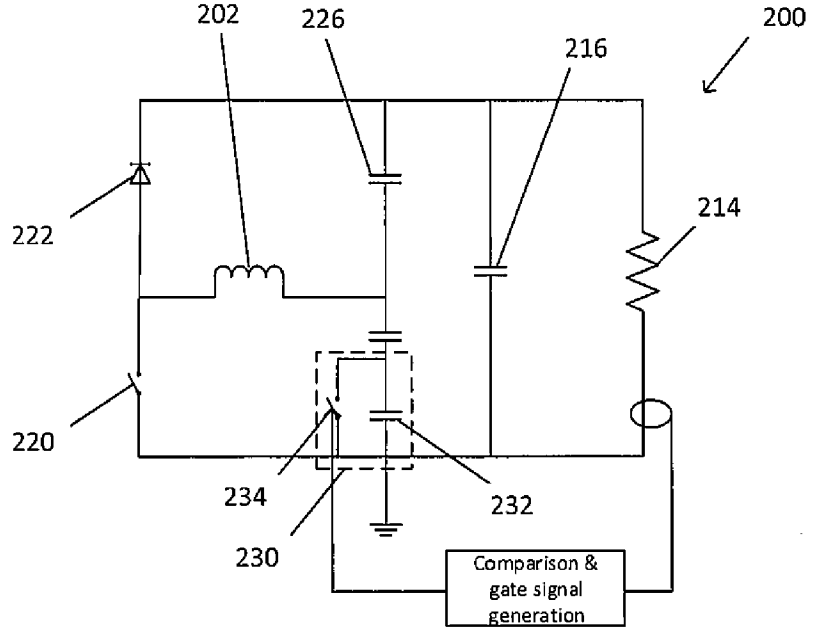


Figure 9