PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4863399

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SILICON GRAPHICS INTERNATIONAL CORP.	05/01/2017

RECEIVING PARTY DATA

Name:	Hewlett Packard Enterprise Development LP
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PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	15339451

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ATTORNEY DOCKET NUMBER:	90444842
NAME OF SUBMITTER:	DEBORAH HIGHAM
SIGNATURE:	/Deborah Higham/
DATE SIGNED:	03/13/2018

Total Attachments: 56
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PATENT ASSIGNMENT

This **PATENT ASSIGNMENT** (this "Assignment"), effective as of May 1, 2017 (the "Effective Date"), is entered into by and between **Silicon Graphics International Corp.** ("SGI" or "Assignor"), a Delaware corporation with a place of business at 3000 Hanover Street, Palo Alto, CA, 94304, United States, and **Hewlett Packard Enterprise Development LP**, a limited partnership organized under the laws of Texas, with a principal office and place of business at 11445 Compaq Center Drive West, Houston, TX 77707 ("HPED" or "Assignee"). SGI and HPED are referred to herein individually as a "Party" and collectively as the "Parties".

RECITALS

WHEREAS, Assignor and Assignee are parties to that certain Intellectual Property Assignment Agreement dated May 1, 2017 (the "Agreement"), pursuant to which Assignor assigned to Assignee all right, title, and interest in and to the patents and patent applications scheduled in Exhibit A ("Patents") and Assignee acquired all right, title, and interest in and to the Patents;

WHEREAS, the Parties wish to record such acquisition; and

NOW, THEREFORE, for good and valuable consideration, the adequacy and receipt of which are hereby acknowledged, the Parties agree as follows:

1. Assignor hereby assigns to Assignee all right, title, and interest, throughout the world, in and to the Patents, including, without limitation, the right to sue for injunctive relief and damages (including based on provisional rights related to published patent applications among the Patents) for infringement of any of the Patents accruing at any time prior to, on or after the Effective Date, and the right (where applicable) to file applications under the Paris Convention corresponding to or based on any of the applications for the Patents and to claim priority from such applications and to file national phase, regional phase, continuation, continuation-in-part and divisional applications based on the Patents.

2. Assignor hereby authorizes and requests the competent authorities to record this Assignment and to grant and issue any and all registrations of the Patents throughout the world to Assignee, its successors, or assigns, whose rights, title, and interests in such registrations are the same as would have been held and enjoyed by Assignor had this Assignment not been made.

3. Assignor will, and will ensure that any other necessary party will, execute all such documents and do all such acts and things as may be required by Assignee for securing and perfecting the assignment of the Patents in accordance with this Assignment.

4. This Assignment will be binding upon the parties and their successors and assigns.

5. This Assignment may be executed simultaneously in two or more counterparts, each of which will be deemed an original, but all of which together will constitute one and the same instrument. This Assignment may be executed by facsimile or .pdf signature, and a facsimile or .pdf signature will constitute an original for all purposes.

IN WITNESS WHEREOF the Parties have executed this Assignment by their duly authorized representatives as of the Effective Date:

Silicon Graphics International Corp.

Rishi Varma

Signature

Rishi Varma

Printed Name

Director

Title

May 1, 2017

Date

Hewlett Packard Enterprise Development LP
By: Enterprise DC Holdings LLC, its General Partner

Rishi Varma

Signature

Rishi Varma

Printed Name

Manager

Title

May 1, 2017

Date

EXHIBIT A

Serial #	Patent/ Publication Number	Title	Country	Filed Date
13/831,649	US 2014-0279926 A1	ACTIVE ARCHIVE BRIDGE	US	3/15/2013
14/529,050	US 2015-0056867 A1	MICRO ETHERNET CONNECTOR	US	10/30/2014
61/779,351		MICRO ETHERNET CONNECTOR	US	3/13/2013
13/853,943	9,124,049	MICRO ETHERNET CONNECTOR	US	3/29/2013
61/780,292		VIRTUAL STORAGE POOL	US	3/13/2013
13/853,863	US 2014-0281355	VIRTUAL STORAGE POOL	US	3/29/2013
61/780,770		SERVER WITH HEAT PIPE COOLING	US	3/13/2013
13/931,813		SERVER WITH HEAT PIPE COOLING	US	6/29/2013
61/780,787		SERVER WITH HEAT BAFFLE COOLING	US	3/13/2013
13/931,814		SERVER WITH HEAT BAFFLE COOLING	US	6/29/2013
61/780,790		HARD DISK DRIVE MOUNTING BRACKET	US	3/13/2013
13/853,839		HARD DISK DRIVE MOUNTING BRACKET	US	3/29/2013
13/835,462	US 2014-0281301 A1	ELASTIC HIERARCHICAL DATA STORAGE BACKEND STORING COPIES OF DATA SIMULTANEOUSLY TO MULTIPLE STORAGES OF DIFFERENT PERFORMANCE METRICS	US	3/15/2013
61/789,681		TCP SERVER BOOTLOADER	US	3/15/2013
13/897,198	US 2014-0282478 A1	TCP SERVER BOOTLOADER	US	5/17/2013
13/831,671	US 2014-0280957 A1	DYNAMIC ASSEMBLY AND DISPATCH OF CONTROLLING SOFTWARE	US	3/15/2013
13/831,683	US 2014-0281604 A1	AUTONOMOUS POWER SPARING STORAGE	US	3/15/2013
13/831,694	US 2014-0281300 A1	OPPORTUNISTIC TIER IN HIERARCHICAL STORAGE	US	3/15/2013
14/492,248	8,997,122	BLOCK DEVICE MANAGEMENT	US	9/22/2014
13/835,575	8,881,176	BLOCK DEVICE MANAGEMENT	US	3/15/2013
13/831,702	US 2014-0281322 A1	TEMPORAL HIERARCHICAL TIERED DATA STORAGE	US	3/15/2013

Serial #	Patent/ Publication Number	Title	Country	Filed Date
13/831,719	US 2014-0281621 A1	STEALTH POWER MANAGEMENT IN STORAGE ARRAY	US	3/15/2013
13/836,073		FAST MOUNT CACHE	US	3/15/2013
13/831,738	9,158,474	DYNAMIC STORAGE DEVICE LIBRARIES	US	3/15/2013
61/786,444		TOTAL QUOTAS FOR DATA STORAGE SYSTEM	US	3/15/2013
13/897,215	9,229,661	TOTAL QUOTAS FOR DATA STORAGE SYSTEM	US	5/17/2013
13/831,771	US 2014-0279919 A1	HIERARCHICAL SYSTEM MANAGER ROLLBACK	US	3/15/2013
13/831,745		FILE SYSTEM REPLICATION	US	3/15/2013
14/521,326		LOGICAL BLOCK PROTECTION FOR TAPE INTERCHANGE	US	10/22/2014
13/831,751	8,879,195	LOGICAL BLOCK PROTECTION FOR TAPE INTERCHANGE	US	3/15/2013
13/860,465		QUICK CONNECT COUPLER RAPID DISENGAGEMENT EXTENSION MECHANISM	US	4/10/2013
61/782,873		QUICK CONNECT COUPLER RAPID DISENGAGEMENT EXTENSION MECHANISM	US	3/14/2013
		MULTI-TIER NON-VOLATILE DATA STORAGE MANAGER	US	
		INFINITE DATA	US	
12/961,328	8,433,902	COMPUTER SYSTEM WITH DUAL OPERATING MODES	US	12/6/2010
11/079,409	7,849,311	COMPUTER SYSTEM WITH DUAL OPERATING MODES	US	3/15/2005
12/121,941	8,433,816	NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM	US	5/16/2008
13/873,058		NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM	US	4/29/2013
09/408,972	6,973,559	SCALABLE HYPERCUBE MULTIPROCESSOR NETWORK FOR MASSIVE PARALLEL PROCESSING	US	9/29/1999
11/295,676		NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM	US	12/6/2005

Serial #	Patent/ Publication Number	Title	Country	Filed Date
12/407,744	7,911,785	RACK MOUNTED COMPUTER SYSTEM INCLUDING CHASSIS RETAINER	US	3/19/2009
13/028,169	8,432,689	RACK MOUNTED COMPUTER SYSTEM	US	2/15/2011
11/125,942	7,529,097	RACK MOUNTED COMPUTER SYSTEM	US	5/9/2005
12/648,501	8,151,347	CLUSTERED FILE SYSTEM FOR MIX OF TRUSTED AND UNTRUSTED NODES	US	12/29/2009
13/438,304	8,578,478	CLUSTERED FILESYSTEMS FOR MIX OF TRUSTED AND UNTRUSTED NODES	US	4/3/2012
14/042,438		CLUSTERED FILESYSTEMS FOR MIX OF TRUSTED AND UNTRUSTED NODES	US	9/30/2013
10/414,239	7,640,582	CLUSTERED FILE SYSTEM FOR MIX OF TRUSTED AND UNTRUSTED NODES	US	4/16/2003
12/938,212	8,438,575	METHOD FOR EQUITABLE RESOURCE SHARING BETWEEN LOCAL AND NETWORK FILESYSTEMS	US	11/2/2010
10/620,835	7,827,556	METHOD FOR EQUITABLE RESOURCE SHARING BETWEEN LOCAL AND NETWORK FILESYSTEMS	US	7/17/2003
12/609,613		APPARATUS AND METHOD FOR ENHANCING THE MAINTAINABILITY AND COOLING OF COMPUTER COMPONENTS ON TRAYS IN A CABINET	US	10/30/2009
10/976,531		SYSTEM AND METHOD FOR SYNCHRONIZING DISTRIBUTION OF TRANSACTION OPERATIONS IN A COMPUTER SYSTEM	US	10/29/2004
09/811,158	7,627,694	MAINTAINING PROCESS GROUP MEMBERSHIP FOR NODE CLUSTERS IN HIGH AVAILABILITY COMPUTING SYSTEMS	US	3/16/2001
61/818,282		FLEXIBLE, SCALABLE, AND INTEGRATED BIG DATA ECOSYSTEM FOR DATA INGESTION, ANALYTICS, AND VISUALIZATION	US	5/1/2013

Serial #	Patent/ Publication Number	Title	Country	Filed Date
61/818,288		PLATFORM AND SOFTWARE FRAMEWROK FOR DATA INTENSIVE APPLICATIONS IN THE CLOUD	US	5/1/2013
61/841,262		PLATFORM AND SOFTWARE FRAMEWORK FOR DATA INTENSIVE APPLICATIONS IN THE CLOUD	US	6/28/2013
14/266,764	US 2014-0330851 A1	PLATFORM AND SOFTWARE FRAMEWORK FOR DATA INTENSIVE APPLICATIONS IN THE CLOUD	US	4/30/2014
12/273,453	8,971,329	SYSTEM AND METHOD FOR ORDERING OF DATA TRANSFERRED OVER MULTIPLE CHANNELS	US	11/18/2008
14/635,708		SYSTEM AND METHOD FOR ORDERING OF DATA TRANSFERRED OVER MULTIPLE CHANNELS	US	3/2/2015
60/219,915		SYSTEM AND METHOD FOR CONTROLLING THE FLOW AND ORDERING OF DATA TRANSFERRED OVER MULTIPLE CHANNELS	US	7/21/2000
09/910,587	7,453,878	SYSTEM AND METHOD FOR ORDERING OF DATA TRANSFERRED OVER MULTIPLE CHANNELS	US	7/20/2001
10/696,146		MULTIPROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN	US	10/29/2003
09/418,520	6,651,157	MULTIPROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN	US	10/15/1999
11/892,627	8,427,491	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR REMOTE GRAPHICS PROCESSING	US	8/24/2007
13/850,250	8,581,917	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR REMOTE GRAPHICS PROCESSING	US	3/25/2013
14/042,659	8,760,456	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR REMOTE GRAPHICS PROCESSING	US	9/30/2013

Serial #	Patent/ Publication Number	Title	Country	Filed Date
14/303,566	9,230,295	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR REMOTE GRAPHICS PROCESSING	US	6/12/2014
09/629,458	7,274,368	SYSTEM METHOD AND COMPUTER PROGRAM PRODUCT FOR REMOTE GRAPHICS PROCESSING	US	7/31/2000
14/987,690		SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR REMOTE GRAPHICS PROCESSING	US	1/4/2016
12/903,096	8,156,080	CLUSTERED FILESYSTEM WITH DATA VOLUME SNAPSHOT MAINTENANCE	US	10/12/2010
10/162,258	6,950,833	CLUSTERED FILESYSTEM	US	6/5/2002
60/296,046		CLUSTER FILE SYSTEM	US	6/5/2001
11/785,256	7,814,058	CLUSTERED FILESYSTEM WITH INTERRUPTIBLE TOKEN ACQUISITION	US	4/16/2007
14/504,368	US 2015-0019492 A1	CLUSTERED FILESYSTEM WITH DATA VOLUME SNAPSHOT	US	10/1/2014
13/442,037	8,527,463	CLUSTERED FILESYSTEM WITH DATA VOLUME SNAPSHOT MAINTENANCE	US	4/9/2012
10/414,245	7,765,329	MESSAGING BETWEEN HETEROGENEOUS CLIENTS OF A STORAGE AREA NETWORK	US	4/16/2003
10/345,357	7,593,968	RECOVERY AND RELOCATION OF A DISTRIBUTED NAME SERVICE IN A CLUSTER FILESYSTEM	US	1/16/2003
10/682,841		CLUSTERED FILESYSTEM WITH INTERRUPTIBLE TOKEN ACQUISITION	US	10/10/2003
14/012,894	9,020,897	CLUSTERED FILESYSTEM WITH DATA VOLUME SNAPSHOT	US	8/28/2013
10/620,387	8,010,558	RELOCATION OF METADATA SERVER WITH OUTSTANDING DMAPI REQUESTS	US	7/17/2003
13/220,257	9,275,058	RELOCATION OF METADATA SERVER WITH OUTSTANDING DMAPI REQUESTS	US	8/29/2011

Serial #	Patent/ Publication Number	Title	Country	Filed Date
13/211,200	8,683,021	CLUSTERED FILESYSTEM WITH MEMBERSHIP VERSION SUPPORT	US	8/16/2011
14/199,619	US 201400188955 A1	CLUSTERED FILESYSTEM WITH MEMBERSHIP VERSION SUPPORT	US	3/6/2014
11/785,255	8,001,222	CLUSTERED FILESYSTEM WITH MEMBERSHIP VERSION SUPPORT	US	4/16/2007
10/084,088	6,877,030	METHOD AND SYSTEM FOR CACHE COHERENCE IN DSM MULTIPROCESSOR SYSTEM WITHOUT GROWTH OF THE SHARING VECTOR	US	2/28/2002
10/434,340	7,818,424	REAL-TIME STORAGE AREA NETWORK	US	5/9/2003
60/378,941		REAL-TIME STORAGE AREA NETWORK	US	5/10/2002
12/907,867	8,589,499	REAL-TIME STORAGE AREA NETWORK	US	10/19/2010
14/042,695	9,386,100	REAL-TIME STORAGE AREA NETWORK	US	9/30/2013
10/631,988	8,185,703	DETECTION AND CONTROL OF RESOURCE CONGESTION BY A NUMBER OF PROCESSORS	US	7/31/2003
13/478,051	9,271,267	DETECTION AND CONTROL OF RESOURCE CONGESTION BY A NUMBER OF PROCESSORS	US	5/22/2012
15/051,512		DETECTION AND CONTROL OF RESOURCE CONGESTION BY A NUMBER OF PROCESSORS	US	2/23/2016
14/141,278	9,361,474	NETWORK FILESYSTEM ASYNCHRONOUS I/O SCHEDULING	US	12/26/2013
10/620,797	8,635,256	NETWORK FILESYSTEM ASYNCHRONOUS I/O SCHEDULING	US	7/17/2003
13/084,280	8,321,634	SYSTEM AND METHOD FOR PERFORMING MEMORY OPERATIONS IN A COMPUTING SYSTEM	US	4/11/2011
10/836,932	7,398,359	SYSTEM AND METHOD FOR PERFORMING MEMORY OPERATIONS IN A COMPUTING SYSTEM	US	4/30/2004

Serial #	Patent/ Publication Number	Title	Country	Filed Date
13/683,367		SYSTEM AND METHOD FOR PERFORMING MEMORY OPERATIONS IN A COMPUTING SYSTEM	US	11/21/2012
12/168,689	7,925,839	SYSTEM AND METHOD FOR PERFORMING MEMORY OPERATIONS IN A COMPUTING SYSTEM	US	7/7/2008
60/467,019		ULTRAVIOLET TRANSACTION MEMORY OPERATION	US	4/30/2003
11/644,770		COMPUTER RACK WITH POWER DISTRIBUTION SYSTEM	US	12/21/2006
60/471,430		COMPUTER RACK WITH POWER DISTRIBUTION SYSTEM	US	5/16/2003
10/464,028	7,173,821	COMPUTER RACK WITH POWER DISTRIBUTION SYSTEM	US	6/17/2003
11/928,616	7,525,797	HIGH DENSITY COMPUTER EQUIPMENT STORAGE SYSTEM	US	10/30/2007
10/279,153	6,741,467	HIGH DENSITY COMPUTER EQUIPMENT STORAGE SYSTEM	US	10/23/2002
10/603,338	6,822,859	COMPUTER RACK COOLING SYSTEM	US	6/24/2003
10/678,006	8,582,290	HIGH DENSITY COMPUTER EQUIPMENT STORAGE SYSTEM	US	10/1/2003
11/715,648	7,355,847	HIGH DENSITY COMPUTER EQUIPMENT STORAGE SYSTEM	US	3/7/2007
10/627,375	6,850,408	HIGH DENSITY COMPUTER EQUIPMENT STORAGE SYSTEM	US	7/24/2003
09/479,824	6,496,366	HIGH DENSITY COMPUTER EQUIPMENT STORAGE SYSTEM	US	1/7/2000
60/161,578		HIGH DENSITY COMPUTER EQUIPMENT STORAGE SYSTEM	US	10/26/1999
10/980,186	7,529,967	METHOD AND SYSTEM FOR NETWORK STORAGE DEVICE FAILURE PROTECTION AND RECOVERY	US	11/4/2004

Serial #	Patent/ Publication Number	Title	Country	Filed Date
10/714,398	7,324,995	METHOD FOR RETRIEVING AND MODIFYING DATA ELEMENTS ON A SHARED MEDIUM	US	11/17/2003
60/219,937		METHOD AND SYSTEM FOR COVERING MULTIPLE RESOURCES WITH A SINGLE CREDIT IN A COMPUTER SYSTEM	US	7/20/2000
09/910,584	7,007,097	METHOD AND SYSTEM FOR COVERING MULTIPLE RESOURCES WITH A SINGLE CREDIT IN A COMPUTER SYSTEM	US	7/20/2001
60/219,951		SYSTEM AND METHOD FOR REMOVING DATA FROM PROCESSOR CACHES IN A DISTRIBUTED MULTIPROCESSOR COMPUTER SYSTEM	US	7/20/2000
14/141,326	9,367,473	SYSTEM AND METHOD FOR REMOVING DATA FROM PROCESSOR CACHES IN A DISTRIBUTED MULTI-PROCESSOR COMPUTER SYSTEM	US	12/26/2013
09/909,700	8,635,410	SYSTEM AND METHOD FOR REMOVING DATA FROM PROCESSOR CACHES IN A DISTRIBUTED MULTIPROCESSOR COMPUTER SYSTEM	US	7/20/2001
15/180,322		SYSTEM AND METHOD FOR REMOVING DATA FROM PROCESSOR CACHES IN A DISTRIBUTED MULTI-PROCESSOR COMPUTER SYSTEM	US	6/13/2016
13/794,483	8,838,658	MULTI-CLASS HETEROGENEOUS CLIENTS IN A CLUSTERED FILESYSTEM	US	3/11/2013
10/414,236	7,617,292	MULTI-CLASS HETEROGENEOUS CLIENTS IN A CLUSTERED FILESYSTEM	US	4/16/2003
12/615,930	8,396,908	MULTI-CLASS HETEROGENEOUS CLIENTS	US	11/10/2009

Serial #	Patent/ Publication Number	Title	Country	Filed Date
		IN A CLUSTERED FILESYSTEM		
14/481,666	US 2015-0012778 A1	MULTI-CLASS HETEROGENEOUS CLIENTS IN A CLUSTERED FILESYSTEM	US	9/9/2014
13/856,394		METHOD FOR TRANSPARENTLY CONNECTING AUGMENTED NETWORK SOCKET OPERATIONS	US	4/3/2013
13/843,810		METHOD FOR TRANSPARENTLY CONNECTING AUGMENTED NETWORK SOCKET OPERATIONS	US	3/15/2013
61/696,078		INTEGRATED VISUALIZATION	US	8/31/2012
13/931,818	9,389,760	INTEGRATED VISUALIZATION	US	6/29/2013
15/203,631		INTEGRATED VISUALIZATION	US	7/6/2016
61/724,274		HIGH-DENSITY CLUSTERED COMPUTER SYSTEM	US	11/8/2012
61/696,047		TRANSACTIONAL MEMORY PROXY	US	8/31/2012
14/012,783	9,208,090	TRANSACTIONAL MEMORY PROXY	US	8/28/2013
61/696,077		DYNAMIC RESOURCE SCHEDULING	US	8/31/2012
13/931,819		DYNAMIC RESOURCE SCHEDULING	US	6/29/2013
61/800,436		NETWORK SECURITY MONITORING IN SHARED MEMORY ENVIRONMENT	US	3/15/2013
14/335,735	US 2014-00337691 A1	SYSTEM AND METHOD FOR CONVEYING INFORMATION	US	7/18/2014
12/264,871	7,873,741	SYSTEM AND METHOD FOR CONVEYING INFORMATION	US	11/4/2008
13/705,087	8,812,721	SYSTEM AND METHOD FOR CONVEYING INFORMATION	US	12/4/2012
13/008,635	8,327,015	SYSTEM AND METHOD FOR CONVEYING INFORMATION	US	1/18/2011
10/310,400	7,447,794	SYSTEM AND METHOD FOR CONVEYING INFORMATION	US	12/4/2002

Serial #	Patent/ Publication Number	Title	Country	Filed Date
10/837,057	7,802,058	METHOD FOR PERFORMING CACHE COHERENCY IN A COMPUTER SYSTEM	US	4/30/2004
60/467,102		ULTRAVIOLET COHERENCY/CONSISTENCY METHODS	US	4/30/2003
12/887,374	8,402,225	METHOD FOR PERFORMING CACHE COHERENCY IN A COMPUTER SYSTEM	US	9/21/2010
13/846,731		METHOD FOR PERFORMING CACHE COHERENCY IN A COMPUTER SYSTEM	US	3/18/2013
13/843,919	9,240,940	SCALABLE INFINIBAND INTERCONNECT PERFORMANCE AND DIAGNOSTIC TOOL	US	3/15/2013
10/426,003	8,291,009	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR APPLYING DIFFERENT TRANSPORT MECHANISMS FOR USER INTERFACE AND IMAGE PORTIONS OF A REMOTELY RENDERED IMAGE	US	4/30/2003
14/528,929	9,117,288	APPLYING DIFFERENT TRANSPORT MECHANISMS FOR USER INTERFACE AND IMAGE PORTIONS OF A REMOTELY RENDERED IMAGE	US	10/30/2014
13/620,223	8,924,473	APPLYING DIFFERENT TRANSPORT MECHANISMS FOR USER INTERFACE AND IMAGE PORTIONS OF A REMOTELY RENDERED IMAGE	US	9/14/2012
08/049,803	5,272,664	HIGH MEMORY CAPACITY DRAM SIMM	US	4/21/1993
08/128,082	5,509,125	A SYSTEM AND METHOD FOR FAIR ARBITRATION ON A MULTI-DOMAIN MULTIPROCESSOR BUS	US	9/29/1993
08/128,080	5,504,874	A SYSTEM AND METHOD OF IMPLEMENTING READ RESOURCES TO MAINTAIN CACHE COHERENCY IN A MULTIPROCESSOR	US	9/29/1993

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		ENVIRONMENT PERMITTING SPLIT TRANSACTIONS		
08/578,997	5,664,151	A SYSTEM AND METHOD OF IMPLEMENTING READ RESOURCES TO MAINTAIN CACHE COHERENCY IN A MULTIPROCESSOR ENVIRONMENT PERMITTING SPLIT TRANSACTIONS	US	12/27/1995
08/128,720	5,544,331	SYSTEM AND METHOD FOR GENERATING A READ-MODIFY-WRITE OPERATION	US	9/30/1993
08/128,081	5,655,102	SYSTEM AND METHOD FOR PIGGYBACKING OF READ RESPONSES ON A SHARED MEMORY MULTIPROCESSOR BUS	US	9/29/1993
08/435,451	5,669,008	HIERARCHICAL FAT HYPERCUBE ARCHITECTURE FOR PARALLEL PROCESSING SYSTEMS	US	5/5/1995
08/435,462	5,991,895	SYSTEM AND METHOD FOR MULTIPROCESSOR PARTITIONING TO SUPPORT HIGH AVAILABILITY	US	5/5/1995
08/435,459	5,787,476	SYSTEM AND METHOD FOR MAINTAINING COHERENCY OF VIRTUAL-TO-PHYSICAL MEMORY TRANLATIONS IN A MULTIPROCESSOR COMPUTER	US	5/5/1995
60/296,046		CLUSTER FILE SYSTEM	US	6/5/2001
10/197,211		EXTENDED ATTRIBUTE CACHING IN CLUSTERED FILESYSTEM	US	7/18/2002
10/191,923	6,862,187	APPARATUS AND METHOD FOR MAXIMIZING EQUIPMENT STORAGE DENSITY	US	7/9/2002
10/875,355	6,906,925	APPARATUS AND METHOD FOR MAXIMIZING EQUIPMENT STORAGE DENSITY	US	6/24/2004

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08/435,463	5,634,110	CACHE COHERENCY USING FLEXIBLE DIRECTORY BIT VECTORS	US	5/5/1995
08/435,453	5,768,529	A SYSTEM AND METHOD FOR THE SYNCHRONOUS TRANSMISSION OF DATA IN A COMMUNICATION NETWORK UTILIZING A SOURCE CLOCK SIGNAL TO LATCH SERIAL DATA INTO FIRST REGISTERS AND A HANDSHAKE SIGNAL TO LATCH PARALLEL DATA INTO SECOND REGISTERS	US	5/5/1995
08/638,186	5,811,997	MULTI-CONFIGURABLE PUSH-PULL/OPEN-DRAIN DRIVER CIRCUIT	US	4/26/1996
08/435,448		SYSTEM FOR CONTINUOUSLY RECIRCULATING NEGATIVELY ACKNOWLEDGED REQUESTS OF THE SOURCE UNTIL THE NEGATIVELY ACKNOWLEDGED REQUESTS ARE ACCEPTED BY FLOW CONTROL ASSOCIATED WITH EACH TARGET	US	5/5/1995
08/892,879	5,974,456	SYSTEM FOR CONTINUOUSLY RECIRCULATING NEGATIVELY ACKNOWLEDGED REQUESTS OF THE SOURCE UNTIL THE NEGATIVELY ACKNOWLEDGED REQUESTS ARE ACCEPTED BY FLOW CONTROL ASSOCIATED WITH EACH TARGET	US	7/15/1997
09/126,944	6,049,476	HIGH MEMORY CAPACITY DIMM WITH DATA AND STATE MEMORY	US	7/31/1998
08/440,214		HIGH MEMORY CAPACITY DIMM WITH DATA AND STATE MEMORY	US	5/15/1995
08/747,975	5,790,447	HIGH MEMORY CAPACITY DIMM WITH DATA AND STATE MEMORY	US	11/12/1996

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08/747,976	5,686,730	DIMM PAIR WITH DATA MEMORY AND STATE MEMORY	US	11/12/1996
08/440,967		DIMM PAIR WITH DATA MEMORY AND STATE MEMORY	US	5/15/1995
09/910,591	7,069,306	METHOD AND SYSTEM FOR MANAGING MEMORY IN A MULTIPROCESSOR SYSTEM	US	7/20/2001
11/426,538	7,500,068	METHOD AND SYSTEM FOR MANAGING MEMORY IN A MULTIPROCESSOR SYSTEM	US	6/26/2006
60/219,950		METHOD AND SYSTEM FOR MANAGING MEMORY IN A MULTIPROCESSOR SYSTEM	US	7/20/2000
09/910,531	6,981,101	METHOD AND SYSTEM FOR MAINTAINING DATA AT INPUT/OUTPUT (I/O) INTERFACES FOR A MULTIPROCESSOR SYSTEM	US	7/20/2001
60/219,938		METHOD AND SYSTEM FOR MAINTAINING DATA AT INPUT/OUTPUT (I/O) INTERFACES FOR A MULTIPROCESSOR SYSTEM	US	7/20/2000
09/910,395	6,839,820	METHOD AND SYSTEM FOR CONTROLLING DATA ACCESS BETWEEN AT LEAST TWO MEMORY ARRANGEMENTS	US	7/20/2001
60/219,948		METHOD AND SYSTEM FOR CONTROLLING DATA ACCESS BETWEEN AT LEAST TWO MEMORY ARRANGEMENTS	US	7/20/2000
10/142,822	6,724,669	SYSTEM AND METHOD FOR REPAIRING A MEMORY COLUMN	US	5/8/2002
10/131,309	6,621,300	SYSTEM AND METHOD FOR IMPROVING SPEED OF OPERATION OF INTEGRATED CIRCUITS	US	4/23/2002
10/310,237	7,712,006	SYSTEM AND METHOD FOR CONVEYING INFORMATION	US	12/4/2002
10/219,654	6,813,151	COMPUTER ENCLOSURE AND METHOD FOR MANUFACTURE	US	8/15/2002

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10/835,855	7,181,589	SYSTEM AND METHOD FOR PERFORMING ADDRESS TRANSLATION IN A COMPUTER SYSTEM	US	4/30/2004
09/789,602	6,667,891	COMPUTER CHASSIS FOR DUAL OFFSET OPPOSING MAIN BOARDS	US	2/20/2001
12/263,311	7,692,928	INTERFACE ASSEMBLY	US	10/31/2008
12/726,299	7,924,570	INTERFACE ASSEMBLY	US	3/17/2010
11/125,941	7,460,375	INTERFACE ASSEMBLY	US	5/9/2005
11/026,163	7,508,663	COMPUTER RACK COOLING SYSTEM WITH VARIABLE AIRFLOW IMPEDANCE	US	12/29/2004
11/125,424	7,411,784	ELECTROMAGNETIC INTERFERENCE SHIELD FOR I/O PORTS	US	5/9/2005
11/125,423	7,372,695	DIRECTIONAL FAN ASSEMBLY	US	5/9/2005
11/125,477	7,236,370	COMPUTER RACK WITH CLUSTER MODULES	US	5/9/2005
08/717,580	6,683,876	PACKET SWITCHED ROUTER ARCHITECTURE FOR PROVIDING MULTIPLE SIMULTANEOUS COMMUNICATIONS	US	9/23/1996
09/896,370	6,985,484	PACKETIZED DATA TRANSMISSIONS IN A SWITCHED ROUTER ARCHITECTURE	US	6/28/2001
08/780,785	6,282,195	PACKETIZED DATA TRANSMISSIONS IN A SWITCHED ROUTER ARCHITECTURE	US	1/9/1997
		POWER MANAGEMENT SYSTEM	US	
		PROGRAMMABLE REMOTE MANAGEMENT	US	
		BATTERY BUFFER FOR A COMPUTER SYSTEM POWER SUPPLY	US	
		COOLING SYSTEM FOR A MOBILE COMPUTING PLATFORM	US	
		POWER SYSTEM FOR A MOBILE COMPUTING PLATFORM	US	
		SELF-CONTAINED CONCENTRO	US	

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		AC BUS BAR	US	
		QUAD SMALL FORM-FACTOR PLUGGABLE HEAT SINK	US	
		METHOD AND SYSTEM TO CONTROL AND MONITOR REMOTE POWER AND COOLING RESOURCES IN A HIGHLY SCALABLE COMPUTER	US	
08/544,537	5,832,306	ACKNOWLEDGE TRIGGERED FORWARDING OF EXTERNAL BLOCK DATA RESPONSES IN A MICROPROCESSOR	US	10/18/1995
08/539,524	5,963,981	SYSTEM AND MERTHOD FOR UNCACHED STORE BUFFERING IN A MICROPROCESSOR	US	10/6/1995
09/407,428	6,751,698	MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD	US	9/29/1999
10/868,181	7,406,086	MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD	US	6/15/2004
12/181,202	7,881,321	MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD	US	7/28/2008
09/909,693	6,775,742	EMORY DEVICE STORING DATA AND DIRECTORY INFORMATION THEREON, AND METHOD FOR PROVIDING THE DIRECTORY INFORMATION AND THE DATA IN THE MEMORY DEVICE	US	7/20/2001
09/410,137	6,279,073	CONFIGURABLE SYNCHRONIZER FOR DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY	US	9/30/1999
10/047,347	6,578,115	METHOD AND APPARATUS FOR HANDLING INVALIDATION REQUESTS TO PROCESSORS NOT PRESENT IN A COMPUTER SYSTEM	US	1/14/2002

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09/410,139	6,339,812	METHOD AND APPARATUS FOR HANDLING INVALIDATION REQUESTS TO PROCESSORS NOT PRESENT IN A COMPUTER SYSTEM	US	9/30/1999
09/627,471	6,901,500	METHOD AND APPARATUS FOR PREFETCHING INFORMATION AND STORING THE INFORMATION IN A STREAM BUFFER	US	7/28/2000
09/636,098	6,683,607	METHOD FOR DISPLAYING THREE-DIMENSIONAL OBJECTS AND A COMPUTER-READABLE STORAGE MEDIUM STORING A PROGRAM FOR ACHIEVING THE SAME	US	8/10/2000
09/909,704	7,406,554	QUEUE CIRCUIT AND METHOD FOR MEMORY ARBITRATION EMPLOYING SAME	US	7/20/2001
09/909,705	6,816,947	SYSTEM AND METHOD FOR MEMORY ARBITRATION	US	7/20/2001
09/910,629	6,877,029	METHOD AND APPARATUS FOR MANAGING NODE CONTROLLERS USING PARTITIONS IN A COMPUTER SYSTEM	US	7/20/2001
10/725,897	6,938,128	SYSTEM AND METHOD FOR REDUCING MEMORY LATENCY DURING READ REQUESTS	US	12/2/2003
09/909,701	6,678,798	SYSTEM AND METHOD FOR REDUCING MEMORY LATENCY DURING READ REQUESTS	US	7/20/2001
09/910,274	6,718,442	METHOD AND SYSTEM FOR USING HIGH COUNT INVALIDATE ACKNOWLEDGEMENTS IN DISTRIBUTED SHARED MEMORY SYSTEMS	US	7/20/2001
09/910,589	6,915,387	SYSTEM AND METHOD FOR HANDLING UPDATES TO MEMORY IN A DISTRIBUTED SHARED MEMORY SYSTEM	US	7/20/2001

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09/346,638	6,629,855	MEMORY SYSTEM INCLUDING GUIDES THAT RECEIVE MEMORY MODULES	US	7/1/1999
09/910,631	6,859,863	METHOD AND SYSTEM FOR MANAGING DATA AT AN INPUT/OUTPUT INTERFACE FOR A MULTIPROCESSOR SYSTEM	US	7/20/2001
09/910,363	6,795,900	METHOD AND SYSTEM FOR STORING DATA AT INPUT/OUTPUT (I/O) INTERFACES FOR A MULTIPROCESSOR SYSTEM	US	7/20/2001
09/910,572	6,829,683	SYSTEM AND METHOD FOR TRANSFERRING OWNERSHIP OF DATA IN A DISTRIBUTED SHARED MEMORY SYSTEM	US	7/20/2001
09/714,047	6,550,048	METHOD AND SYSTEM FOR DETERMINING REPEATER ALLOCATION REGIONS	US	11/15/2000
08/807,551	5,963,913	SYSTEM AND METHOD FOR SCHEDULING AN EVENT SUBJECT TO THE AVAILABILITY OF REQUESTED PARTICIPANTS	US	2/28/1997
09/270,613	6,393,533	METHOD AND DEVICE FOR CONTROLLING ACCESS TO MEMORY	US	3/17/1999
09/356,106	6,421,712	METHOD AND APPARATUS FOR BROADCASTING INVALIDATION MESSAGES IN A COMPUTER SYSTEM	US	7/16/1999
09/315,806	7,197,589	SYSTEM AND METHOD FOR PROVIDING ACCESS TO A BUS	US	5/21/1999
09/410,120	6,381,681	SYSTEM AND METHOD FOR SHARED MEMORY PROTECTION IN A MULTIPROCESSOR COMPUTER	US	9/30/1999
09/409,606	6,453,408	SYSTEM AND METHOD FOR MEMORY PAGE MIGRATION IN A MULTI-PROCESSOR COMPUTER	US	9/30/1999
09/409,639	6,546,451	METHOD AND APPARATUS FOR DECOUPLING PROCESSOR SPEED FROM	US	9/30/1999

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		MEMORY SUBSYSTEM SPEED IN A NODE CONTROLLER		
08/935,820	6,182,089	METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR DYNAMICALLY ALLOCATING LARGE MEMORY PAGES OF DIFFERENT SIZES	US	9/23/1997
09/409,605	6,532,501	SYSTEM AND METHOD FOR DISTRIBUTING OUTPUT QUEUE SPACE	US	9/30/1999
09/910,630	6,915,388	METHOD AND SYSTEM FOR EFFICIENT USE OF A MULTI-DIMENSIONAL SHARING VECTOR IN A COMPUTER SYSTEM	US	7/20/2001
11/054,031	7,286,345	RACK-MOUNTED AIR DEFLECTOR	US	2/8/2005
11/855,370	7,499,273	RACK-MOUNTED AIR DEFLECTOR	US	9/14/2007
11/282,848	7,535,707	POWER SUPPLY COOLING SYSTEM	US	11/17/2005
11/764,551	7,768,780	FLOW-THROUGH COOLING FOR COMPUTER SYSTEMS	US	6/18/2007
11/860,685	7,724,513	CONTAINER-BASED DATA CENTER	US	9/25/2007
10/815,422	7,123,477	COMPUTER RACK COOLING SYSTEM	US	3/31/2004
11/099,396	7,558,971	ADAPTABLE POWER SUPPLY	US	4/4/2005
09/713,842	6,853,969	METHOD AND SYSTEM FOR ESTIMATING INTERCONNECT DELAY	US	11/15/2000
09/417,348	6,336,177	METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR MANAGING MEMORY IN A NON-UNIFORM MEMORY ACCESS SYSTEM	US	10/13/1999
08/933,833	6,289,424	METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR MANAGING MEMORY IN A NON-UNIFORM MEMORY ACCESS SYSTEM	US	9/19/1997
08/933,999	6,148,379	SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR INTER-CELL PAGE SHARING IN A	US	9/19/1997

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		DISTRIBUTED SHARED MEMORY SYSTEM		
08/921,257	6,115,790	SYSTEM METHOD AND COMPUTER PROGRAM PRODUCT FOR ORGANIZING PAGE CACHES	US	8/29/1997
08/911,192	5,974,536	METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR PROFILING THREAD VIRTUAL MEMORY ACCESSES	US	8/14/1997
08/933,998	6,112,286	REVERSE MAPPING PAGE FRAME DATA STRUCTURES TO PAGE TABLE ENTRIES	US	9/19/1997
08/866,247	6,173,322	NETWORK REQUEST DISTRIBUTION BASED ON STATIC RULES AND DYNAMIC PERFORMANCE DATA	US	6/5/1997
08/921,545	6,167,437	METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR PAGE REPLICATION IN A NON-UNIFORM MEMORY ACCESS SYSTEM	US	9/2/1997
09/128,392	6,728,206	CROSSBAR SWITCH WITH COMMUNICATION RING BUS	US	8/3/1998
08/971,261	6,055,579	DATA PROCESSING SYNCHRONIZATION WITH AUTOMATIC QUEUING	US	11/17/1997
09/427,203	6,766,358	EXCHANGING MESSAGES BETWEEN COMPUTER SYSTEMS COMMUNICATIVELY COUPLED IN A COMPUTER SYSTEM NETWORK	US	10/25/1999
09/399,437	6,594,787	INPUT/OUTPUT DEVICE MANAGED TIMER PROCESS	US	9/17/1999
09/409,805	6,622,182	UPSTREAM SITUATED APPARATUS AND METHOD FOR PROVIDING HIGH BANDWIDTH DATA FLOW CONTROL TO AN INPUT/OUTPUT UNIT	US	9/30/1999

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09/409,765	6,397,274	METHOD AND APPARATUS FOR ANALYZING BUFFER ALLOCATION TO A DEVICE ON A PERIPHERAL COMPONENT INTERCONNECT BUS	US	9/30/1999
10/210,257	7,406,587	METHOD AND SYSTEM FOR RENAMING REGISTERS IN A MICROPROCESSOR	US	7/31/2002
09/730,871	6,721,739	SYSTEM AND METHOD FOR MAINTAINING AND RECOVERING DATA CONSISTENCY ACROSS MULTIPLE PAGES	US	12/5/2000
09/418,597	6,281,108	SYSTEM AND METHOD TO PROVIDE POWER TO A SEA OF GATES STANDARD CELL BLOCK FROM AN OVERHEAD BUMP GRID	US	10/15/1999
09/459,995	6,879,948	SYNCHRONIZATION OF HARDWARE SIMULATION PROCESSES	US	12/14/1999
09/409,764	6,457,146	METHOD AND APPARATUS FOR PROCESSING ERRORS IN A COMPUTER SYSTEM	US	9/30/1999
09/409,607	6,487,685	SYSTEM AND METHOD FOR MINIMIZING ERROR CORRECTION CODE BITS IN VARIABLE SIZED DATA FORMATS	US	9/30/1999
09/409,768	6,529,570	DATA SYNCHRONIZER FOR A MULTIPLE RATE CLOCK SOURCE AND METHOD THEREOF	US	9/30/1999
09/608,935	6,293,813	ELECTRICAL CONNECTOR WITH LATCHING BACKPLATE ASSEMBLY	US	6/30/2000
09/409,766	6,564,277	METHOD AND SYSTEM FOR HANDLING INTERRUPTS IN A NODE CONTROLLER WITHOUT ATTACHED PROCESSORS	US	9/30/1999
09/660,732	6,532,575	METHOD AND SYSTEM FOR CALCULATING INTERCONNECT MOMENTS AND DELAY	US	9/13/2000
29/127,551	D445,112	SERVER DOOR	US	8/8/2000
29/125,876	D445,425	FRONT PANEL MEDIA DOOR	US	6/30/2000

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29/125,872	D444,471	DRIVE SLED HANDLE	US	6/30/2000
29/125,873	D444,474	DRIVE SLED COVER	US	6/30/2000
29/127,590	D444,461	SERVER COVER	US	8/8/2000
29/146,729	D464,056	SERVER PRODUCT FACEPLATE	US	8/15/2001
29/148,943	D473,561	SET OF MULTI-DEVICE FACEPLATES	US	9/28/2001
29/118,970	D475,705	COMPUTER CHASSIS FOR DUAL, OPPOSING MAIN BOARDS	US	2/18/2000
29/137,456	D473,225	PORTION OF A BANK OF COMPUTER CHASSIS MOUNTED TO RACK BARS	US	2/20/2001
13/931,790	US 2015-0006478 A1	REPLICATED DATABASE USING ONE SIDED RDMA	US	6/28/2013
09/995,668		SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR CAPTURING A VISUALIZATION SESSION	US	11/29/2001
08/935,819	6,112,285	METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR VIRTUAL MEMORY SUPPORT FOR MANAGING TRANSLATION LOOK ASIDE BUFFERS WITH MULTIPLE PAGE SIZE SUPPORT	US	9/23/1997
61/841,270		PRESSURE-ACTIVATED SERVER COOLING SYSTEM	US	6/28/2013
14/289,590	US 2015-0003010 A1	PRESSURE-ACTIVATED SERVER COOLING SYSTEM	US	5/28/2014
61/841,259		ROTATION OF GRAPHICAL SCENES	US	6/28/2013
13/931,785		COMBINING PARALLEL COORDINATES AND HISTOGRAMS	US	6/28/2013
13/931,797	US 2015-0007113 A1	VOLUME RENDERING FOR GRAPH RENDERIZATION	US	6/28/2013
09/615,312	6,601,120	SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR IMPLEMENTING SCALABLE MULTI-READER/SINGLE-WRITER LOCKS	US	7/13/2000
61/888,412		DEPLOYING BIG DATA SOFTWARE IN A MULTI-INSTANCE NODE	US	10/8/2013

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14/266,758		DEPLOYING BIG DATA SOFTWARE IN A MULTI-INSTANCE NODE	US	4/30/2014
61/841,279		SOFTWARE DESIGN PATTERN FOR ADAPTING A GRAPH DATABASE VISUALIZATION SOFTWARE	US	6/29/2013
14/266,656	US 2014-0330867 A1	SOFTWARE DESIGN PATTERN FOR ADAPTING A GRAPH DATABASE VISUALIZATION SOFTWARE	US	4/30/2014
08/168,166	5,564,804	DISK DRIVE BRACKET	US	12/17/1993
08/435,460	5,680,576	DIRECTORY-BASED COHERENCE PROTOCOL ALLOWING EFFICIENT DROPPING OF CLEAN-EXCLUSIVE DATA	US	5/5/1995
08/435,455	5,822,381	DISTRIBUTED GLOBAL CLOCK SYSTEM	US	5/5/1995
08/435,452	5,721,819	PROGRAMMABLE, DISTRIBUTED NETWORK ROUTING	US	5/5/1995
08/766,363	5,727,150	APPARATUS AND METHOD FOR PAGE MIGRATION IN A NON-UNIFORM MEMORY ACCESS (NUMA) SYSTEM	US	12/17/1996
08/592,736	5,727,037	SYSTEM AND METHOD TO REDUCE PHASE OFFSET AND PHASE JITTER IN PHASE-LOCKED AND DELAY-LOCKED LOOPS USING SELF-BIASED CIRCUITS	US	1/26/1996
08/933,829	6,249,802	METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR ALLOCATING PHYSICAL MEMORY IN A DISTRIBUTED SHARED MEMORY NETWORK	US	9/19/1997
08/938,672	5,960,434	SYSTEM METHOD AND COMPUTER PROGRAM PRODUCT FOR DYNAMICALLY SIZING HASH TABLES	US	9/26/1997
10/899,316		SYSTEM AND METHOD FOR NETWORKED COMPUTER GRAPHICS	US	7/27/2004

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		FAST COMMUNICATION OF CONTROL INFORMATION FOR A BULK DATA MOVE ENGINE	US	
61/864,586		MODIFYING BINNING OPERATIONS	US	8/11/2013
14/152,968	US 2015-0199105 A1	AUTOMATIC SELECTION OF CENTER OF ROTATION FOR GRAPHICAL SCENES	US	1/10/2014
14/162,613	US 2015-0205506 A1	SELECTION THRESHOLDS IN A VISUALIZATION INTERFACE	US	1/23/2014
14/152,969	US 2015-0199420 A1	VISUALLY APPROXIMATING PARALLEL COORDINATES DATA	US	1/10/2014
14/164,045	US 2015-0212736 A1	RAID SET INITIALIZATION	US	1/24/2014
10/180,478	6,714,464	SYSTEM AND METHOD FOR A SELF-CALIBRATING SENSE-AMPLIFIER STROBE	US	6/26/2002
14/265,195	US 2015-0312165 A1	TEMPORAL BASED COLLABORATIVE MUTUAL EXCLUSION CONTROL OF A SHARED RESOURCE	US	4/29/2014
08/421,566	5,701,416	ADAPTIVE ROUTING MECHANISM FOR TORUS INTERCONNECTION NETWORK	US	4/13/1995
08/450,251	5,721,921	BARRIER AND EUREKA SYNCHRONIZATION ARCHITECTURE FOR MULTIPROCESSORS	US	5/25/1995
08/971,184	6,633,958	MULTIPROCESSOR COMPUTER SYSTEM AND METHOD FOR MAINTAINING CACHE COHERENCE UTILIZING A MULTI-DEMENSIONAL CACHE COHERENCE DIRECTORY STRUCTURE	US	11/17/1997
11/405,387	7,433,441	SYSTEM AND METHOD FOR ADAPTIVELY DESKEWING PARALLEL DATA SIGNALS RELATIVE TO A CLOCK	US	4/17/2006
12/247,122	8,031,823	SYSTEM AND METHOD FOR ADAPTIVELY DESKEWING PARALLEL DATA SIGNALS RELATIVE TO A CLOCK	US	10/7/2008

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09/476,678	7,031,420	SYSTEM AND METHOD FOR ADAPTIVELY DESKEWING PARALLEL DATA SIGNALS RELATIVE TO A CLOCK	US	12/30/1999
08/550,992	6,055,618	VIRTUAL MAINTENANCE NETWORK IN MULTIPROCESSING SYSTEM HAVING A NON-FLOW CONTROLLED VIRTUAL MAINTENANCE CHANNEL	US	10/31/1995
29/060,203	D395,286	COMPACT COMPUTER HOUSING	US	9/24/1996
29/065,316	D396,698	COMPACT COMPUTER HOUSING	US	1/23/1997
29/060,131	D393,249	HOUSING FOR DESKSIDE COMPUTER	US	9/23/1996
29/060,425	D393,449	HOUSING FOR A COMPUTER	US	9/27/1996
29/097,545	D431,242	COMPUTER HOUSING	US	12/8/1998
29/096,304	D417,203	COMPUTER HOUSING	US	11/9/1998
08/971,587	5,970,232	ROUTER TABLE LOOKUP MECHANISM	US	11/17/1997
08/971,591	6,101,181	VIRTUAL CHANNEL ASSIGNMENT IN LARGE TORUS SYSTEMS	US	11/17/1997
08/606,291	6,091,155	BGA LAND PATTERN	US	2/23/1996
08/520,408	5,829,512	HEATSINK AND METHOD OF FORMING A HEATSINK	US	8/29/1995
08/422,072	5,659,796	SYSTEM FOR RANDOMLY MODIFYING VIRTUAL CHANNEL ALLOCATION AND ACCEPTING THE RANDOM MODIFICATION BASED ON THE COST FUNCTION	US	4/13/1995
07/710,146	6,282,583	METHOD AND APPARATUS FOR MEMORY ACCESS IN A MATRIX PROCESSOR COMPUTER	US	6/4/1991
08/406,571	5,487,074	BOUNDARY SCAN TESTING USING CLOCKED SIGNAL	US	3/20/1995
08/250,375	5,420,583	COMMUNICATION PROTOCOL FOR TRANSFERRING INFORMATION ACROSS A #S SERIAL COMMUNICATION LINK	US	5/27/1994

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08/407,808	5,592,487	COMMUNICATION PROTOCOL FOR TRANSFERRING INFORMATION ACROSS A #S SERIAL COMMUNICATION LINK	US	3/20/1995
07/788,496	5,390,041	COMMUNICATION PROTOCOL FOR TRANSFERRING INFORMATION ACROSS A #S SERIAL COMMUNICATION LINK	US	11/6/1991
08/661,908	5,797,035	SYSTEM FOR ALLOCATING MESSAGES BETWEEN VIRTUAL CHANNELS TO AVOID DEADLOCK AND TO OPTIMIZE THE AMOUNT OF MESSAGE TRAFFIC ON EACH TYPE OF VIRTUAL CHANNEL	US	6/12/1996
08/662,868	5,737,628	SYSTEM FOR ALLOCATING MESSAGES BETWEEN VIRTUAL CHANNELS TO AVOID DEADLOCK AND TO OPTIMIZE THE AMOUNT OF MESSAGE TRAFFIC ON EACH TYPE OF VIRTUAL CHANNEL	US	6/12/1996
08/165,266	5,583,990	SYSTEM FOR ALLOCATING MESSAGES BETWEEN VIRTUAL CHANNELS TO AVOID DEADLOCK AND TO OPTIMIZE THE AMOUNT OF MESSAGE TRAFFIC ON EACH TYPE OF VIRTUAL CHANNEL	US	12/10/1993
08/165,379	5,586,325	METHOD FOR THE DYNAMIC ALLOCATION OF ARRAY SIZES IN A MULTIPROCESSOR SYSTEM	US	12/10/1993
07/308,401	5,526,487	SYSTEM FOR MULTIPROCESSOR COMMUNICATION	US	2/9/1989
08/003,000	6,195,676	METHOD AND APPARATUS FOR USER SIDE SCHEDULING IN A MULTIPROCESSOR OPERATING SYSTEM PROGRAM THAT IMPLEMENTS DISTRIBUTIVE SCHEDULING OF PROCESSES	US	1/11/1993

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07/976,899		GLOBAL REGISTERS FOR A MULTIPROCESSOR SYSTEM	US	11/16/1992
08/379,123	5,524,255	GLOBAL REGISTERS FOR A MULTIPROCESSOR SYSTEM	US	1/27/1995
07/536,198	5,165,038	GLOBAL REGISTERS FOR A MULTIPROCESSOR SYSTEM	US	6/11/1990
07/459,083	5,197,130	METHOD AND APPARATUS FOR USER SIDE SCHEDULING IN A MULTIPROCESSOR OPERATING SYSTEM PROGRAM THAT IMPLEMENTS DISTRIBUTIVE SCHEDULING OF PROCESSES	US	12/29/1989
07/537,466	5,179,702	METHOD AND APPARATUS FOR USER SIDE SCHEDULING IN A MULTIPROCESSOR OPERATING SYSTEM PROGRAM THAT IMPLEMENTS DISTRIBUTIVE SCHEDULING OF PROCESSES	US	6/11/1990
08/268,660	5,561,784	METHOD AND APPARATUS FOR USER SIDE SCHEDULING IN A MULTIPROCESSOR OPERATING SYSTEM PROGRAM THAT IMPLEMENTS DISTRIBUTIVE SCHEDULING OF PROCESSES	US	6/29/1994
08/889,251	6,119,198	RECURSIVE ADDRESS CENTRIFUGE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS	US	7/8/1997
08/165,388	5,696,922	RECURSIVE ADDRESS CENTRIFUGE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS	US	12/10/1993
08/165,747	5,418,481	REPETITIVE SIGNAL DETECTOR FOR PREVENTING THERMAL RUNAWAY	US	12/10/1993
08/009,576	5,269,698	RETAINING AND RELEASE MECHANISM FOR COMPUTER STORAGE DEVICES INCLUDING A PAWL LATCH ASSEMBLY	US	1/26/1993
08/027,049	5,537,498	OPTICAL CLOCK DISTRIBUTION SYSTEM	US	3/5/1993

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07/923,086	5,495,596	METHOD FOR CLOCKING FUNCTIONAL UNITS IN ONE CYCLE BY USING A SINGLE CLOCK FOR ROUTING CLOCK INPUTS TO INITIATE RECEIVE OPERATIONS PRIOR TO TRANSMIT OPERATIONS	US	7/31/1992
08/340,238	6,173,428	APPARATUS AND METHOD FOR TESTING USING CLOCKED TEST ACCESS PORT CONTROLLER FOR LEVEL SENSITIVE SCAN DESIGNS	US	11/16/1994
08/333,133	5,761,706	STREAM BUFFERS FOR HIGH-PERFORMANCE COMPUTER MEMORY SYSTEMS	US	11/1/1994
08/166,293	5,566,321	METHOD OF MANAGING DISTRIBUTED MEMORY WITHIN A MASSIVELY PARALLEL PROCESSING SYSTEM	US	12/13/1993
08/165,814	5,784,706	VIRTUAL TO LOGICAL TO PHYSICAL ADDRESS TRANSLATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS	US	12/13/1993
08/166,443	5,581,705	MESSAGING FACILITY WITH HARDWARE TAIL POINTER AND SOFTWARE IMPLEMENTED HEAD POINTER MESSAGE QUEUE FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEM	US	12/13/1993
08/166,451	5,802,341	METHOD FOR THE DYNAMIC ALLOCATION OF PAGE SIZES IN VIRTUAL MEMORY	US	12/13/1993
08/205,990	5,834,705	ARRANGEMENT FOR MODIFYING ELECTRICAL PRINTED CIRCUIT BOARDS	US	3/4/1994
07/912,964	5,428,803	EXTENDIBLE CLOCK MECHANISM	US	7/10/1992
08/331,730	5,625,831	EXTENDIBLE CLOCK MECHANISM	US	10/31/1994
08/604,841	6,305,463	AIR OR LIQUID COOLED COMPUTER MODULE COLD PLATE	US	2/22/1996

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08/348,056	5,717,895	ASSOCIATIVE SCALAR DATA CACHE WITH WRITE-THROUGH CAPABILITIES FOR A VECTOR PROCESSOR	US	12/1/1994
08/604,839	5,761,043	DAUGHTER CARD ASSEMBLY	US	2/22/1996
08/605,355	5,768,104	COOLING APPROACH FOR HIGH POWER INTEGRATED CIRCUITS MOUNTED ON PRINTED CIRCUIT BOARDS	US	2/22/1996
08/595,528	5,765,198	TRANSPARENT RELOCATION OF REAL MEMORY ADDRESSES IN THE MAIN MEMORY OF A DATA PROCESSOR	US	2/1/1996
08/903,042	5,867,419	PROCESSOR-INCLUSIVE MEMORY MODULE	US	7/29/1997
08/789,557	5,999,437	PROCESSOR-INCLUSIVE MEMORY MODULE	US	1/27/1997
08/589,532	5,710,733	PROCESSOR-INCLUSIVE MEMORY MODULE	US	1/22/1996
08/592,890	5,654,873	SINGLE CONNECTOR ATTACHMENT DRIVE SLED ASSEMBLY HAVING LIGHT PIPE COUPLED TO A RAIL	US	1/29/1996
08/564,404	5,662,163	READILY REMOVABLE HEAT SINK ASSEMBLY	US	11/29/1995
08/567,082	5,671,235	SCAN CHAIN FOR SHITING THE STATE OF A PROCESSOR INTO MEMORY AT A SPECIFIED POINT DURING SYSTEM OPERATION FOR TESTING PURPOSES	US	12/4/1995
08/521,566	5,848,286	VECTOR WORD SHIFT BY VO SHIFT COUNT IN VECTOR SUPERCOMPUTER PROCESSOR	US	8/30/1995
09/138,613		VECTOR SHIFT FUNCTIONAL UNIT FOR SUCCESSIVELY SHIFTING OPERANDS STORED IN A VECTOR REGISTER BY CORRESPONDING SHIFT COUNTS STORED IN ANOTHER VECTOR REGISTER	US	8/24/1998

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08/218,997	5,481,746	VECTOR SHIFT FUNCTIONAL UNIT FOR SUCCESSIVELY SHIFTING OPERANDS STORED IN A VECTOR REGISTER BY CORRESPONDING SHIFT COUNTS STORED IN ANOTHER VECTOR REGISTER	US	3/29/1994
08/552,801	5,661,638	HIGH PERFORMANCE SPIRAL HEAT SINK	US	11/3/1995
08/551,070	5,709,263	NIGH PERFORMANCE SINUSOIDAL HEAT SINK FOR HEAT REMOVAL FROM ELECTRONIC EQUIPMENT	US	10/19/1995
08/141,259	5,535,365	METHOD AND APPARATUS FOR LOCKING SHARED MEMORY LOCATIONS IN MULTIPROCESSING SYSTEMS	US	10/22/1993
08/165,118	5,765,181	SYSTEM AND METHOD OF ADDRESSING DISTRIBUTED MEMORY WITHIN A MASSIVELY PARALLEL PROCESSING SYSTEM	US	12/10/1993
08/165,265	5,434,995	BARRIER SYNCHRONIZATION FOR DISTRIBUTED MEMORY MASSIVELY PARALLEL PROCESSING SYSTEMS	US	12/10/1993
61/913,901		SERVER EMBEDDED STORAGE DEVICE	US	12/9/2013
14/565,084	US 2015-0163954 A1	SERVER EMBEDDED STORAGE DEVICE	US	12/9/2014
10/660,173	6,847,526	SUB RACK BASED VERTICAL HOUSING FOR COMPUTER SYSTEMS	US	9/11/2003
11/386,382		SUB RACK BASED VERTICAL HOUSING FOR COMPUTER SYSTEMS	US	3/22/2006
09/955,562	6,487,080	SUB RACK BASED VERTICAL HOUSING FOR COMPUTER SYSTEMS	US	9/18/2001
11/012,591	7,193,857	SUB RACK BASED VERTICAL HOUSING FOR COMPUTER SYSTEMS	US	12/15/2004
10/252,654	6,661,667	SUB RACK BASED VERTICAL HOUSING FOR COMPUTER SYSTEMS	US	9/23/2002

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10/200,803	6,765,795	MODULAR FAN BRICK AND METHOD FOR EXCHANGING AIR IN A BRICK-BASED COMPUTER SYSTEM	US	7/23/2002
10/201,230	6,882,531	METHOD AND RACK FOR EXCHANGING AIR WITH MODULAR BRICKS IN A COMPUTER SYSTEM	US	7/23/2002
11/343,968	7,425,117	SYSTEM AND METHOD FOR REDUCING BACK FLOW	US	1/31/2006
11/323,029	7,478,285	GENERATION AND USE OF SYSTEM LEVEL DEFECT TABLES FOR MAIN MEMORY	US	12/30/2005
11/116,734	7,327,167	ANTICIPATORY PROGRAMMABLE INTERFACE PRE-DRIVER	US	4/28/2005
10/691,838	7,152,142	METHOD FOR A WORKLOAD-ADAPTIVE HIGH PERFORMANCE STORAGE SYSTEM WITH DATA PROTECTION	US	10/23/2003
11/592,281	7,222,216	METHOD FOR A WORKLOAD-ADAPTIVE HIGH PERFORMANCE STORAGE SYSTEM WITH DATA PROTECTION	US	11/1/2006
11/585,619	7,603,573	SYSTEM AND METHOD FOR OPTIMIZING COMPUTATIONAL DENSITY	US	10/24/2006
11/261,045	7,466,561	SYSTEM FOR INSERTION AND EXTRACTION OF AN ELECTRONIC MODULE	US	10/28/2005
08/615,694	5,841,973	MESSAGING IN DISTRIBUTED MEMORY MULTIPROCESSING SYSTEM HAVING SHELL CIRCUITRY FOR ATOMIC CONTROL OF MESSAGE STORAGE QUEUE'S TAIL POINTER STRUCTURE IN LOCAL MEMORY	US	3/13/1996
29/108,315	D429,248	BEZEL FOR A COMPUTER	US	7/23/1999
29/113,555	D436,950	RADIAL COMPUTER SYSTEM	US	11/5/1999
29/135,733	D464,973	PANEL	US	1/18/2001
09/006,449		USING EXTERNAL REGISTERS TO EXTEND MEMORY REFERENCE CAPABILITIES OF A MICROPROCESSOR	US	1/13/1998

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08/615,671	5,835,925	USING EXTERNAL REGISTERS TO EXTEND MEMORY REFERENCE CAPABILITIES OF A MICROPROCESSOR	US	3/13/1996
29/135,803	D464,054	PANEL	US	1/18/2001
29/136,032	D463,796	INDUSTRIAL RACK	US	1/24/2001
10/687,196	7,174,437	MEMORY ACCESS MANAGEMENT IN A SHARED MEMORY MULTI-PROCESSOR SYSTEM	US	10/16/2003
10/205,877	7,124,505	BACKSHELL ASSEMBLY	US	7/24/2002
10/231,511	6,726,505	MEMORY DAUGHTER CARD APPARATUS, CONFIGURATIONS, AND METHODS	US	8/29/2002
10/235,221	7,485,003	ELECTROMAGNERIC INTERFERENCE CABLE BACKSHELL ASSEMBLY FOR HIGH-DENSITY INTERCONNECT	US	9/5/2002
10/274,766	6,986,001	SYSTEM AND METHOD FOR HIERARCHICAL APPROXIMATION OF LEAST RECENTLY USED REPLACEMENT ALGORITHMS WITHIN A CACHE ORGANIZED AS TWO OR MORE SUPER-WAYS OF MEMORY BLOCKS	US	10/21/2002
10/356,236	7,302,027	SYNCHRONIZATION CIRCUITS FOR THE DISTRIBUTION OF UNIQUE DATA TO SCATTERED LOCATIONS	US	1/31/2003
10/171,095	7,167,523	SPACIAL DERIVATIVE BUS ENCODER AND DECODER	US	6/13/2002
08/971,185	6,480,548	SPACIAL DERIVATIVE BUS ENCODER AND DECODER	US	11/17/1997
09/934,443	7,249,357	TRANSPARENT DISTRIBUTION AND EXECUTION OF DATA IN A MULTIPROCESSOR ENVIRONMENT	US	8/20/2001
10/160,437	6,672,878	ACTUATABLE CONNECTOR SYSTEM	US	5/31/2002

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10/202,377	6,771,517	PRINTED CIRCUIT BOARD STIFFENER	US	7/26/2002
10/020,854	7,356,026	NODE TRANSLATION AND PROTECTION IN A CLUSTERED MULTIPROCESSOR SYSTEM	US	12/14/2001
10/068,991	6,799,238	BUS SPEED CONTROLLER USING SWITCHES	US	2/7/2002
10/143,413	6,803,872	PROGRAMMABLE DIFFERENTIAL DELAY CIRCUIT WITH FINE DELAY ADJUSTMENT	US	5/9/2002
09/475,466	6,417,713	PROGRAMMABLE DIFFERENTIAL DELAY CIRCUIT WITH FINE DELAY ADJUSTMENT	US	12/30/1999
10/142,472	6,486,723	PROGRAMMABLE DIFFERENTIAL DELAY CIRCUIT WITH FINE DELAY ADJUSTMENT	US	5/9/2002
08/609,068	5,790,612	SYSTEM AND METHOD TO REDUCE JITTER IN DIGITAL DELAY-LOCKED LOOPS	US	2/29/1996
08/614,860	6,233,704	SYSTEM AND METHOD FOR FAULT-TOLERANT TRANSMISSION OF DATA WITHIN A DUAL RING NETWORK	US	3/13/1996
08/611,785	5,757,658	PROCEDURE AND SYSTEM FOR PLACEMENT OPTIMIZATION OF CELLS WITHIN CIRCUIT BLOCKS BY OPTIMIZING PLACEMENT OF INPUT/OUTPUT PORTS WITHIN AN INTEGRATED CIRCUIT DESIGN	US	3/6/1996
08/614,859	5,864,738	MASSIVELY PARALLEL PROCESSING SYSTEM USING TWO DATA PATHS: ONE CONNECTING ROUTER CIRCUIT TO THE INTERCONNECT NETWORK AND THE OTHER CONNECTING ROUTER CIRCUIT TO I/O CONTROLLER	US	3/13/1996
10/632,681	7,100,018	SYSTEM AND METHOD FOR ENCODING PAGE SIZE INFORMATION	US	7/31/2003

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10/017,488	6,925,547	REMOTE ADDRESS TRANSLATION IN A MULTIPROCESSOR SYSTEM	US	12/14/2001
10/632,131	7,089,398	ADDRESS TRANSLATION USING A PAGE SIZE TAG	US	7/31/2003
10/785,575	7,370,154	METHOD AND APPARATUS FOR MAINTAINING COHERENCE INFORMATION IN MULTI-CACHE SYSTEMS	US	2/24/2004
90/013,174		MESSAGE-PASSING MULTIPROCESSOR SYSTEM	US	3/7/2014
61/859,521		I/O ACCELERATION IN HYBRID STORAGE	US	7/29/2013
14/335,752	US 2015-0032921 A1	I/O ACCELERATION IN HYBRID STORAGE	US	7/18/2014
14/328,423	US 2015-0019807 A1	LINEARIZED DYNAMIC STORAGE POOL	US	7/10/2014
61/845,162		LINEARIZED DYNAMIC STORAGE POOL	US	7/11/2013
08/988,524	5,946,496	DISTRIBUTED VECTOR ARCHITECTURE	US	12/10/1997
		A FLEXIBLE, SCALABLE, AND INTEGRATED BIG DATA ECOSYSTEM FOR DATA INGESTION, ANALYTICS, AND VISUALIZATION	US	
61/985,354		UTILIZING NOSQL GRAPH DATABASES FOR GENE DETECTION, CANCER PREDICTION AND DRUG DISCROVERY	US	4/28/2014
14/698,029		ING NOSQL GRAPH DATABASES FOR GENE DETECTION, CANCER PREDICTION AND DRUG DISCOVERY	US	4/28/2015
61/985,378		ANALYZING DNA SEQUENCES USING DECISION TREE CLASSIFICATION AND STATISTICAL LEARNING WITHIN A GRAPH DATABASE	US	4/28/2014
14/698,177		ANALYZING DNA SEQUENCES USING DECISION TREE CLASSIFICATION AND STATISTICAL LEARNING WITHIN A GRAPH DATABASE	US	4/28/2015

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08/718,743	5,812,754	RAID SYSTEM WITH FIBRE CHANNEL ARBITRATED LOOP	US	9/18/1996
08/708,298	5,875,468	METHOD TO PIPELINE WRITE MISSES IN SHARED CACHE MULTIPROCESSOR SYSTEMS	US	9/4/1996
08/675,849	5,818,250	APPARATUS AND METHOD FOR DETERMINING THE SPEED OF A SEMICONDUCTOR CHIP	US	7/3/1996
08/788,369	5,825,238	CIRCUIT FOR FILTERING A POWER SUPPLY FOR NOISE SENSITIVE DEVICES	US	1/27/1997
09/475,469	6,381,139	CARRIER FOR COMPUTER PERIPHERAL DEVICE	US	12/30/1999
09/408,769	6,406,257	MODULAR AIR MOVING SYSTEM AND METHOD	US	9/29/1999
09/408,084	6,604,161	TRANSLATION OF PCI LEVEL INTERRUPTS INTO PACKET BASED MESSAGES FOR EDGE EVENT DRIVE MICROPROCESSORS	US	9/29/1999
09/418,706	6,856,950	ABSTRACT VERIFICATION ENVIRONMENT	US	10/15/1999
09/409,438	6,601,183	DIAGNOSTIC SYSTEM AND METHOD FOR A HIGHLY SCALABLE COMPUTING SYSTEM	US	9/30/1999
09/409,299	6,553,446	MODULAR INPUT/OUTPUT CONTROLLER CAPABLE OF ROUTING PACKETS OVER BUSSES OPERATING AT DIFFERENT SPEEDS	US	9/29/1999
09/408,778	6,674,720	AGE-BASED NETWORK ARBITRATION SYSTEM AND METHOD	US	9/29/1999
09/498,939	6,169,659	METERED FORCE SINGLE POINT HEATSINK ATTACH MECHANISM	US	2/4/2000
09/541,068	6,680,636	METHOD AND SYSTEM FOR CLOCK CYCLE MEASUREMENT AND DELAY OFFSET	US	3/31/2000
09/408,657	6,496,385	METHOD AND ASSEMBLY FOR INSTALLATION OR REMOVAL OF PRINTED CIRCUIT CARD	US	9/29/1999

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09/346,659	6,256,196	DESIGN FOR CIRCUIT BOARD ORTHOGONAL INSTALLATION AND REMOVAL	US	7/1/1999
09/542,791	6,760,876	SCAN INTERFACE CHIP (SIC) SYSTEM AND METHOD FOR SCAN TESTING ELECTRONIC SYSTEMS	US	4/4/2000
09/372,660	6,132,019	DOOR ASSEMBLY FOR A COMPUTER	US	8/11/1999
09/478,968	6,280,257	CABLE DOCK FIXTURE WITH EMI SHIELDING	US	1/6/2000
09/408,772	6,366,461	SYSTEM AND METHOD FOR COOLING ELECTRONIC COMPONENTS	US	9/29/1999
09/137,017	6,275,239	MEDIA COPROCESSOR WITH GRAPHICS VIDEO AND AUDIO TASKS PARTITIONED BY TIME DIVISION MULTIPLEXING	US	8/20/1998
08/920,177	5,987,626	PRECISE DETECTION OF ERRORS USING HARDWARE WATCHPOINT MECHANISM	US	8/25/1997
09/118,158	6,226,330	EIGEN-MODE ENCODING OF SIGNALS IN A DATA GROUP	US	7/16/1998
09/215,531	6,167,947	HIGH PERFORMANCE GAS COOLING SYSTEM AND METHOD	US	12/18/1998
09/176,696	6,128,731	ADVANCED BOOT SEQUENCE FOR AN X86 COMPUTER SYSTEM THAT MAINTAINS EXPANSION CARD DEVICE COMPATIBILITY	US	10/21/1998
09/176,694	6,357,003	ADVANCED FIRMWARE BOOT SEQUENCE X86 COMPUTER SYSTEM THAT MAINTAINS LEGACY HARDWARE AND SOFTWARE COMPATIBILITY	US	10/21/1998
09/162,673	6,216,174	SYSTEM AND METHOD FOR FAST BARRIER SYNCHRONIZATION	US	9/29/1998
09/287,592	6,496,909	METHOD FOR MANAGING CONCURRENT ACCESS TO VIRTUAL MEMORY DATA STRUCTURES	US	4/6/1999

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08/940,273	5,924,780	SLIDING DOOR ASSEMBLY FOR A COMPUTER HOUSING	US	9/30/1997
09/294,830	6,223,270	METHOD FOR EFFICIENT TRANSLATION OF MEMORY ADDRESSES IN COMPUTER SYSTEMS	US	4/19/1999
09/097,601	6,208,361	METHOD AND SYSTEM FOR EFFICIENT CONTEXT SWITCHING IN A COMPUTER GRAPHICS SYSTEM	US	6/15/1998
08/911,909	5,967,825	INTEGRAL ACTUATOR FOR A PRINTED CIRCUIT BOARD	US	8/15/1997
09/265,487	6,317,126	METHOD AND DEVICE FOR ASSOCIATING A PIXEL WITH ONE OF A PLURALITY OF REGIONS IN A LOGARITHM OR COSINE SPACE	US	3/9/1999
09/005,219	6,171,120	MODULAR CARD CAGE	US	1/9/1998
09/005,129	6,292,192	SYSTEM AND METHOD FOR THE DIRECT RENDERING OF CURVE BOUNDED OBJECTS	US	1/9/1998
08/987,948	5,913,069	INTERLEAVING MEMORY IN DISTRIBUTED VECTOR ARCHITECTURE MULTIPROCESSOR SYSTEM	US	12/10/1997
08/985,562	6,044,424	IMPROVED HOT- PLUG POWER SUPPLY FOR HIGH-AVAILABILITY COMPUTER SYSTEMS	US	12/5/1997
09/056,037	6,055,157	LARGE AREA, MULTI-DEVICE HEAT PIPE FOR STACKED MCM-BASED SYSTEMS	US	4/6/1998
09/055,677	6,172,874	SYSTEM AND FOR STACKING OF INTEGRATED CIRCUIT PACKAGES	US	4/6/1998
09/055,554	6,181,231	DIAMOND-BASED TRANSFORMERS AND POWER CONVERTORS	US	4/6/1998
09/021,651	6,092,226	THE FABRICATION OF TEST LOGIC FOR LEVEL SENSITIVE SCAN ON A CIRCUIT	US	2/10/1998
08/971,179	6,018,459	POROUS METAL HEAT SINK	US	11/17/1997
08/966,611	5,907,962	LATCHING ASSEMBLY FOR A COMPUTER	US	11/10/1997
08/927,359	6,116,915	STOP ALIGN LATERAL MODULE TO MODULE INTERCONNECT	US	9/9/1997

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08/801,646	6,766,515	DISTRIBUTED SCHEDULING OF PARALLEL JOBS WITH NO KERNEL-TO-KERNEL COMMUNICATION	US	2/18/1997
08/802,802	6,418,460	SYSTEM AND METHOD FOR FINDING PREEMPTED THREADS IN A MULTI-THREADED APPLICATION	US	2/18/1997
08/815,636	5,826,922	ROTARY LATCH ASSEMBLY FOR A COMPUTER HOUSING	US	3/13/1997
08/796,129	5,991,824	METHOD AND SYSTEM FOR SIMULTANEOUS HIGH BANDWIDTH INPUT OUTPUT	US	2/6/1997
08/796,302	5,848,906	LOADING AND PLACEMENT DEVICE FOR CONNECTING CIRCUIT BOARDS	US	2/7/1997
08/794,195	5,817,997	POWER SWITCH PLUNGER MECHANISM	US	1/24/1997
08/773,486	6,353,844	GUARANTEEING COMPLETION TIMES FOR BATCH JOBS WITHOUT STATIC PARTITIONING	US	12/23/1996
08/752,925	5,928,322	LOW-LATENCY REAL-TIME DISPATCHING IN GENERAL PURPOSE MULTIPROCESSOR SYSTEMS	US	11/20/1996
08/780,781	5,915,104	HIGH BANDWIDTH PCI TO PACKET SWITCHED ROUTER BRIDGE HAVING MINIMIZED MEMORY LATENCY	US	1/9/1997
08/775,834	6,065,084	PROGRAMMABLE PACKER AND UNPACKER WITH DITHERER	US	12/31/1996
08/717,988	5,957,556	CABLE MANAGEMENT SYSTEM FOR A COMPUTER	US	9/23/1996
08/713,283	5,730,605	COMPRESSION CONNECTOR	US	9/12/1996
08/713,602	6,108,722	DIRECT MEMORY ACCESS APPARATUS FOR TRANSFERRING A BLOCK OF DATA HAVING DISCONTINUOUS ADDRESSES USING AN ADDRESS CALCULATING CIRCUIT	US	9/13/1996
08/716,928	5,897,180	RESILIENT PANEL FOR HOUSING A MACHINE	US	9/23/1996

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08/716,972	5,812,147	INSTRUCTION METHODS FOR PERFORMING DATA FORMATTING WHILE MOVING DATA BETWEEN MEMORY AND A VECTOR REGISTER FILE	US	9/20/1996
08/706,808	5,940,625	DENSITY DEPENDENT VECTOR MASK OPERATION CONTROL APPARATUS AND METHOD	US	9/3/1996
08/697,073	5,770,822	BULKHEAD GASKET ASSEMBLY	US	8/19/1996
08/688,501	5,774,704	APPARATUS AND METHOD FOR DYNAMIC CENTRAL PROCESSING UNIT CLOCK ADJUSTMENT	US	7/29/1996
08/673,436	5,900,023	METHOD AND APPARATUS FOR REMOVING POWER-OF-TWO RESTRICTIONS ON DISTRIBUTED ADDRESSING	US	6/28/1996
08/650,630	5,761,534	A SYSTEM FOR ARBITRATING PACKETIZED DATA FROM THE NETWORK TO THE PERIPHERAL RESOURCES AND PRIORITIZING THE DISPATCHING OF PACKETS ONTO THE NETWORK	US	5/20/1996
08/650,632	5,862,313	A RAID SYSTEM USING I/O BUFFER SEGMENT TO TEMPORARY STORE STRIPED AND PARITY DATA AND CONNECTING ALL DISK DRIVES VIA A SINGLE TIME MULTIPLEXED NETWORK	US	5/20/1996
08/650,337	5,694,028	METHOD AND APPARATUS FOR ADJUSTING THE POWER SUPPLY VOLTAGE PROVIDED TO A MICROPROCESSOR	US	5/20/1996
08/650,336	5,805,788	RAID-5 PARITY GENERATION AND DATA RECONSTRUCTION	US	5/20/1996
08/649,769	5,735,340	HEAT SINK WITH INTEGRAL ATTACHMENT MECHANISM	US	5/15/1996
11/334,526	8,078,907	FAILSOFT SYSTEM FOR MULTIPLE CPU SYSTEM	US	1/19/2006
10/365,658	7,451,278	GLOBAL POINTERS FOR SCALABLE PARALLEL APPLICATIONS	US	2/13/2003

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09/103,201	6,308,250	METHOD AND APPARATUS FOR PROCESSING A SET OF DATA VALUES WITH PLURAL PROCESSING UNITS USING MASK BITS GENERATED BY OTHER PROCESSING UNITS	US	6/23/1998
09/408,969	6,193,532	PRINTED CIRCUIT BOARD CARRIER INSERTION/EXTRACTION ASSEMBLY	US	9/29/1999
09/408,874	6,829,666	MODULAR COMPUTING ARCHITECTURE HAVING COMMON COMMUNICATION INTERFACE	US	9/29/1999
09/407,421	6,711,636	TRANSFER ATTRIBUTE ENCODING WITHIN PCI CONSTRUCTED ADDRESS TO INDICATE WHETHER BYTES WITHIN A WORD SHOULD BE SWAPPED	US	9/29/1999
09/391,133	6,541,853	ELECTRICALLY CONDUCTIVE PATH THROUGH A DIELECTRIC MATERIAL	US	9/7/1999
09/196,624	6,078,515	MEMORY SYSTEM WITH MULTIPLE ADDRESSING AND CONTROL BUSSES	US	11/18/1998
09/060,451	5,870,325	MEMORY SYSTEM WITH MULTIPLE ADDRESSING AND CONTROL BUSSES	US	4/14/1998
09/384,906	6,775,339	CIRCUIT DESIGN FOR HIGH-SPEED DIGITAL COMMUNICATION	US	8/27/1999
09/408,148	6,452,805	COMPUTER MODULE MOUNTING SYSTEM AND METHOD	US	9/29/1999
09/548,497	6,574,121	COMPUTER MODULE MOUNTING SYSTEM AND METHOD	US	4/13/2000
09/388,938	6,389,581	OPTIMIZING REPEATERS POSITIONING ALONG INTERCONNECTS	US	9/2/1999
09/387,934	6,353,917	DETERMINING A WORST CASE SWITCHING FACTOR FOR INTEGRATED CIRCUIT DESIGN	US	9/1/1999
11/268,164	8,407,424	DATA COHERENCY METHOD AND APPARATUS FOR	US	11/7/2005

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		MULTI-NODE COMPUTER SYSTEM		
11/620,215	8,036,247	SYSTEM AND METHOD OF SNYCHRONIZING REAL TIME CLOCK VALUES IN ARBITRARY DISTRIBUTED SYSTEMS	US	1/5/2007
10/435,211	6,975,510	VENTILATED HOUSING FOR ELECTRONIC COMPONENTS	US	5/9/2003
11/232,399	7,227,751	VENTILATED HOUSING FOR ELECTRONIC COMPONENTS	US	9/21/2005
10/912,722	7,590,775	METHOD FOR EMPIRICALLY DETERMINING A QUALIFIED BANDWIDTH OF FILE STORAGE FOR A SHARED FILED SYSTEM	US	8/6/2004
08/935,667	5,958,017	ADAPTIVE CONGESTION CONTROL MECHANISM FOR MODULAR COMPUTER NETWORKS	US	9/23/1997
08/615,700	5,748,900	ADAPTIVE CONGESTION CONTROL MECHANISM FOR MODULAR COMPUTER NETWORKS	US	3/13/1996
08/717,581	5,784,569	GUARANTEED BANDWIDTH ALLOCATION METHOD IN A COMPUTER SYSTEM FOR INPUT/OUTPUT DATA TRANSFERS	US	9/23/1996
08/718,765	6,067,411	ADAPTIVE FREQUENCY SYNTHESIZER WITH SYNCHRONIZATION	US	9/23/1996
09/384,471		MEMORY SYSTEM WITH SWITCHING FOR DATA ISOLATION	US	8/27/1999
09/247,256	6,115,278	MEMORY SYSTEM WITH SWITCHING FOR DATA ISOLATION	US	2/9/1999
09/057,701	6,081,882	QUANTUM ACCELERATION OF CONVENTIONAL NON-QUANTUM COMPUTERS	US	4/9/1998
08/931,565	6,205,119	ADAPTIVE BANDWIDTH SHARING	US	9/16/1997
08/991,233	6,256,677	MESSAGE BUFFERING FOR A COMPUTER-BASED NETWORK	US	12/16/1997

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08/972,010	6,085,303	SERIALIZED RACE-FREE VIRTUAL BARRIER NETWORK	US	11/17/1997
08/971,588	6,230,252	HYBRID HYPERCUBE/TORUS ARCHITECTURE	US	11/17/1997
08/934,973	6,142,789	DEMATEABLE, COMPLIANT, AREA ARRAY INTERCONNECT	US	9/22/1997
09/174,862	6,128,639	ARRAY ADDRESS AND LOOP ALIGNMENT CALCULATIONS	US	10/19/1998
61/901,731		SHARED MEMORY EIGENSOLVER	US	11/8/2013
14/537,839	US 2015-0134714 A1	SHARED MEMORY EIGENSOLVER	US	11/10/2014
15/132,085		SHARED MEMORY EIGENSOLVER	US	4/18/2016
08/541,803	5,689,646	DIRECTION ORDER PRIORITY ROUTING OF PACKETS BETWEEN NODES IN A NETWORKED SYSTEM	US	10/10/1995
07/983,979	5,533,198	DIRECTION ORDER PRIORITY ROUTING OF PACKETS BETWEEN NODES IN A NETWORKED SYSTEM	US	11/30/1992
14/710,492		SCALABLE SOFTWARE STACK	US	5/12/2015
62/149,061		PLASMA EIGENSOLUTION ON LARGE SCALE CACHE-COHERENT SHARED MEMORY SYSTEMS	US	4/17/2015
61/973,622		MATHEMATICAL MODELING TOOL	US	4/1/2014
09/679,447	RE38,134	SYSTEM FOR COMMUNICATIONS WHERE FIRST PRIORITY DATA TRANSFER IS NOT DISTURBED BY SECOND PRIORITY DATA TRANSFER AND WHERE ALLOCATED BANDWIDTH IS REMOVED WHEN PROCESS TERMINATES ABNORMALLY	US	10/3/2000
09/136,908	5,963,428	COOLING CAP METHOD AND APPARATUS FOR TAB PACKAGED INTEGRATED CIRCUITS	US	8/20/1998
11/470,551	8,429,274	STORAGE RESOURCE SCAN	US	9/6/2006

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08/551,493	5,727,197	METHOD AND APPARATUS FOR SEGMENTING A DATABASE	US	11/1/1995
09/036,671	6,049,804	METHOD AND APPARATUS FOR SEGMENTING A DATABASE	US	3/9/1998
11/470,537	7,512,756	PERFORMANCE IMPROVEMENT FOR BLOCK SPAN REPLICATION	US	9/6/2006
11/470,548	7,676,682	LIGHTWEIGHT MANAGEMENT AND HIGH AVAILABILITY CONTROLLER	US	9/6/2006
11/470,539	7,721,025	REUSING TASK OBJECT AND RESOURCES	US	9/6/2006
11/470,550	8,015,270	REDUNDANT APPLIANCE CONFIGURATION REPOSITORY IN STANDARD HIERARCHICAL FORMAT	US	9/6/2006
11/470,544	7,734,882	GENERATING DIGEST FOR BLOCK RANGE VIA ISCSI	US	9/6/2006
11/470,542		INCREMENTAL REPLICATION USING SNAPSHOTS	US	9/6/2006
11/470,545		BLOCK SNAPSHOTS OVER iSCSI	US	9/6/2006
09/608,378	6,483,024	PANEL GASKET	US	6/30/2000
09/522,695	6,845,410	SYSTEM AND METHOD FOR A HIERARCHICAL SYSTEM MANAGEMENT ARCHITECTURE OF A HIGHLY SCALABLE COMPUTING SYSTEM	US	3/10/2000
09/644,698	7,219,156	SYSTEM AND METHOD FOR A HIERARCHICAL SYSTEM MANAGEMENT ARCHITECTURE OF A HIGHLY SCALABLE COMPUTING SYSTEM	US	8/24/2000
09/620,504	6,684,373	OPTIMIZE GLOBAL NET TIMING WITH REPEATER BUFFERS	US	7/20/2000
09/620,059	6,487,082	PRINTED CIRCUIT BOARD COMPONENT PACKAGING	US	7/20/2000
09/301,863	6,732,065	NOISE ESTIMATION FOR COUPLED RC INTERCONNECTS IN DEEP SUBMICRON INTEGRATED CIRCUITS	US	4/29/1999

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62/252,946		FLOATING LIQUID COOLED HEAT TRANSFER SOLUTION	US	11/9/2015
62/249,024		CONFIGURABLE NODE EXPANSION SPACE	US	10/30/2015
62/249,038		NODE BLIND MATE LIQUID COOLING	US	10/30/2015
09/619,724	6,703,908	I/O IMPEDANCE CONTROLLER	US	7/20/2000
62/250,275		STORAGE ERROR TYPE DETERMINATION	US	11/3/2015
62/255,832		ZERO COPY ARCHITECTURE (ZCA) FOR BURST BUFFER AND IN SITU ANALYTICS, VISUALIZATION AND COMPUTATIONAL STEERING	US	11/16/2015
13/931,754	US 2014-0124168 A1	CLOSED -LOOP COOING SYSTEM FOR HIGH-DENSITY CLUSTERED COMPUTER SYSTEM	US	6/28/2013
PCT/US14/ 17291		ACTIVE ARCHIVE BRIDGE	PCT	2/20/2014
PCT/US14/ 17293		ELASTIC HIERARCHICAL DATA STORAGE BACKEND	PCT	2/20/2014
PCT/US02/ 05779		METHOD AND SYSTEM FOR CACHE COHERENCE IN DSM MULTIPROCESSOR SYSTEM WITHOUT GROWTH OF THE SHARING VECTOR	PCT	2/28/2002
PCT/US04/ 14941	WO 2004/102354	COMPUTER RACK WITH POWER DISTRIBUTION SYSTEM	PCT	5/12/2004
PCT/IB2005 /003706		METHOD AND SYSTEM FOR NETWORK STORAGE DEVICE FAILURE PROTECTION AND RECOVERY	PCT	11/3/2005
PCT/IB2004 /003755		METHOD FOR RETRIEVING AND MODIFYING DATA ELEMENTS ON A SHARED MEDIUM	PCT	11/16/2004
PCT/US96/ 06216	WO 1996/35178	SOURCE SYNCHRONOUS CLOCKED DATA LINK	PCT	4/26/1996
PCT/US14/ 44924		REPLICATED DATABASE USING ONE SIDED RDMA	PCT	6/30/2014
PCT/US14/ 44930		SOFTWARE DESIGN PATTERN FOR ADAPTING A GRAPH DATABASE VISUALIZATION SOFTWARE	PCT	6/30/2014

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PCT/US15/11053	WO 2015/106214	VISUALLY APPROXIMATING PARALLEL COORDINATES DATA	PCT	1/12/2015
PCT/US2014/069400		SERVER EMBEDDED STORAGE DEVICE	PCT	12/9/2014
PCT/US2014/047305		I/O ACCELERATION IN HYBRID STORAGE	PCT	7/18/2014
PCT/US14/46222		LINEARIZED DYNAMIC STORAGE POOL	PCT	7/10/2014
PCT/US14/64888		SHARED MEMORY EIGENSOLVER	PCT	11/10/2014
PCT/US2016/032117		SCALABLE SOFTWARE STACK	PCT	5/12/2016
11/121,975		Liquid DIMM Cooler	US	5/4/2005
11/113,805	7,464,115	Node Synchronization for Multi-Processor Computer Systems	US	4/25/2005
11/136,260	7,765,454	Fault Tolerant Memory System	US	5/24/2005
60/676,551		Directory Delegation and Update Pushing in Shared Memory Microprocessor Systems	US	4/29/2005
11/235,493	7,533,208	Hot Plug Control Apparatus and Method	US	9/26/2005
PCT/US2008/050314		System and Method of Synchronizing Real Time Clock Values in Arbitrary Distributed Systems	PCT	1/4/2008
8727372.8		System and Method of Synchronizing Real Time Clock Values in Arbitrary Distributed Systems	EP	1/4/2008
11/413,620	7,386,680	Apparatus and Method of Controlling Data Sharing on a Shared Memory Computer System	US	4/28/2006
11/685,750	7,831,746	Direct Memory Access Engine for Data Transfers	US	3/13/2007
12/039,048	8,239,566	Non-Saturating Fairness Protocol and Method for Nacking Systems	US	2/28/2008
12/330,413		Node Synchronization for Multi-Processor Computer Systems	US	12/8/2008
12/463,941	7,868,656	Hot Plug Control Apparatus and Method	US	5/11/2009
11/677,460	8,713,576	Load Balancing for Parallel Tasks	US	2/21/2007
12/538,020	7,908,410	Method for Empirically Determining a Qualified Bandwidth of File Storage for a Shared Filed System Using a	US	8/7/2009

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		Guaranteed Rate I/O (GRIO) or Non-GRIO Process		
12/941,492		Direct Memory Access Engine for Data Transfers	US	11/8/2010
13/270,002	8,498,315	System and Method of Synchronizing Real Time Clock Values in Arbitrary Distributed Systems	US	10/10/2011
61/783,544		Allocating Accelerators to Threads in a High Performance Computing System	US	3/14/2013
61/783,791		Apparatus and Method for Providing Information About Organization of Resources in a High Performance Computing System	US	3/14/2013
13/833,956	9,176,669	Address Resource Mapping in a Shared Memory Computer System	US	3/15/2013
13/798,604	9,104,343	Global Synchronous Clock Circuit and Method for Blade Processors (as amended)	US	3/13/2013
13/780,248	9,389,940	System and Method for Error Logging	US	2/28/2013
13/802,086		An Associative Look-up Instruction for a Processor Instruction Set Architecture	US	3/13/2013
13/801,841	9,250,826	Enhanced Performance Monitoring Method and Apparatus	US	3/13/2013
13/784,160		First-in First-Out (FIFO) Modular Memory Structure	US	3/4/2013
13/788,281	8,892,805	High Performance System that Includes Reconfigurable Protocol Tables Within an Asic Wherein a First Protocol Block Implements an Inter-Asic Communications Protocol and a Second Block Implements an Intra-Asic Function	US	3/7/2013
13/804,537		Maintaining Coherence When Removing Nodes From a Directory-Based Shared Memory System	US	3/14/2013
13/828,896		Synchronizing Scheduler Interrupts Across Multiple Computing Nodes	US	3/14/2013

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13/804,532		Apparatus and Methods for Providing Performance Data of Nodes in a High Performance Computing System	US	3/14/2013
13/830,432	9,237,093	Bandwidth On-Demand Adaptive Routing	US	3/14/2013
13/848,546	8,812,765	Data Coherence Method and Apparatus for Multi-Node Computer System	US	3/21/2013
13/900,757		Allocating Accelerators to Threads in a High Performance Computing System	US	5/23/2013
61/806,716		Localized Fast Bulk Storage in a Multi-Node Computer System	US	3/29/2013
61/817,928		Scalable Matrix Multiplication in a Shared Memory System	US	5/1/2013
13/928,050		Assessment of a High Performance Computing Application in Relation to Network Latency Due to the Chosen Interconnects	US	6/26/2013
13/930,955		High Performance Computing Network Activity Tracking Tool	US	6/28/2013
13/931,730	9,229,497	On-blade Cold Sink for High-Density Clustered Computer System	US	6/28/2013
PCT/US2013/061374		On-blade Cold Sink for High-Density Clustered Computer System	PCT	9/24/2013
PCT/US2013/061392		Twin Server Blades for High-Density Clustered Computer System	PCT	9/24/2013
13853840		Twin Server Blades for High-Density Clustered Computer System	EP	9/24/2013
2015-541765		Twin Server Blades for High-Density Clustered Computer System	JP	9/24/2013
13/931,748		Twin Server Blades for High-Density Clustered Computer System	US	6/28/2013
13/949,920	9,128,682	Independent Removable Computer Rack Power Distribution System for High-Density Clustered Computer System	US	7/24/2013
PCT/US2013/061424		Independent Removable Computer Rack Power Distribution System	PCT	9/24/2013

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		for High-Density Clustered Computer System		
PCT/US2013/061469		Closed-loop Cooling System for High-Density Clustered Computer System	PCT	9/24/2013
13852972.2		Closed-loop Cooling System for Computer System	EP	9/24/2013
2015-541767		Closed-loop Cooling System for Computer System	JP	9/24/2013
13/931,754		Closed-loop Cooling System for High-Density Clustered Computer System	US	6/28/2013
PCT/US2014/030983		Localized Fast Bulk Storage in a Multi-Node Computer System	PCT	3/18/2014
13/931,861		Localized Fast Bulk Storage in a Multi-Node Computer System	US	6/29/2013
13/931,870	9,268,684	Populating Localized Fast Bulk Storage in a Multi-Node Computer System	US	6/29/2013
PCT/US2014/31003		Populating Localized Fast Bulk Storage in a Multi-Node Computer System	PCT	3/18/2014
14/041,974		Scalable Matrix Multiplication in a Shared Memory System	US	9/30/2013
61/901,731		Shared Memory Eigensolver	US	11/8/2013
14/102,121		Hot Swappable Computer Cooling System	US	12/10/2013
PCT/US2014/068329		Liquid Cooling System for a Hot Swappable Computer System (as amended by the ISA)	PCT	12/3/2014
61/908,433		Remote Actuated Leveling Mechanism	US	11/25/2013
14/536,477	9,262,799	Shared Memory Eigensolver	US	11/7/2014
14/229,796	9,252,812	Low Latency Serial Data Encoding Scheme For Enhanced Burst Error Immunity and Long Term Reliability	US	3/28/2014
PCT/US2015/022935		Low Latency Serial Data Encoding Scheme for Enhanced Burst Error Immunity (as amended by ISA)	PCT	3/27/2015
15767933.3		Low Latency Serial Data Encoding Scheme for Enhanced Burst Error Immunity (as amended by ISA)	EP	3/27/2015

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2017-502938		Low Latency Serial Data Encoding Scheme for Enhanced Burst Error Immunity (as amended by ISA)	JP	3/27/2015
PCT/US2015/022181		High Speed Serial Link In-Band Lane Fail Over for RAS and Power Management	PCT	3/24/2015
14/224,795		High Speed Serial Link In-Band Lane Fail Over for RAS and Power Management	US	3/25/2014
15769516.4		High Speed Serial Link In-Band Lane Fail Over for RAS and Power Management	EP	3/24/2015
2016-558731		High Speed Serial Link In-Band Lane Fail Over for RAS and Power Management	JP	3/24/2015
61/951,792		Apparatus and Method of Resolving Protocol Conflicts in an Unordered Network	US	3/12/2014
61/973,622		Methematical Modeling Tool	US	4/1/2014
14/550,444		Remote Actuated Leveling Mechanism	US	11/21/2014
14/542,023	9,122,816	High Performance System that includes Reconfigurable Protocol Tables within an Asic wherein a First Protocol Block Implements an Inter-Asic Communications Protocol and a Second Block Implements an Intra-Asic Function	US	11/14/2014
PCT/US2015/020126		Apparatus and Method of Resolving Protocol Conflicts in an Unordered Network	PCT	3/12/2015
14/644,629		Apparatus and Method of Resolving Protocol Conflicts in an Unordered Network	US	3/11/2015
15761069.2		Apparatus and Method of Resolving Protocol Conflicts in an Unordered Network	EP	3/12/2015
2016-575617		Apparatus and Method of Resolving Protocol Conflicts in an Unordered Network	JP	3/12/2015
14/709,201**		Method and Apparatus for Managing Nodal Power in a High Performance Computer System	US	5/11/2015
14/742,007		Method and System for High Speed Data Links	US	6/17/2015

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62/169,058		Managing Power in a High Performance Computer System for Error Avoidance or Cooling	US	6/1/2015
PCT/US201 6/031001		Managing Power in a High Performance Computing System for Resiliency and Cooling	PCT	5/5/2016
15/148,242		Managing Power in a High Performance Computing System for Resiliency and Cooling	US	5/6/2016
15/177,609		Method for Error Logging	US	6/9/2016
62/362,911		Caching Network Fabric for High Preformance Computing	US	7/15/2016
62/363,014		Workload Management System and Process	US	7/15/2016
15/357,479		Adaptive Routing for Link-Level Retry Protocol	US	11/21/2016
15/427,941		Packet-Based Adaptive Forward Error Correction	US	2/8/2017
15/483,880		Virtual Channel and Resource Assignment	US	4/10/2017
15/262,571		Assessment of a High Performance Computing Application in Relation to Network Latency Due to the Chosen Interconnects	US	9/12/2016
15/370,485		Predictive Arbitration Circuit	US	12/6/2016
15/370,508		Age-Based Arbitration Circuit	US	12/6/2016
15/370,529		Shared-Credit Arbitration Circuit	US	12/6/2016
15/370,545		Scripted Arbitration Circuit	US	12/6/2016
15/332,290		Localized Fast Bulk Storage in a Multi-Node Computer System	US	10/24/2016
15/453,576		Closed-loop Cooling System for High-Density Clustered Computer System	US	3/8/2017
62/460,402		Valved Connector	US	2/17/2017
15/457,204		Maintaining Coherence When Removing Nodes From a Directory-Based Shared Memory System	US	3/13/2017
14832889.1		I/O ACCELERATION IN HYBRID STORAGE	EP	
2001-526728	4480315	NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM	JP	
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963600.2	1224553	MULTI-PROCESSOR SYSTEM AND METHOD OF ACCESSING DATA THEREIN	FR	
3733979.3	1504343	REAL-TIME STORAGE AREA NETWORK	DE	
2004819660	ZL200480019660	Computer rack with power distribution system	CN	
7100323.1	1094061	A RACK MOUNTED COMPUTER APPARATUS	HK	
93113750	I368128	Computer rack with power distribution system	TW	
5809012.7			EP	
97937252.1	927477	PACKET SWITCHED ROUTER ARCHITECTURE FOR PROVIDING MULTIPLE SIMULTANEOUS COMMUNICATIONS	DE	
2001-526730	4472909	MULTIPROCESSOR NODE CONTROLLER CIRCUIT AND METHOD	JP	
2001-527284	3856696	CONFIGURABLE SYNCHRONIZER FOR DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY	JP	
2001-526712	3825692	METHOD AND APPARATUS FOR HANDLING INVALIDATION REQUESTS TO PROCESSORS NOT PRESENT IN A COMPUTER SYSTEM	JP	
11-236161	4204713	DISPLAY METHOD FOR THREE-DIMENSIONAL MODEL, AND COMPUTER-READABLE STORAGE MEDIUM STORED WITH PROGRAM ACTUALIZING SAME	JP	
200680007567.5	ZL200680007567.5		CN	
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2004-7021170	968632		KR	
98961737.8	69828813	MULTI-DIMENSIONAL CACHE COHERENCE DIRECTORY STRUCTURE	DE	
2003-129793	4267364	METHOD FOR PROCESSING THREE-DIMENSIONAL IMAGE	JP	
517327/1997	3639848		JP	
2003-356594	3933620	MAINTENANCE METHOD FOR MULTIPROCESSOR COMPUTER SYSTEM	JP	
974651	974651		FR	
2068117	2068117		GB	
9706956.6	M9706956.6		DE	
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2067607	2067607		GB	
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992864	992864		FR	
2082932	2082932		GB	
98959468.4	69804131	ROUTER TABLE LOOKUP MECHANISM	DE	
98957995.8	69806798	VIRTUAL CHANNEL ASSIGNMENT IN LARGE TORUS SYSTEMS	DE	
09/642,957	6,345,515	Conditioning and filling system for a spray evaporative cooling working fluid	US	8/21/2000
09/620,336	6,441,666	System and method for generating clock signals	US	7/20/2000

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09/619,818	6,483,699	Baffle system for air cooled computer assembly	US	7/20/2000
09/620,683	6,496,048	System and method for accurate adjustment of discrete integrated circuit delay lines	US	7/20/2000
09/407,426	6,516,372	Partitioning a distributed shared memory multiprocessor computer to facilitate selective hardware maintenance	US	9/29/1999
09/619,959	6,518,812	Discrete delay line system and method	US	7/20/2000
09/620,372	6,643,764	Multiprocessor system utilizing multiple links to improve point to point bandwidth	US	7/20/2000
09/620,338	6,701,496	Synthesis with automated placement information feedback	US	7/20/2000
09/619,722	6,779,072	Method and apparatus for accessing MMR registers distributed across a large asic	US	7/20/2000
09/619,869	6,831,834	Assembly process and heat sink design for high powerd processor	US	7/20/2000
09/620,373	7,248,635	Method and apparatus for communicating computer data from one point to another over a communications medium	US	7/20/2000
09/619,851	6,604,185	Distribution of address-translation-purge requests to multiple processors	US	7/20/2000
09/650,101	6,751,705	Cache line converter	US	8/25/2000
09/620,333	6,831,924	Variable mode bi-directional and uni-directional computer communication system	US	7/20/2000
09/620,058	6,839,856	Method and circuit for reliable data capture in the presence of bus-master changeovers	US	7/20/2000
09/619,771	6,920,526	Dual-bank FIFO for synchronization of read data in DDR SDRAM	US	7/20/2000
09/621,315	7,333,516	Interface for synchronous data transfer between domains clocked at different frequencies	US	7/20/2000
15/474,162		SYSTEM AND METHOD FOR CONVEYING INFORMATION	US	3/30/2017
15/442,458		HIERARCHICAL SYSTEM MANAGER ROLLBACK	US	2/24/2017

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15/442,445		SYSTEM, METHOD AND COMPUTER PROGRAM PRODUCT FOR REMOTE GRAPHICS PROCESSING	US	2/24/2017
15/441,094		DEPLOYING SOFTWARE IN A MULTI-INSTANCE NODE	US	2/23/2017
15/439,771		ACTIVE ARCHIVE BRIDGE	US	2/22/2017
15/438,561		RAID SET INITIALIZATION	US	2/21/2017
15/428,004		MULTI-CLASS HETEROGENEOUS CLIENTS IN A FILESYSTEM	US	2/8/2017
15/408,092		SHARED MEMORY EIGENSOLVER	US	1/17/2017
15/353,413		METHOD AND SYSTEM FOR SHARED DIRECT ACCESS STORAGE	US	11/16/2016
PCT/US16/ 62316		METHOD AND SYSTEM FOR SHARED DIRECT ACCESS STORAGE	PCT	11/16/2016
PCT/US16/ 62253		UNIFIED POWER DEVICE MANAGEMENT AND ANALYZER	PCT	11/16/2016
PCT/US16/ 62098		NODE BLIND MATE LIQUID COOLING	PCT	11/15/2016
PCT/US16/ 62076		CONFIGURABLE NODE EXPANSION SPACE	PCT	11/15/2016
PCT/US16/ 61131		FLOATING LIQUID COOLED HEAT TRANSFER SOLUTION	PCT	11/9/2016
PCT/US16/ 60358		STORAGE ERROR TYPE DETERMINATION	PCT	11/3/2016
15/340,486		CLUSTERED FILESYSTEM WITH MEMBERSHIP VERSION SUPPORT	US	11/1/2016
15/339,704		FLOATING LIQUID COOLED HEAT TRANSFER SOLUTION	US	10/31/2016
15/339,483		NODE BLIND MATE LIQUID COOLING	US	10/31/2016
15/339,451		CONFIGURABLE NODE EXPANSION SPACE	US	10/31/2016
15/339,411		SYSTEM METHOD FOR I/O ACCELERATION IN HYBRID STORAGE WHEREIN COPIES OF DATA SEGMENTS ARE DELETED IF IDENTIFIED SEGMENTS DOES NOT MEET QUALITY LEVEL THRESHOLD	US	10/31/2016

Serial #	Patent/ Publication Number	Title	Country	Filed Date
15/339,186		PLATFORM AND SOFTWARE FRAMEWORK FOR DATA INTENSIVE APPLICATIONS IN THE CLOUD	US	10/31/2016
15/336,628		STORAGE ERROR TYPE DETERMINATION	US	10/27/2016
15/336,506		UNIFIED POWER DEVICE MANAGEMENT AND ANALYZER	US	10/27/2016
15/227,502		METHOD FOR TRANSPARENTLY CONNECTING AUGMENTED NETWORK SOCKET OPERATIONS	US	8/3/2016
15/226,045		SYSTEM AND METHOD FOR ORDERING OF DATA TRANSFERRED OVER MULTIPLE CHANNELS	US	8/2/2016
15/222,581		SERVER EMBEDDED STORAGE DEVICE	US	7/28/2016
15/221,936		DEPLOYING BIG DATA SOFTWARE IN A MULTI-INSTANCE NODE	US	7/28/2016
15/220,189		NETWORK TOPOLOGY FOR A SCALABLE MULTIPROCESSOR SYSTEM	US	7/26/2016
15/219,797		CLUSTERED FILESYSTEMS FOR MIX OF TRUSTED AND UNTRUSTED NODES	US	7/26/2016
15/219,030		DYNAMIC RESOURCE SCHEDULING	US	7/25/2016
15/216,358		LOGICAL BLOCK PROTECTION FOR TAPE INTERCHANGE	US	7/21/2016
15/215,009		SERVER WITH HEAT PIPE COOLING	US	7/20/2016