PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4979410

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
TIER LOGIC, INC.	07/24/2011

RECEIVING PARTY DATA

Name:	YAKIMISHU CO. LTD., L.L.C.
Street Address:	160 GREENTREE DRIVE
Internal Address:	SUITE 101
City:	DOVER
State/Country:	DELAWARE
Postal Code:	19904

PROPERTY NUMBERS Total: 3

Property Type	Number
Application Number:	15877224
Application Number:	15985590
Application Number:	15893537

CORRESPONDENCE DATA

Fax Number: (408)938-9069

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 408-938-9060
Email: jgarcia@mhbpatents.com
Correspondent Name: MURABITO HAO & BARNES LLP
Address Line 1: TWO NORTH MARKET STREET
Address Line 2: THIRD FLOOR
Address Line 4: SAN JOSE, CALIFORNIA 95113

ATTORNEY DOCKET NUMBER:	TIER PORTFOLIO
NAME OF SUBMITTER:	JOSE S. GARCIA
SIGNATURE:	/Jose S. Garcia/
DATE SIGNED:	05/25/2018

Total Attachments: 13
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Exhibit C

ASSIGNMENT OF RIGHTS IN CERTAIN ASSETS

For good and valuable consideration, the receipt of which is hereby acknowledged, Tier Logic, Inc., a Delaware corporation, with an address of P.O. Box 2760, Cupertino, CA 95015 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Yakimishu Co. Ltd., L.L.C., a Delaware limited liability company, having an address at 160 Greentree Drive, Suite 101, Dover, DE 19904 ("***Assignee***"), or its designees, the right, title, and interest in and to any and all of the following provisional patent applications, patent applications, patents, and other governmental grants or issuances of any kind (the "***Certain Assets***"):

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP08769461.8	EP	05/13/2008	Three dimensional programmable devices Raminda Madurawe
PCT/US2008/063483	WO	05/13/2008	Three dimensional programmable devices Raminda Madurawe
7,176,716	US	02/17/2006	Look-up table structure with embedded carry logic Raminda Udaya Madurawe
61/073,393	US	06/18/2008	Very high density logic Nij Dorairaj
7,176,713	US	01/05/2004	Integrated circuits with ram and rom fabrication options Raminda Udaya Madurawe
12/770,519	US	04/29/2010	Programmable logic devices comprising time multiplexed programmable interconnect Raminda Udaya Madurawe
12/234,677	US	09/21/2008	
60/419,208	US	10/18/2002	Programmable multi-purpose flip-flop Raminda Udaya Madurawe
60/397,070	US	07/22/2002	Wire replaceable thin film fuse and anti-fuse technology Raminda Udaya Madurawe

Exhibit C

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
10/267,483	US	10/08/2002	Three dimensional integrated circuits Raminda U Madurawe
10/267,484	US	10/08/2002	Methods for fabricating three dimensional integrated circuits Raminda U. Madurawe
10/413,808	US	04/14/2003	Insulated-gate field-effect thin film transistors Raminda U Madurawe
7,112,994	US	05/17/2004	Three dimensional integrated circuits Raminda Udaya Madurawe
11/042,362	US	01/26/2005	Semiconductor switching devices Raminda Udaya Madurawe
11/985,829	US	11/19/2007	Insulated-gate field-effect thin film transistors Raminda Udaya Madurawe
12/207,064	US	09/09/2008	Thin film transistors and fabrication methods Raminda Udaya Madurawe
60/393,763	US	07/08/2002	Wire replaceable tft sram cell and cell array technology Raminda Udaya Madurawe
11/494,001	US	07/28/2006	Configurable embedded multi-port memory Raminda Udaya Madurawe
11/986,022	US	11/19/2007	Three dimensional programmable devices Raminda Udaya Madurawe
61/318,636	US	03/29/2010	Integrated circuits comprising application specific & programmable logic functions

Exhibit C

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
60/419,759	US	10/20/2002	Programmable interconnect structures Raminda Udaya Madurawe
60/400,007	US	08/01/2002	Re-programmable asic Raminda U Madurawe
60/402,573	US	08/12/2002	Thin film sram cell Raminda Udaya Madurawe
60/449,011	US	02/24/2003	Sram cell and cell arrays Raminda Udaya Madurawe
12/567,088	US	09/25/2009	Low power programmable logic devices Raminda Udaya Madurawe

Assignor assigns to Assignee all rights to the inventions, invention disclosures, and discoveries in the assets listed above, together, with the rights, if any, to revive prosecution of claims under such assets and to sue or otherwise enforce any claims under such assets for past, present or future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to make available to Assignee all records regarding the Certain Assets.

The terms and conditions of this Assignment of Rights in Certain Assets will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

DATED this __ day of _____ 2011.

ASSIGNOR:

Tier Logic, Inc.

By: Douglas Laird
Name: Douglas Laird
Title: Authorized Individual

Exhibit B

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Tier Logic, Inc., a Delaware corporation, with an address of P.O. Box 2760, Cupertino, CA 95015 ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Yakimishu Co. Ltd., L.L.C., a Delaware limited liability company, having an address at 160 Greentree Drive, Suite 101, Dover, DE 19904 ("***Assignee***"), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the "***Patent Rights***"):

(a) the provisional patent applications, patent applications and patents listed in the table below (the "***Patents***");

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
TW097137797	TW	10/01/2008	Three dimensional programmable devices Raminda Udaya Madurawe
7,030,651	US	12/04/2003	Programmable structured arrays Raminda Udaya Madurawe
7,253,659	US	02/17/2006	Field programmable structured arrays Raminda Udaya Madurawe
7,323,905	US	04/13/2006	Programmable structured arrays Raminda Udaya Madurawe
12/018,243	US	01/23/2008	Programmable structured arrays Raminda Udaya Madurawe
7,019,557	US	12/24/2003	Look-up table based logic macro-cells Raminda Udaya Madurawe
7,208,976	US	02/10/2006	Look-up table based logic macro-cells Raminda Udaya Madurawe

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7,239,175	US	10/13/2006	Look-up table based logic macro-cells Raminda Udaya Madurawe
7,285,984	US	02/16/2007	Look-up table structure with embedded carry logic Raminda Udaya Madurawe
7,336,097	US	03/28/2007	Look-up table structure with embedded carry logic Raminda Udaya Madurawe
7,466,163	US	11/19/2007	Look-up table structure with embedded carry logic Raminda Udaya Madurawe
7,656,190	US	06/08/2009	Incrementer based on carry chain compression Nij Dorairaj
7,265,577	US	02/16/2007	Integrated circuits with ram and rom fabrication options Raminda Udaya Madurawe
7,486,111	US	03/08/2006	Programmable logic devices comprising time multiplexed programmable interconnect Raminda Udaya Madurawe
7,759,969	US	10/05/2008	Programmable logic devices comprising time multiplexed programmable interconnect Raminda Udaya Madurawe
7,489,164	US	11/19/2007	Multi-port memory devices Raminda Udaya Madurawe
7,635,988	US	07/14/2008	Multi-port thin-film memory devices Raminda Udaya Madurawe
12/834,697	US	07/12/2010	

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7,602,213	US	12/26/2007	Using programmable latch to implement logic Nij Dorairaj
7,795,913	US	01/16/2008	Programmable latch based multiplier Nij Dorairaj
7,573,293	US	05/12/2008	Programmable logic based latches and shift registers Raminda Madurawe
7,573,294	US	05/12/2008	Programmable logic based latches and shift registers Nij Dorairaj
7,042,756	US	10/14/2003	Configurable storage device Raminda Udaya Madurawe
7,298,641	US	03/02/2006	Configurable storage device Raminda Udaya Madurawe
12/836,530	US	01/01/1900	
6,747,478	US	10/08/2002	Field programmable gate array with convertibility to application specific integrated circuit Raminda U. Madurawe
6,855,988	US	04/14/2003	Semiconductor switching devices Raminda U. Madurawe
6,828,689	US	04/14/2003	Semiconductor latches and sram devices Raminda U. Madurawe
7,018,875	US	01/23/2004	Insulated-gate field-effect thin

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			film transistors Raminda U. Madurawe
6,856,030	US	01/26/2004	Semiconductor latches and sram devices Raminda Udaya Madurawe
6,992,503	US	04/16/2004	Programmable devices with convertibility to customizable devices Raminda Udaya Madurawe
6,849,958	US	05/05/2004	Semiconductor latches and sram devices Raminda Udaya Madurawe
7,064,018	US	05/17/2004	Methods for fabricating three dimensional integrated circuits Raminda Udaya Madurawe
6,998,722	US	05/24/2004	Semiconductor latches and sram devices Raminda Udaya Madurawe
7,205,589	US	06/08/2004	Semiconductor devices fabricated with different processing options Raminda Udaya Madurawe
7,064,579	US	06/22/2004	Alterable application specific integrated circuit (asic) Raminda Udaya Madurawe
7,030,446	US	08/06/2004	Semiconductor switching devices Raminda Udaya Madurawe
7,777,319	US	09/10/2004	Three dimensional integrated circuits Raminda Udaya Madurawe

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7,265,421	US	11/02/2004	Insulated-gate field-effect thin film transistors Raminda Udaya Madurawe
7,268,580	US	11/15/2004	Configuration circuits for three dimensional programmable logic devices Raminda Udaya Madurawe
7,312,109	US	04/11/2005	Methods for fabricating fuse programmable three dimensional integrated circuits Raminda Udaya Madurawe
7,285,981	US	02/21/2006	Configuration circuit for programmable logic devices Raminda Udaya Madurawe
11/363,304	US	02/27/2006	Three dimensional integrated circuits Raminda Udaya Madurawe
7,285,982	US	03/02/2006	Configuration circuits for programmable logic devices Raminda Udaya Madurawe
7,356,799	US	03/20/2006	Timing exact design conversions from fpga to asic Raminda Udaya Madurawe
7,345,505	US	04/10/2006	Alterable application specific integrated circuit (asic) Raminda Udaya Madurawe
7,627,848	US	12/26/2006	Bit stream compatible fpga to mpga conversions Raminda Udaya Madurawe
7,673,273	US	03/01/2007	Mpga products based on a prototype fpga

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			Thomas Henry White
7,759,705	US	05/11/2007	Semiconductor devices fabricated with different processing options Raminda Udaya Madurawe
7,362,133	US	05/11/2007	Three dimensional integrated circuits Raminda Udaya Madurawe
7,446,563	US	11/19/2007	Three dimensional integrated circuits Raminda Udaya Madurawe
7,463,059	US	03/10/2008	Alterable application specific integrated circuit (asic) Raminda Udaya Madurawe
12/104,377	US	04/16/2008	Timing exact design conversions from fpga to asic Raminda Udaya Madurawe
7,538,575	US	04/17/2008	Three dimensional integrated circuits Raminda Udaya Madurawe
7,709,314	US	09/09/2008	Semiconductor switching devices and fabrication methods Raminda Udaya Madurawe
7,656,192	US	10/20/2008	Three dimensional integrated circuits Raminda Udaya Madurawe
12/834,077	US	07/12/2010	Three dimensional integrated circuits Raminda U. Madurawe
7,129,744	US	10/23/2003	Programmable interconnect structures

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			Raminda U. Madurawe
7,084,666	US	01/24/2005	Programmavle interconnect structures Raminda U. Madurawe
7,239,174	US	10/10/2006	Programmable interconnect structures Raminda Udaya Madurawe
7,332,934	US	11/06/2006	Programmable interconnect structures Raminda Udaya Madurawe
7,679,399	US	02/16/2008	Programmable interconnect structures Raminda Udaya Madurawe
7,812,458	US	11/19/2007	Pad invariant fpga and asic devices Raminda Udaya Madurawe
11/986,023	US	11/19/2007	Pads and pin-outs in three dimensional integrated circuits Raminda Udaya Madurawe
12/210,212	US	09/14/2008	Automated metal pattern generation for integrated circuits Raminda Udaya Madurawe
12/254,670	US	10/20/2008	Low power programmable logic devices

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that incorporate by reference, or are incorporated by reference into, the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) inventions, invention disclosures, and discoveries described in any of the Patents and/or any item in the foregoing categories (b) through (e) that (i) are included in any claim in the Patents and/or any item in the foregoing categories (b) through (e), (ii) are subject matter capable of being reduced to a patent claim in a reissue or reexamination proceeding brought on any of the Patents and/or any item in the foregoing categories (b) through (e), and/or (iii) could have been included as a claim in any of the Patents and/or any item in the foregoing categories (b) through (e);

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

(1) damages,
(2) injunctive relief, and
(3) any other remedies of any kind

for past, current, and future infringement; and

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h).

Assignor represents, warrants and covenants that:

(1) Assignor has the full power and authority, and has obtained all third party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee; and

(2) Assignor owns, and by this document assigns to Assignee, all right, title, and interest to the Patent Rights, including, without limitation, all right, title, and interest to sue for infringement of the Patent Rights. Assignor has obtained and properly recorded previously executed assignments for the Patent Rights as necessary to fully perfect its rights and title therein in accordance with governing law and regulations in each respective jurisdiction. The Patent Rights are free and clear of all liens, claims, mortgages, security interests or other encumbrances, and restrictions. There are no actions, suits, investigations, claims or proceedings threatened, pending or in progress relating in any way to the Patent Rights. There are no existing contracts, agreements, options, commitments, proposals, bids, offers, or rights with, to, or in any person to acquire any of the Patent Rights.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

Assignor will, at the reasonable request of Assignee and without demanding any further consideration therefore, do all things necessary, proper, or advisable, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at _____ on July 24, 2011.

ASSIGNOR:

Tier Logic, Inc.

By: Douglas Laird
Name: Douglas Laird
Title: Authorized Individual
(Signature MUST be attested)

ATTESTATION OF SIGNATURE PURSUANT TO 28 U.S.C. § 1746

The undersigned witnessed the signature of Douglas Laird to the above Assignment of Patent Rights on behalf of Tier Logic, Inc. and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. Douglas Laird is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on July 24, 2011 to execute the above Assignment of Patent Rights on behalf of Tier Logic, Inc.

3. Douglas Laird subscribed to the above Assignment of Patent Rights on behalf of Tier Logic, Inc.

I declare under penalty of perjury under the laws of the United States of America that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

EXECUTED on July 24, 2011 (date)

Joan Laird

Print Name: Joan Laird