PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT4981270

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SUVOLTA, INC.	03/03/2015

RECEIVING PARTY DATA

Name:	MIE FUJITSU SEMICONDUCTOR LIMITED
Street Address:	2000 MIZONO, TADO-CHO
City:	KUWANA, MIE
State/Country:	JAPAN
Postal Code:	511-0118

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	15963598

CORRESPONDENCE DATA

Fax Number: (512)322-2501

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ATTORNEY DOCKET NUMBER:	083852.0387
NAME OF SUBMITTER:	JULI TRAN
SIGNATURE:	/Juli Tran/
DATE SIGNED:	05/29/2018

Total Attachments: 17
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EXHIBIT B

FORM OF PATENT ASSIGNMENT

PATENT ASSIGNMENT

This PATENT ASSIGNMENT ("**Assignment**") is made as of 2/27, 2015, to effectuate an assignment of certain patent assets from SuVolta, Inc., a Delaware corporation having a principal address at 130 D Knowles Drive, Los Gatos, CA 95032, USA ("**Assignor**") to MIE FUJITSU SEMICONDUCTOR LIMITED, a Japanese corporation having its principal place of business at 2000 Mizono, Tado-cho, Kuwana, Mie 511-0118, Japan ("**Assignee**").

WHEREAS, Assignor is the owner of the patents and patent applications (the "**Assigned Patents**") stated in Exhibit A attached to the Agreement.

WHEREAS, Assignor and Assignee have entered into an IPR PURCHASE AGREEMENT ("**Agreement**") dated 2/27/2015, pursuant to which Assignor has agreed, *inter alia*, to grant and assign all of Assignor's right, title and interest in and to the Assigned Patents to Assignee, and Assignee desires to acquire the entire right, title and interest in and to the Assigned Patents.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, Assignor and Assignee agree as follows.

1. Assignor hereby irrevocably sells, transfers, conveys and assigns unto Assignee, its successors and assigns, Assignor's entire right, title and interest in and to the Assigned Patents and any continuations, divisions, reissues, or extensions of the Assigned Patents.

2. Assignor hereby authorizes the United States Patent and Trademark Office and foreign patent and trademark offices to issue any patents from patent applications of the Assigned Patents, with the right, title and interest to be held by Assignee, Assignee's successors and assigns.

Agreed.

Assignor
SuVolta, Inc.

By: _____

Name: Naomi Obinata

Title: Legal Counsel, SuVolta

Date: 3/3/2015

Assignee
Mie Fujitsu Semiconductor Limited

By: _____

Name: Hayayoshi Yagi

Title: President and Representative Director

Date: 2/27/2015

CALIFORNIA ALL-PURPOSE ACKNOWLEDGMENT **CIVIL CODE § 1189**

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document.

State of California)
County of Santa Clara)

On 03/03/2015 (Date) before me, DAVID JOSEPH BOUSQUET, NOTARY PUBLIC, (Here Insert Name and Title of the Officer)

personally appeared Naomi Obinata, (Name(s) of Signer(s))

who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Signature _____ (Signature of Notary Public)

DAVID JOSEPH BOUSQUET
Commission # 1937711
Notary Public - California
Santa Clara County
My Comm. Expires May 22, 2015

Place Notary Seal Above

OPTIONAL

Though this section is optional, completing this information can deter alteration of the document or fraudulent reattachment of this form to an unintended document.

Description of Attached Document

Title or Type of Document: _____ Document Date: _____

Number of Pages: _____ Signer(s) Other Than Named Above: _____

Capacity(ies) Claimed by Signer(s)

Signer's Name: Naomi Obinata	Signer's Name: _____
☐ Corporate Officer — Title(s): _____	☐ Corporate Officer — Title(s): _____
☐ Partner — ☐ Limited ☐ General	☐ Partner — ☐ Limited ☐ General
☐ Individual ☐ Attorney In Fact	☐ Individual ☐ Attorney In Fact
☐ Trustee ☐ Guardian or Conservator	☐ Trustee ☐ Guardian or Conservator
☒ Other: Assignor	☐ Other: _____
Signer is Representing: _____	Signer is Representing: _____

EXHIBIT A
PATENT ASSETS

SuVolta patent assets – U.S.

SuVolta confidential							
#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.		Notes
1	10-001 US	Electronic Devices and Systems, and Methods for Making and Using the Same	Issued	02-18-2010 12/708,497	09-25-2012 8,273,617		3.5 yr. maintenance fee due 2016
2	10-001 CON1	Electronic Devices and Systems, and Methods for Making and Using the Same	Issued	07-19-2012 13/553,593	09-24-2013 8,541,824		3.5 yr. maintenance fee due 2017
3	10-001 CON2	Electronic Devices and Systems, and Methods for Making and Using the Same	Issued	09-14-2012 13/616,053	12-10-2013 8,604,527		3.5 yr. maintenance fee due 2017
4	10-001 CON3	Electronic Devices and Systems, and Methods for Making and Using the Same	Issued	09-14-2012 13/616,059	12-10-2013 8,604,530		3.5 yr. maintenance fee due 2017
5	10-001 CON31	Electronic Devices and Systems, and Methods for Making and Using the Same	Issued	11-15-2013 14/082,931	8,975,126		3.5 yr. maintenance fee due 2016
6	10-002 US	Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof	Issued	12-17-2010 12/971,884	09-10-2013 8,530,286		3.5 yr. maintenance fee due 2017
7	10-002 CON1	Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof	Filed	08-19-2013 13/969,938			
8	10-003 US	Transistor with Threshold Voltage Set Notch and Method of Fabrication Thereof	Issued	12-17-2010 12/971,955	06-24-2014 8,759,872		3.5 yr. maintenance fee due 2017
9	10-003 DIV1	Transistor with Threshold Voltage Set Notch and Method of Fabrication Thereof	Filed	06-05-2014 14/296,627			
10	10-004 DIV1	Process for Manufacturing an Improved Analog Transistor	Issued	07-20-2012 13/553,502	06-10-2014 8,748,270		3.5 yr. maintenance fee due 2017
11	10-004 DIV2	Analog Transistor	Filed	05-09-2014 14/273,938			Office action response to be filed by SuVolta 2/23/16
12	10-005 US	Semiconductor Structure and Method of Fabrication Thereof with Mixed Metal Types	Issued	12-03-2010 12/960,266	10-29-2013 8,569,128		3.5 yr. maintenance fee due 2017
13	10-005 CON1	Semiconductor Structure and Method of Fabrication Thereof with Mixed Metal Types	Filed	10-04-2013 14/046,234			Office action response due 5/4/16 (indication of allowable claims)
14	10-007 US	Semiconductor Structure with Improved Channel Stack and Method for Fabrication Thereof	Issued	03-03-2011 13/039,956	09-03-2013 8,525,271		3.5 yr. maintenance fee due 2017

#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.	Notes
15	10-007 CON1	Semiconductor Structure with Improved Channel Stack and Method for Fabrication Thereof	Filed	07-31-2013 13/955,787		
16	10-009 US	Source/Drain Extension Control for Advanced Transistors	Issued	12-03-2010 12/960,289	03-26-2013 8,404,551	3.5 yr. maintenance fee due 2016
17	10-009 CON1	Source/Drain Extension Control for Advanced Transistors	Issued	02-19-2013 13/770,313	10-22-2013 8,563,384	3.5 yr. maintenance fee due 2017
18	10-009 CON2	Source/Drain Extension Control for Advanced Transistors	Issued	09-18-2013 14/030,471	04-01-2014 8,686,511	3.5 yr. maintenance fee due 2017
19	10-009 CON3	Source/Drain Extension Control for Advanced Transistors	Allowed	02-24-2014 14/188,493		Issue fee to be paid by SuVolta on 3/2/15
20	DSM-0010 CON2	Circuit Configurations Having Four Terminal Devices	Issued	08-23-2010 12/861,659	07-26-2011 7,986,167	3.5 yr. maintenance fee paid 2015
21	10-011 US	Method for Minimizing Defects in a Semiconductor Substrate due to Ion Implantation	Issued	09-30-2010 12/895,657	02-19-2013 8,377,807	3.5 yr. maintenance fee due 2016
22	10-012 US	Method for Reducing Punch-Through in a Transistor Device	Issued	09-30-2010 12/895,695	02-19-2013 8,377,783	3.5 yr. maintenance fee due 2016
23	10-013 US	Method for Minimizing Defects in a Semiconductor Substrate due to Ion Implantation	Issued	09-30-2010 12/895,730	10-14-2014 8,858,818	3.5 yr. maintenance fee due 2018
24	10-014 US	Advanced Transistors with Punch Through Suppression	Issued	09-30-2010 12/895,813	04-16-2013 8,421,162	3.5 yr. maintenance fee due 2016
25	10-014 DIV1	Advanced Transistors with Punch Through Suppression	Filed	02-24-2014 14/188,218		
26	10-015 US	Advanced Transistors with Threshold Voltage Set Dopant Structures	Filed	09-30-2010 12/895,785		Office action response due 3/10/15 (SuVolta will respond)
27	11-021 US	Digital Circuits having Improved Transistors, and Methods Therefor	Issued	02-18-2011 13/030,939	06-11-2013 8,461,875	3.5 yr. maintenance fee due 2016
28	11-021 CON1	Digital Circuits having Improved Transistors, and Methods Therefor	Filed	06-10-2013 13/891,929		
29	11-024 US	Analog Circuits having Improved Transistors, and Methods Therefor	Issued	03-24-2011 13/071,399	03-19-2013 8,400,219	3.5 yr. maintenance fee due 2016

#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.	Notes
30	11-024 CON1	Analog Circuits having Improved Transistors, and Methods Therefor	Issued	02-19-2013 13/770,482	09-30-2014 8,847,684	3.5 yr. maintenance fee due 2018
31	11-024 CON2	Analog Circuits having Improved Transistors, and Methods Therefor	Filed	09-29-2014 14/500,236		
32	11-025 US	Circuit Devices and Methods Having Adjustable Transistor Body Bias	Allowed	06-23-2011 13/167,625		Notice of allowance received (SuVolta will pay issue fee)
33	11-028 US	Electronic Device with Controlled Threshold Voltage	Issued	07-26-2012 13/559,554	06-10-2014 8,748,985	3.5 yr. maintenance fee due 2017
34	11-028 CON1	Electronic Device with Controlled Threshold Voltage	Issued	06-30-2014 14/292,806	8,963,249	3.5 yr. maintenance fee due 2018
35	11-032 US	Porting a Circuit Design from a First Semiconductor Process to a Second Semiconductor Process	Issued	08-22-2012 13/592,122	02-04-2014 8,645,878	3.5 yr. maintenance fee due 2017
36	11-032 CON1	Porting a Circuit Design from a First Semiconductor Process to a Second Semiconductor Process	Issued	02-04-2014 14/171,224	08-12-2014 8,806,395	3.5 yr. maintenance fee due 2018
37	11-032 CON2	Porting a Circuit Design from a First Semiconductor Process to a Second Semiconductor Process	Filed	07-21-2014 14/336,793		
38	11-033 US	Tipless Transistors, Short-Tip Transistors, and Methods and Circuits Therefor	Issued	12-05-2012 13/706,983	11-25-14 8,895,327	3.5 yr. maintenance fee due 2018
	11-033 DIV1	Tipless Transistors, Short-Tip Transistors, and Methods and Circuits Therefor	Filed	11-05-2014 14/533,414		
39	11-034 US	Transistor with Reduced Scattered Dopants	Filed	05-11-2012 13/469,583		Office action response due 4/1/15 (SuVolta to respond early March)
40	11-035 US	Integrated Circuit Devices and Methods	Issued	05-14-2012 13/471,353	08-19-2014 8,811,068	3.5 yr. maintenance fee due 2018
41	11-035 CON1	Integrated Circuit Devices and Methods	Filed	08-09-2014 14/455,892		
42	11-036 US	Epitaxial Channel Transistors and Die with Diffusion Doped Channels	Filed	05-11-2012 13/469,201		
43	11-036 US1	Transistor having Reduced Junction Leakage and Methods of Forming Thereof	Issued	12-21-2012 13/725,152	11-11-14 8,883,600	3.5 yr. maintenance fee due 2018
44	11-036 DIV1	High Uniformity Screen and Epitaxial Layers for CMOS Devices	Filed	11-05-2014 14/534,595		

#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.	Notes
45	11-037 US	Analog Circuits having Improved Insulated Gate Transistors, and Methods Therefor	Filed	10-05-2012 13/646,506		RCE to be filed week of 2/23/15 (SuVolta will file)
46	11-038A US	Monitoring and Measurement of Thin Film Layers	Issued	05-11-2012 13/469,595	08-05-2014 8,796,048	3.5 yr. maintenance fee due 2018
47	11-038A CON1	Monitoring and Measurement of Thin Film Layers	Filed	06-11-2014 14/301,512		
48	11-039 US	Semiconductor Structure with Substitutional Boron and Method for Fabrication Thereof	Allowed	05-11-2012 13/469,249		Issue fee to be paid 3/2/2015 (SuVolta will pay)
49	11-040 US	Reducing or Eliminating Pre-Amorphization in Transistor Manufacture	Issued	05-16-2012 13/473,403	10-29-2013 8,569,156	3.5 yr. maintenance fee due 2017
50	11-040 CON1	Reducing or Eliminating Pre-Amorphization in Transistor Manufacture	Issued	10-04-2013 14/046,147	01-20-15 8,937,005	3.5 yr. maintenance fee due 2018
	11-040 CON2	Reducing or Eliminating Pre-Amorphization in Transistor Manufacture	Filed	01-20-2015		
51	11-041 US	CMOS Gate Stack Structures and Processes	Issued	06-06-2012 13/489,824	05-27-2014 8,735,987	3.5 yr. maintenance fee due 2017
52	11-041 CON1	CMOS Gate Stack Structures and Processes	Filed	04-30-2014 14/266,115		
53	11-042 US	Body Bias Circuits and Methods	Issued	11-02-2012 13/668,053	08-26-2014 8,816,754	3.5 yr. maintenance fee due 2018
54	11-042 DIV1	Body Bias Circuits and Methods	Filed	08-19-2014 14/463,399		
55	11-043 US	Semiconductor Devices having Fin Structures and Fabrication Methods Thereof	Allowed	02-05-2014 14/173,570		Issue fee due 5/5/15
56	11-044 US	Circuits and Methods for Measuring Circuit Elements in an Integrated Circuit Device	Issued	12-23-2011 13/336,434	12-03-2013 8,599,623	3.5 yr. maintenance fee due 2017
57	11-044 CON1	Circuits and Methods for Measuring Circuit Elements in an Integrated Circuit Device	Issued	11-05-2013 14/072,761	09-16-2014 8,837,230	3.5 yr. maintenance fee due 2017
58	11-044 CON2	Circuits and Methods for Measuring Circuit Elements in an Integrated Circuit Device	Filed	09-15-2014 14/487,053		

#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.	Notes
59	11-045 US	Deeply Depleted MOS Transistors having a Screening Layer and Methods Thereof	Filed	09-05-2013 14/019,187		
60	11-048 US	Multiple Transistor Types Formed in a Common Epitaxial Layer by Differential Out-Diffusion from a Doped Underlayer	Issued	04-30-2012 13/459,971	01-14-2014 8,629,016	3.5 yr. maintenance fee due 2017
61	11-048 CON1	Multiple Transistor Types Formed in a Common Epitaxial Layer by Differential Out-Diffusion from a Doped Underlayer	Issued	09-24-2013 13/624,449	02-18-2014 8,653,604	3.5 yr. maintenance fee due 2017
62	11-048 CON2	Multiple Transistor Types Formed in a Common Epitaxial Layer by Differential Out-Diffusion from a Doped Underlayer	Issued	02-14-2014 14/180,488	8,916,937	3.5 yr. maintenance fee due 2018
	11-048 CON3	Multiple Transistor Types Formed in a Common Epitaxial Layer by Differential Out-Diffusion from a Doped Underlayer	Filed	12-15-2014		
63	11-050 US	CMOS Structures and Processes Based on Selective Thinning	Issued	08-22-2012 13/591,767	12-24-2013 8,614,128	3.5 yr. maintenance fee due 2017
64	11-050 CON1	CMOS Structures and Processes Based on Selective Thinning	Filed	12-10-2013 14/101,691		Abandoned
	11-050 DIV	CMOS Structures and Processes Based on Selective Thinning	Filed	12-15-2014		
65	11-051 US	Tools and Methods for Yield-Aware Semiconductor Manufacturing Process Target Generation	Issued	09-17-2012 13/621,695	04-29-2014 8,713,511	3.5 yr. maintenance fee due 2017
66	11-051 CON1	Tools and Methods for Yield-Aware Semiconductor Manufacturing Process Target Generation	Filed	04-25-2014 14/263,849		
67	11-052 US	Integrated Circuits having a Plurality of High-K Metal Gate FETs with Various Combinations of Channel Foundation Structure and Gate Stack Structure and Methods of Making Same	Filed	01-31-2013 13/755,897		Waiting to hear from patent office
68	11-054 US	Uncoped Channel Transistor with Parameters Matched to a Doped Channel Transistor	Filed	05-03-2013 13/887,142		Waiting to hear from patent office
69	11-055 US	Integrated Circuits having a Plurality of Metal Gate FETS with Precisely Set Work Functions through Combinations of Channel Structure and Metal Gate Layering	Filed	11-15-2012 13/677,767		Office action response due 3/15/15 (SuVolta will respond)
70	11-056 US	Memory Circuits and Methods of Making and Designing the Same	Issued	12-14-2012 13/715,080	09-26-2014 8,819,603	3.5 yr. maintenance fee due 2018
71	11-056 CIP1	Memory Circuits and Methods of Making and Designing the Same	Filed	05-16-2014 14/280,318		

#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.		Notes
72	11-056 DIV1	Memory Circuits and Methods of Making and Designing the Same	Filed	08-18-2014 14/461,442			
73	12-057 US	Method for Substrate Preservation During Transistor Fabrication	Issued	05-29-2012 13/482,394	07-15-2014 8,776,786		3.5 yr. maintenance fee due 2018
74	12-058 US	Process For Manufacture of Integrated Circuits With Different Channel Doping Transistor Architectures and Devices Therefrom	Issued	01-23-2013 13/748,418	11-04-2014 8,877,619		3.5 yr. maintenance fee due 2018
75	12-059 US	Circuits and Devices for Generating Bi-Directional Body Bias Voltages, and Methods Therefor	Allowed	01-22-2013 13/747,256			Issue fee paid, expect issue notification approx. 3/1
76	12-060 US	Method for Fabricating Multiple Transistor Devices on a Substrate with Varying Threshold Voltages	Filed	02-28-2012 13/407,527			Office action response due 3/29/15 (SuVolta will respond)
77	12-062 US	Semiconductor Structure with Multiple Transistors having Various Threshold Voltages and Method of Fabrication Thereof	Filed	06-25-2013 13/926,555			Waiting to hear from patent office
78	12-063 US	Semiconductor Devices with Dopant Migration Suppression and Method of Fabrication Thereof	Filed	09-18-2012 13/622,194			Office action response due 3/24/15 (SuVolta will respond)
79	12-064A	SRAM Cell Layout Structure and Devices Therefrom	Issued	02-26-2013 13/776,912	10-14-2014 8,863,064		3.5 yr. maintenance fee due 2018
80	12-064A DIV1	SRAM Cell Layout Structure and Devices Therefrom	Filed	10-10-2014 14/511,487			
81	12-065 US	Semiconductor Structure with Reduced Junction Leakage and Method of Fabrication Thereof	Issued	08-31-2012 13/600,647	01-28-2014 8,637,956		3.5 yr. maintenance fee due 2017
82	12-065 CON1	Semiconductor Structure with Reduced Junction Leakage and Method of Fabrication Thereof	Filed	12-19-2013 14/133,743			Office action response due 3/12/15 (SuVolta will respond)
83	12-066 US	Integrated Circuit Device Methods and Models with Predicted Device Metric Variations	Filed	02-28-2013 13/780,006			
84	12-068 US	DRAM-Type Device with Low Variation Transistor Peripheral Circuits, and Related Methods	Filed	10-31-2013 14/068,756			Restriction requirement response due 3/27/15 (SuVolta will respond)
85	12-069 US	Integrated Circuit Process and Bias Monitors and Related Methods	Filed	12-20-2013 14/136,258			Office action response due 4/28/15 (SuVolta will respond)
86	12-070 US	Slew Based Process and Bias Monitors and Related Methods	Filed	11-15-2013 14/081,264			Office action response due for 4/30/15 (SuVolta will respond)
87	12-071 US	6T Interleaved Low Voltage 6-T SRAM and Related Methods	Allowed	12-12-2013 14/104,182			Issue fee due 5/4/15

#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.		Notes
88	12-072 US	Ring Oscillator with NMOS or PMOS Variation Insensitivity	Allowed	03-08-2013 13/792,006			Issue fee paid, waiting for issue notification
89	13-075 US	Method for Fabricating a Transistor Device with a Tuned Dopant Profile	Filed	03-14-2013 13/828,262			
90	13-076 US	Integrated Circuit Device Body Bias Circuits and Methods	Filed	03-15-2013 13/838,221			
91	13-077 US	Multiple VDD Clock Buffer	Allowed	03-01-2013 13/783,167			Issue fee paid, waiting for issue notification
92	13-078 US	Transistor Array Structure	Filed	03-15-2013 13/835,327			
93	13-080 US	Buried Channel Deeply Depleted Channel Transistor	Filed	05-23-2014 14/286,063			
94	13-081 US	Architecture and Fabrication Method for DDC Transistors	Filed	06-25-2014 14/315,232			
95	13-083 US	SRAM Performance Monitor	Issued	08-29-2013 14/014,076			3.5 yr. maintenance fee due 2018
96	13-084 US	Fabrication Method for Deeply Depleted Channel and Other Devices Using Selective Epitaxial Growth	Filed	05-20-2014 14/463,813			
97	13-086 PRO	Flash Device Fabrication Method for Deeply Depleted Channel and Other Devices	Filed	11-27-2013 61/909,910		*	Abandoned
98	13-087 PRO	Structure and Method for Reducing Junction Leakage in a Transistor Device	Filed	02-18-2014 61/941,093		*	Abandoned
99	13-089 PRO	Methods for Achieving Multiple Program and Erase States in Flash Memory using a Four-Terminal Transistor	Filed	12-12-2013 61/915,418		*	Abandoned
100	14-090 PRO	Buried Dielectric Barrier for Mitigated Source Drain Junction Leakage Transistors	Filed	03-31-2014 61/972,907		*	Utility conversion due 3/31/15
101	14-091 PRO	Structure and Method for Reducing Junction Leakage in a Transistor Device	Filed	02-11-2014 61/938,229		*	Abandoned
102	14-092 US	Power Up Body Bias Circuits and Methods	Filed	07-25-2014 14/341,733			
103	14-093 PRO	Three Dimensional Flash Memory Structures and Methods of Making the Same	Filed	02-12-2014 61/938,941		*	Abandoned
104	14-094 PRO	Structure and Method for Reducing Leakage in a Transistor Device	Filed	03-06-2014 61/948,784		*	Conversion to utility due 3/6/2015

#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.		Notes
105	14-095 US	Operational Amplifier Input Offset Correction with Transistor Threshold Voltage Adjustment	Filed	06-19-2014 14/463,568			
							* Provisional conversions have not been done. FSL Mie has option to file new patent applications.

#	DMI Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.		Notes
1	0001	Integrated Circuit using Complementary Junction Field Effect Transistor and MOS Transistor in Silicon and Silicon Alloys	Issued	10-28-2005 11/261,573	08-04-2009 7,569,873		
2	0001-DIV1	Integrated Circuit using Complementary Junction Field Effect Transistor and MOS Transistor in Silicon and Silicon Alloys	Issued	06-26-2009 12/492,329	03-29-2011 7,915,107		
3	0002	Method of Producing and Operating a Low Power Junction Field Effect Transistor	Issued	12-07-2006 11/635,004	01-06-2009 7,474,125		
4	0003	Semiconductor Device, Design Method and Structure	Issued	10-31-2006 11/590,265	04-28-2009 7,526,163		
5	0003-DIV1	Semiconductor Device, Design Method and Structure	Issued	02-26-2009 12/380,497	05-31-2011 7,954,920		
6	0003-DIV2	Semiconductor Device, Design Method and Structure	Issued	02-26-2009 12/380,490	06-28-2011 7,968,393		
7	0005	Self Aligned Gate JFET Structure and Method	Issued	06-09-2006 11/450,112	07-14-2009 7,560,755		
8	0005-DIV1	Self Aligned Gate JFET Structure and Method	Issued	09-22-2009 12/235,164	03-30-2010 7,687,335		
9	0006	Scalable Process and Structure for JFET for Small and Decreasing Line Widths	Issued	06-12-2006 11/451,886	01-05-2010 7,642,565		
10	0010	Circuit Configurations Having Four Terminal JFET Devices	Issued	06-13-2006 11/452,442	09-22-2009 7,592,643		
11	0010-CON1	Circuit Configurations Having Four Terminal JFET Devices	Issued	07-21-2009 12/506,848	03-23-2010 7,684,332		

DSM Patent assets – U.S. (see also rows 1-11 immediately above)

#	NuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.		Notes
12	0014	Semiconductor Device having a FIN Structure and Fabrication Method Thereof	Issued	05-02-2006 12/114,183	08-10-2010 7,772,619		
13	0019	Integrated Circuit using Complementary Junction Field Effect Transistor and MOS Transistor in Silicon and Silicon Alloys	Issued	11-03-2006 12/263,854	03-30-2010 7,687,834		
14	0022	JFET with Built-in Back Gate in either SOI or Bulk Silicon	Issued	06-19-2006 11/592,172	07-07-2009 7,557,393		
15	0022-DIV1	JFET with Built-in Back Gate in either SOI or Bulk Silicon	Issued	11-14-2008 12/270,564	01-12-2010 7,646,654		
16	0023	Oxide Isolated Metal Silicon-Gate JFET	Issued	07-11-2006 11/484,402	12-15-2009 7,633,101		
17	0023-DIV1	Method of Forming an Oxide Isolated Metal Silicon-Gate JFET	Issued	11-24-2008 12/276,574	05-11-2010 7,713,804		
18	0026	Level Shifting Circuit having Junction Field Effect Transistors	Issued	07-25-2006 11/495,908	01-12-2010 7,646,233		
19	0031	Junction Field Effect Transistor Input Buffer Level Shifting Circuit	Issued	09-01-2006 11/515,252	06-29-2010 7,746,145		
20	0032	Semiconductor Device including a Bias Voltage Generator	Issued	06-14-2007 11/818,395	03-16-2010 7,679,427		
21	0035	Circuit and Method for Generating Electrical Solitons with Junction Field Effect Transistors	Issued	09-21-2007 11/903,296	07-27-2010 7,764,137		
22	0041	Double Gate JFET with Reduced Area Consumption and Fabrication Method Therefor	Issued	04-30-2008 12/113,118	07-05-2011 7,973,344		
23	0043	Semiconductor Device Storage Cell Structure, Method of Operation and Method of Manufacture	Issued	05-01-2007 11/799,572	04-06-2010 7,692,220		
24	0044	Image Sensing Cell, Device, Method of Operation, and Method of Manufacture	Issued	05-01-2007 11/799,571	05-01-2010 7,727,821		
25	0049	Common Data Line Signaling and Method	Issued	07-02-2007 11/823,737	05-10-2011 7,941,096		
26	0051	Method and Apparatus for Improving SRAM Write Operations	Issued	12-19-2008 12/339,564	12-07-2010 7,848,139		
27	0057A	Method for Applying a Stress Layer to a Semiconductor Device and Device formed therefrom	Issued	05-04-2007 11/744,517	11-18-2008 7,453,107		
28	0057B	Semiconductor Device Having Strain-Inducing Substrate and Fabrication Methods Thereof	Issued	05-04-2007 11/744,660	05-12-2009 7,531,854		

#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.	Notes
29	0057B-DIV1	Semiconductor Device Having Strain-Inducing Substrate and Fabrication Methods Thereof	Issued	07-23-2008 12/178,291	10-20-2009 7,605,035	
30	0067	System and Method for Detecting Multiple Matches	Issued	03-29-2007 11/693,441	04-06-2010 7,694,059	
31	0069	Content Addressable Memory Cell Including a Junction Field Effect Transistor	Issued	05-01-2007 11/799,305	05-01-2010 7,729,149	
32	0070	Junction Field Effect Dynamic Random Access Memory Cell and Content Addressable Memory Cell	Issued	05-17-2007 11/804,132	12-15-2009 7,633,784	
33	0074	System and Method for Routing Connections	Issued	12-19-2007 11/960,452	03-30-2010 7,689,964	
34	0075	System and Method for Routing Connections with Improved Interconnect Thickness	Issued	06-06-2008 12/115,991	10-18-2011 8,042,076	
35	0078	JFET Device with Improved Off-State Leakage Current and Method of Fabrication	Issued	05-03-2007 11/744,080	04-28-2009 7,525,138	
36	0078-DIV1	JFET Device with Improved Off-State Leakage Current and Method of Fabrication	Issued	07-23-2008 12/178,404	05-04-2010 7,709,311	
37	0079	Current-Limited Output Buffer	Issued	07-15-2008 12/173,405	06-22-2010 7,741,882	
38	0082	Swapped-Body RAM Architecture	Issued	12-17-2007 11/958,032	06-22-2010 7,742,325	
39	0084	Transistor Providing Different Threshold Voltages and Method of Fabrication Thereof	Issued	05-03-2007 11/743,973	01-12-2010 7,645,662	
40	0084-DIV1	Transistor Providing Different Threshold Voltages and Method of Fabrication Thereof	Issued	02-02-2009 12/363,795	11-30-2010 7,843,018	
41	0085	JFET Device with Virtual Source and Drain Link Regions and Method of Fabrication	Issued	05-03-2007 11/744,120	04-28-2009 7,525,136	
42	0087	Switching Circuits and Methods for Programmable Logic Devices	Issued	08-03-2007 11/869,977	12-08-2009 7,629,812	
43	0094	Method to Fabricate Gate Electrodes	Issued	02-19-2008 12/033,487	01-12-2010 7,645,698	
44	0097	Programmable Switch Circuit and Method, Method of Manufacture, and Devices and Systems Including the Same	Issued	06-02-2008 12/155,865	05-04-2010 7,710,148	
45	0098	Method for Manufacturing a Junction Field Effect Transistor having a Double Gate	Issued	12-02-2008 12/326,415	09-13-2011 8,017,476	

#	SuVolta Docket No.	Title	Status	Filing Date Serial No.	Issued Date Patent No.	Notes
46	0098-CON	Junction Field Effect Transistor having a Double Gate Structure	Issued	08-26-2011 13/219,609	09-11-2012 8,264,017	
47	0100	Level-Shifting Circuit with Bipolar Junction Transistor	Issued	08-21-2008 12/195,725	03-30-2010 7,688,118	
48	0101	Voltage-Level Translator	Issued	07-11-2008 12/171,906	07-06-2010 7,750,735	
49	0105	Dynamic Random Access Memory having Junction Field Effect Transistor Cell Access Device	Issued	08-20-2008 12/194,651	10-11-2011 8,035,139	
50	0124	Memory Cell including an Emitter Follower and Emitter Follower Sensing Scheme and Method of Reading Data Therefrom	Issued	09-18-2008 12/284,037	11-30-2010 7,843,721	
51	0126	Junction Field Effect Transistor (JFET) Structure Having Top-To-Bottom Gate Tie and Method Of Manufacture	Issued	12-17-2008 12/316,944	05-17-2011 7,943,971	
52	0128	Semiconductor Device with Multiple Transistors Formed in a Partially Depleted Semiconductor-On-Insulator Substrate	Issued	02-06-2009 12/366,791	12-07-2010 7,847,354	
53	0132	Junction Field Effect Transistor using a Silicon on Insulator Architecture	Issued	07-25-2008 12/180,155	08-10-2010 7,772,620	
54	0139	Method for Providing Temperature Uniformity of Rapid Thermal Annealing	Issued	02-11-2009 12/369,169	09-06-2011 8,012,873	
55	0144	Method and Apparatus for Improving SRAM Write Operations	Issued	12-19-2008 12/339,618	06-28-2011 7,969,759	
56	0146	Advanced JFET with Reliable Channel Control and Method of Manufacture	Issued	01-07-2009 12/349,747	05-15-2010 7,736,962	

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#	SuVolta Docket No.	Title	Filing Date PCT Application No.	Status	Publication Date Publication No.	Notes
1	10-001 PCT1	Electronic Devices and Systems, and Methods for Making and Using the Same	09-15-2010 US2010/048998	National Stage	04-07-2011 WO 2011/041109	
2	10-001 PCT2	Electronic Devices and Systems, and Methods for Making and Using the Same	09-15-2010 US2010/049000	National Stage	04-07-2011 WO 2011/041110	
3	10-001 PCT4	Electronic Devices and Systems, and Methods for Making and Using the Same	11-09-2010 US2010/056702	National Stage	05-26-2011 WO 2011/062788	
4	10-001 PCT5	Electronic Devices and Systems, and Methods for Making and Using the Same	02-17-2011 US2011/025278	National Stage	08-25-2011 WO 2011/103314	
5	10-001 PCT6	Electronic Devices and Systems, and Methods for Making and Using the Same	02-17-2011 US2011/025284	National Stage	08-25-2011 WO 2011/103318	
6	10-002 PCT	Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof	04-07-2011 US2011/031531	National Stage	10-20-2011 WO 2011/130088	
7	10-003 PCT	Transistor with Threshold Voltage Set Notch and Method of Fabrication Thereof	06-21-2011 US2011/041167	National Stage	12-29-2011 WO 2011/163171	
8	10-007 PCT	Semiconductor Structure with Improved Channel Stack and Method for Fabrication Thereof	02-29-2012 US2012/027053	National Stage	09-07-2012 WO 2012/119873	
9	10-008 PCT	Source/Drain Extension Control for Advanced Transistors	11-30-2011 US2011/062495	National Stage	10-26-2012 WO 2012/145026	
10	10-014 PCT	Advanced Transistors with Punch Through Suppression	06-21-2011 US2011/041165	National Stage	12-29-2011 WO 2011/163169	
11	10-016 PCT	Advanced Transistors with Threshold Voltage Set Dopant Structures	06-21-2011 US2011/041166	National Stage	12-29-2011 WO 2011/163164	
12	10-018 PCT	Advanced Transistors with Structured Low Dopant Channels	11-05-2010 US2010/055560	National Stage	05-12-2012 WO 2012/060839	
13	11-043 PCT	Semiconductor Devices having Fin Structures and Fabrication Methods Thereof	08-03-2012 US2012/049531	National Stage	02-14-2013 WO 2013/022753	
14	11-045 PCT	Deeply Depleted MOS Transistors having a Screening Layer and Methods Thereof	08-17-2013 US2013/055045	Filed		National phase filing due 3/21/15 -- CN, KR
15	12-002 PCT	Semiconductor Structure with Multiple Transistors having Various Threshold Voltages and Method of Fabrication Thereof	08-26-2013 US2013/047767	Filed		Did not file National
16	12-008 PCT	DRAM-Type Device with Low Variation Transistor Peripheral Circuits, and Related Methods	10-31-2013 US2013/067832	Filed		National phase filing due 4/30/2015

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#	DSM Docket No.	Title	Filing Date PCT Application No.	Status	Publication Date Publication No.	Notes
1	0001 PCT	Integrated Circuit using Complementary Junction Field Effect Transistor and MOS Transistor in Silicon and Silicon Alloys	10-30-2006 US2006/042139	National Stage	05-10-2007 WO 2007/053485	
2	0002 PCT	Method of Producing and Operating a Low Power Junction Field Effect Transistor	12-07-2006 US2006/046666	National Stage	06-14-2007 WO 2007/067684	
3	0005 PCT	Self Aligned Gate JFET Structure and Method	06-07-2007 US2007/070589	National Stage	12-21-2007 WO 2007/146734	
4	0006 PCT	Scalable Process and Structure for JFET for Small and Decreasing Line Widths	06-11-2007 US2007/070804	National Stage	12-21-2007 WO 2007/146872	
5	0010 PCT	Circuit Configurations Having Four Terminal JFET Devices	06-13-2007 US2007/071075	National Stage	12-21-2007 WO 2007/146979	
6	0021 PCT	Silicon-on-Insulator (SOI) Junction Field Effect Transistor and Method of Manufacture	08-15-2007 US2007/075953	National Stage	02-28-2008 WO 2008/024655	
7	0022 PCT	JFET with Built-in Back Gate in either SOI or Bulk Silicon	08-09-2007 US2007/075535	National Stage	02-21-2008 WO 2008/021919	
8	0029 PCT	Semiconductor Device with Circuits Formed with Essentially Uniform Pattern Density	09-12-2007 US2007/078218	National Stage	04-10-2008 WO 2008/042560	
9	0033 PCT	Method and System for Adaptive Power Management	05-02-2008 US2008/062338	National Stage	11-13-2008 WO 2008/137625	

SuVolta, DSM patent assets -- China

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#	SuVolta Docket No.	Filing Date CN Application No.	Status	Issued Date Patent No.	Notes
1	10-001 CN1	09-15-2010 201080054379.4	Filed		
2	10-001 CN2	09-15-2010 201080054378.X	Filed		office action response due 3/10/15 (SuVolta will respond)
3	10-001 CN4	11-08-2010 201080061745.9	Filed		
4	10-001 CN5	02-17-2011 201180019743.8	Filed		Office action response due 4/8/15 (SuVolta will respond)
5	10-001 CN6	02-17-2011 201180019710.3	Filed		Office action response due 4/12/15 (SuVolta will respond)
6	10-003 CN	06-21-2011 201180040485.1	Filed		
7	10-007 CN	02-29-2012 201280017397.4	Filed		
8	10-009 CN	11-30-2011 201180058243.5	Filed		
9	10-014 CN	06-21-2011 201180035830.2	Filed		
10	10-016 CN	06-21-2011 201180035832.1	Filed		
#	DSM Docket No.	Filing Date CN Application No.	Status	Issued Date Patent No.	Notes
1	0001 CN	10-30-2006 200680039832.8	Issued	11-9-2011 ZL 200680039832.8	

SuVolta patent assets -- EP

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#	SuVolta Docket No	Filing Date EP Application No.	Status	Publication Date Publication No.	Notes
1	10-001 EP1	09-15-2010 10821021.2	Filed	08-08-2012 EP2483916	Waiting for search report
2	10-001 EP2	09-15-2010 10821022.0	Filed	08-08-2012 EP2483915	Waiting for search report

DSM patent assets -- India

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#	DSM Docket No.	Filing Date IN Application No.	Status
1	0001 IN	10-30-2006 4201/DELNP/2008	Filed

SuVolta and DSM patent assets -- Japan

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#	SuVolta Docket No.	Filing Date JP Application No.	Status	Issued Date Patent No.	Notes
1	10-001 JP1	09-15-2010 2012-532104	Filed		
2	10-001 JP2	09-15-2010 2012-532105	Filed		
3	10-001 JP4	11-8-2010 2012-539939	Filed		
4	10-001 JP5	02-17-2011 2012-554028	Filed		
5	10-001 JP6	02-17-2011 2012-554029	Filed		
6	10-003 JP	06-21-2011 2013-516664	Filed		
7	10-014 JP	06-21-2011 2013-516663	Filed		
#	DSM Docket No.	Filing Date JP Application No.	Status	Issued Date Patent No.	Notes
1	0010 JP	06-13-2007 2009-515621	Issued	10-05-2012 5,101,610	

SuVolta patent assets -- Korea

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#	SuVolta Docket No	Filing Date KR Application No.	Status	Issued Date Patent No.	Notes
1	10-001 KR1	09-15-2010 10-2012-7011021	Filed		Request for exam due 9/15/15
2	10-001 KR2	09-15-2010 10-2012-7011008	Filed		Request for exam due 9/15/15
3	10-001 KR4	11-08-2010 10-2012-7015629	Filed		Request for exam due 11/8/15
4	10-001 KR5	02-17-2011 10-2012-7024299	Filed		Request for exam due 02/17/16
5	10-001 KR6	02-17-2011 10-2012-7024293	Filed		Request for exam due 2/17/16
6	10-002 KR	04-07-2011 10-2012-7029435	Filed		
7	10-003 KR	06-21-2011 10-2013-7001612	Filed		Request for exam due 6/21/16
8	10-014 KR	06-21-2011 10-2013-7001668	Filed		Request for exam due 6/21/16
9	10-016 KR	06-21-2011 10-2013-7001667	Filed		Request for exam due 6/21/16
10	10-018 KR	11-05-2010 10-2011-7023427	Issued	08-22-2012 10-1178016	
11	11-043 KR	02-28-2014 10-2014-7005446	Filed		Request for exam due 8/4/17

SuVolta and DSM patent assets -- Taiwan

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#	SuVolta Docket No.	Filing Date TW Application No.	Status	Issued Date Patent No.	Notes
1	10-001 TW	09-29-2010 099132985	Filed		
2	10-002 TW	04-11-2011 100112429	Filed		
3	10-003 TW	06-21-2011 100121618	Filed		
4	10-009 TW	12-02-2011 100144358	Filed		Did not seek examination
5	10-014 TW	06-21-2011 100121611	Filed		
6	10-016 TW	06-21-2011 100121612	Filed		
7	11-043 TW	08-06-2012 101128322	Filed		Request for exam due 8/6/15
#	DSM Docket No.	Filing Date TW Application No.	Status	Issued Date Patent No.	Notes
1	0001 TW	10-27-2006 95139730	Issued	11-21-2010 I333695	
2	0082 TW	11-21-2008 97145237	Filed		