# PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5038984

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|---|---|
| **SUBMISSION TYPE:** | NEW ASSIGNMENT |
| **NATURE OF CONVEYANCE:** | ASSIGNMENT |

**CONVEYING PARTY DATA**

| Name | Execution Date |
|---|---|
| ADVANCED MICRO DEVICES, INC. | 06/26/2018 |

**RECEIVING PARTY DATA**

| | |
|---|---|
| **Name:** | INNOVATIVE FOUNDRY TECHNOLOGIES LLC |
| **Street Address:** | 40 PLEASANT STREET |
| **Internal Address:** | SUITE 208 |
| **City:** | PORTSMOUTH |
| **State/Country:** | NEW HAMPSHIRE |
| **Postal Code:** | 03801 |

**PROPERTY NUMBERS Total: 62**

| Property Type | Number |
|---|---|
| **Patent Number:** | 6455938 |
| **Patent Number:** | 6514860 |
| **Patent Number:** | 6515861 |
| **Patent Number:** | 6580122 |
| **Patent Number:** | 6583012 |
| **Patent Number:** | 6586842 |
| **Patent Number:** | 6646326 |
| **Patent Number:** | 6657267 |
| **Patent Number:** | 6657303 |
| **Patent Number:** | 6657304 |
| **Patent Number:** | 6661102 |
| **Patent Number:** | 6689684 |
| **Patent Number:** | 6709954 |
| **Patent Number:** | 6734559 |
| **Patent Number:** | 6762463 |
| **Patent Number:** | 6768204 |
| **Patent Number:** | 6797572 |
| **Patent Number:** | 6803631 |
| **Patent Number:** | 6806126 |

| Property Type | Number |
|---|---|
| **Patent Number:** | 6841473 |
| **Patent Number:** | 6855582 |
| **Patent Number:** | 6872647 |
| **Patent Number:** | 6881641 |
| **Patent Number:** | 6881665 |
| **Patent Number:** | 6897527 |
| **Patent Number:** | 6933620 |
| **Patent Number:** | 6939793 |
| **Patent Number:** | 6989604 |
| **Patent Number:** | 6991990 |
| **Patent Number:** | 7005357 |
| **Patent Number:** | 7009226 |
| **Patent Number:** | 7033940 |
| **Patent Number:** | 7049666 |
| **Patent Number:** | 7081655 |
| **Patent Number:** | 7157795 |
| **Patent Number:** | 7208383 |
| **Patent Number:** | 7276755 |
| **Patent Number:** | 7297994 |
| **Patent Number:** | 7306998 |
| **Patent Number:** | 7315054 |
| **Patent Number:** | 7354838 |
| **Patent Number:** | 7381622 |
| **Patent Number:** | 7396718 |
| **Patent Number:** | 7416973 |
| **Patent Number:** | 7442601 |
| **Patent Number:** | 7534689 |
| **Patent Number:** | 7704840 |
| **Patent Number:** | 7745264 |
| **Patent Number:** | 7755194 |
| **Patent Number:** | 7767540 |
| **Patent Number:** | 7880236 |
| **Patent Number:** | 7893496 |
| **Patent Number:** | 7985687 |
| **Patent Number:** | 7994014 |
| **Patent Number:** | 7994020 |
| **Patent Number:** | 8039878 |
| **Patent Number:** | 8283718 |

| Property Type | Number |
|---|---|
| **Patent Number:** | 8368221 |
| **Patent Number:** | 8390127 |
| **Patent Number:** | 8431466 |
| **Patent Number:** | 8815727 |
| **Patent Number:** | 9373548 |

**CORRESPONDENCE DATA**

**Fax Number:**

***Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.***

**Email:** CXU@MINTZ.COM
**Correspondent Name:** CATHERINE XU
**Address Line 1:** ONE FINANCIAL CENTER
**Address Line 2:** MINTZ LEVIN
**Address Line 4:** BOSTON, MASSACHUSETTS 02111

| | |
|---|---|
| **ATTORNEY DOCKET NUMBER:** | 052416-001 |
| **NAME OF SUBMITTER:** | ROBERT SWEENEY |
| **SIGNATURE:** | /ROBERT SWEENEY/ |
| **DATE SIGNED:** | 07/06/2018 |

**Total Attachments: 19**
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**Advanced Micro Devices, Inc. a corporation** with an office at 2485 Augustine Dr, Santa Clara, CA 95054 ("Assignor"), is the sole owner of the patents and patent applications listed in Schedule 1 hereto (collectively the "Listed Patents"); and

Innovative Foundry Technologies LLC, a Delaware corporation, with an office at 40 Pleasant Street, Suite 208, Portsmouth, NH 03801 ("Assignee") desires to acquire all right, title and interest in the Listed Patents and the other patents and related rights described below.

For good and valuable consideration, the receipt of which is hereby acknowledged, Assignor does hereby sell, assign, transfer and convey to Assignee and its successors and assigns all right, title and interest that may exist today and in the future to any and all:

(1) Listed Patents;

(2) foreign counterparts to any of the items covered by (1) above, including utility models, inventors' certificates, industrial design protection and any other form of governmental grants or issuances for the protection of inventions, designs or discoveries;

(3) inventions, invention disclosures, designs and discoveries described, disclosed or claimed in the items covered by (1) through (2) above;

(4) patents that issue from any of the items covered by (1) through (3) above;

(5) claims, causes of action and enforcement rights of any kind, whether currently pending, filed or otherwise, and whether known or unknown, under or arising from any of the items covered by (1) through (4) above, including all rights to pursue and collect damages, costs, injunctive relief and other remedies for past, current or future infringement thereof and including rights afforded under 35 U.S.C. § 154(d);

(6) royalties, income and other payments due as of the date hereof or hereafter under or arising from any of the items covered by (1) through (5) above; and

(7) rights to apply for, file, register, maintain, extend and renew in any or all countries of the world patents, certificates of invention, utility models, industrial design protection, design patent protection and other governmental grants or issuances of any kind related to any of the items covered by (1) through (6) above.

Assignor shall execute and deliver any instruments, and do and perform any other acts and things as may be reasonably necessary or desirable for effecting and evidencing the assignments contemplated hereby, including the execution, acknowledgment and recordation of any instruments.

Assignor hereby authorizes and requests the Commissioner of Listed Patents and Trademarks and any other patent office to issue any and all patents, utility models or other

governmental grants or issuances pertaining to any of the items assigned hereunder in the name of Assignee.

The assignment of right pursuant hereto will inure to the benefit of Assignee and its successors, assigns and other legal representatives and is binding upon Assignor and its successors, assigns, heirs and legal representatives.

Assignor, by its duly authorized representative, has executed this assignment on the date set forth below.

DATE: June 26, 2018

**Advanced Micro Devices, Inc.**

By: Kevin O'Neil
Printed/Typed Name

Title: VP - IP & Licensing

Signature

DATE: June ___, 2018

Innovative Foundry Technologies LLC,

By: _____
Printed/Typed Name

Title: _____

_____
Signature

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Province
STATE OF Ontario )
Town ) ss.
~~COUNTY~~ OF Markham )

On this 26 day of June, 2018, personally appeared before me Lou Onne, to me known and known to me to be the person aforesaid, who duly acknowledged the signing of the foregoing instrument to be his or her voluntary act and deed, and as Vice President of Advanced Micro Devices, Inc. did execute the same for the uses and purposes therein set forth.

WITNESS my hand and official seal.
(Seal)

Notary Public in and for the ~~state~~ Province of Ontario

LINDA LAM

Print Name

My appointment ~~expires on~~: Does not expire

ACCEPTED:

DATE: June ____, 2018

Advanced Micro Devices, Inc.

By: _____
Printed/Typed Name

Title: _____

_____
Signature

**SCHEDULE 1**

**To**

**Patent Assignment**

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| US | 6455938B1 | INTEGRATED CIRCUIT INTERCONNECT SHUNT LAYER | 1/18/2002 | 12/9/2003 |
| US | 6514860B1 | INTEGRATION OF ORGANIC FILL FOR DUAL DAMASCENE PROCESS | 6/12/2003 | 2/15/2005 |
| US | 6515861B1 | METHOD AND APPARATUS FOR SHIELDING ELECTROMAGNETIC EMISSIONS FROM AN INTEGRATED CIRCUIT | 5/2/2005 | 10/2/2007 |
| US | 6580122B1 | TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME | 7/5/2005 | 1/1/2008 |
| US | 6583012B1 | SEMICONDUCTOR DEVICES UTILIZING DIFFERENTLY COMPOSED METAL-BASED IN-LAID GATE ELECTRODES | 3/20/2001 | 6/17/2003 |
| US | 6586842B1 | DUAL DAMASCENE INTEGRATION SCHEME FOR PREVENTING COPPER CONTAMINATION OF DIELECTRIC LAYER | 2/13/2001 | 6/24/2003 |

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| US | 6646326B1 | METHOD AND SYSTEM FOR PROVIDING SOURCE/DRAIN-GATE SPATIAL OVERLAP ENGINEERING FOR LOW-POWER DEVICES | 7/28/2008 | 2/1/2011 |
| US | 6657267B1 | SEMICONDUCTOR DEVICE AND FABRICATION TECHNIQUE USING A HIGH-K LINER FOR SPACER ETCH STOP | 6/28/2001 | 2/4/2003 |
| US | 6657303B1 | INTEGRATED CIRCUIT WITH LOW SOLUBILITY METAL-CONDUCTOR INTERCONNECT CAP | 4/2/2001 | 2/4/2003 |
| US | 6657304B1 | CONFORMAL BARRIER LINER IN AN INTEGRATED CIRCUIT INTERCONNECT | 12/12/2001 | 12/2/2003 |
| US | 6661102B1 | SEMICONDUCTOR PACKAGING APPARATUS FOR CONTROLLING DIE ATTACH FILLET HEIGHT TO REDUCE DIE SHEAR STRESS | 6/9/2001 | 7/13/2004 |
| US | 6689684B1 | CU DAMASCENE INTERCONNECTIONS USING BARRIER/CAPPING LAYER | 9/6/2002 | 10/19/2004 |
| US | 6709954B1 | SCRIBE SEAL STRUCTURE AND METHOD OF MANUFACTURE | 8/9/2004 | 8/23/2005 |
| US | 6734559B1 | SELF-ALIGNED SEMICONDUCTOR INTERCONNECT BARRIER AND MANUFACTURING METHOD THEREFOR | 6/10/2005 | 7/8/2008 |



PATENT
REEL: 047014 FRAME: 0784

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| US | 6762463B2 | MOSFET WITH SIGE SOURCE/DRAIN REGIONS AND EPITAXIAL GATE DIELECTRIC | 7/12/2004 | 3/7/2006 |
| US | 6768204B1 | SELF-ALIGNED CONDUCTIVE PLUGS IN A SEMICONDUCTOR DEVICE | 7/27/2004 | 1/31/2006 |
| US | 6797572B1 | METHOD FOR FORMING A FIELD EFFECT TRANSISTOR HAVING A HIGH-K GATE DIELECTRIC AND RELATED STRUCTURE | 12/3/2003 | 7/25/2006 |
| US | 6803631B2 | STRAINED CHANNEL FINFET | 9/15/2000 | 5/11/2004 |
| US | 6806126B1 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT | 7/11/2003 | 9/28/2004 |
| US | 6841473B1 | MANUFACTURING AN INTEGRATED CIRCUIT WITH LOW SOLUBILITY METAL-CONDUCTOR INTERCONNECT CAP | 9/26/2003 | 1/11/2005 |
| US | 6855582B1 | FINFET GATE FORMATION USING REVERSE TRIM AND OXIDE POLISH | 3/30/2004 | 4/25/2006 |
| US | 6872647B1 | METHOD FOR FORMING MULTIPLE FINS IN A SEMICONDUCTOR DEVICE | 10/30/2002 | 4/24/2007 |
| US | 6881641B2 | SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION AND METHOD FOR FABRICATING THE SAME | 6/7/2006 | 12/11/2007 |



PATENT
REEL: 047014 FRAME: 0785

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| US | 6881665B1 | DEPTH OF FOCUS (DOF) FOR TRENCH-FIRST-VIA-LAST (TFVL) DAMASCENE PROCESSING WITH HARD MASK AND LOW VISCOSITY PHOTORESIST | 10/3/2006 | 8/26/2008 |
| US | 6897527B2 | STRAINED CHANNEL FINFET | 9/18/2006 | 10/28/2008 |
| US | 6933620B2 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE | 3/16/2006 | 7/13/2010 |
| US | 6939793B1 | DUAL DAMASCENE INTEGRATION SCHEME FOR PREVENTING COPPER CONTAMINATION OF DIELECTRIC LAYER | 12/6/2006 | 8/3/2010 |
| US | 6989604B1 | CONFORMAL BARRIER LINER IN AN INTEGRATED CIRCUIT INTERCONNECT | 10/10/2008 | 8/9/2011 |
| US | 6991990B1 | METHOD FOR FORMING A FIELD EFFECT TRANSISTOR HAVING A HIGH-K GATE DIELECTRIC | 7/21/2008 | 8/9/2011 |
| US | 7005357B2 | LOW STRESS SIDEWALL SPACER IN INTEGRATED CIRCUIT TECHNOLOGY | 6/23/2010 | 10/18/2011 |
| US | 7009226B1 | IN-SITU NITRIDE/OXYNITRIDE PROCESSING WITH REDUCED DEPOSITION SURFACE PATTERN SENSITIVITY | 7/5/2011 | 4/30/2013 |



PATENT
REEL: 047014 FRAME: 0786

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| US | 7033940B1 | METHOD OF FORMING COMPOSITE BARRIER LAYERS WITH CONTROLLED COPPER INTERFACE SURFACE ROUGHNESS | 8/27/2008 | 6/21/2016 |
| US | 7049666B1 | LOW POWER PRE-SILICIDE PROCESS IN INTEGRATED CIRCUIT TECHNOLOGY | 4/28/2004 | 5/24/2005 |
| US | 7081655B2 | FORMATION OF ABRUPT JUNCTIONS IN DEVICES BY USING SILICIDE GROWTH DOPANT SNOWPLOW EFFECT | 12/22/2009 | 2/22/2011 |
| US | 7157795B1 | COMPOSITE TANTALUM NITRIDE/TANTALUM COPPER CAPPING LAYER | 7/13/2001 | 9/24/2002 |
| US | 7208383B1 | METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT | 2/28/2001 | 7/1/2003 |
| US | 7276755B2 | INTEGRATED CIRCUIT AND METHOD OF MANUFACTURE | 11/15/2000 | 11/11/2003 |
| US | 7297994B2 | SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION | 6/6/2002 | 12/2/2003 |
| US | 7306998B2 | FORMATION OF ABRUPT JUNCTIONS IN DEVICES BY USING SILICIDE GROWTH DOPANT SNOWPLOW EFFECT | 6/6/2002 | 12/2/2003 |



PATENT
REEL: 047014 FRAME: 0787

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| US | 7315054B1 | DECOUPLING CAPACITOR DENSITY WHILE MAINTAINING CONTROL OVER ACLV REGIONS ON A SEMICONDUCTOR INTEGRATED CIRCUIT | 2/15/2001 | 2/10/2004 |
| US | 7354838B2 | TECHNIQUE FOR FORMING A CONTACT INSULATION LAYER WITH ENHANCED STRESS TRANSFER EFFICIENCY | 6/21/2002 | 3/23/2004 |
| US | 7381622B2 | METHOD FOR FORMING EMBEDDED STRAINED DRAIN/SOURCE REGIONS BASED ON A COMBINED SPACER AND CAVITY ETCH PROCESS | 4/5/2001 | 7/27/2004 |
| US | 7396718B2 | TECHNIQUE FOR CREATING DIFFERENT MECHANICAL STRAIN IN DIFFERENT CHANNEL REGIONS BY FORMING AN ETCH STOP LAYER STACK HAVING DIFFERENTLY MODIFIED INTRINSIC STRESS | 5/6/2003 | 3/29/2005 |
| US | 7416973B2 | METHOD OF INCREASING THE ETCH SELECTIVITY IN A CONTACT STRUCTURE OF SEMICONDUCTOR DEVICES | 8/9/2000 | 4/19/2005 |
| US | 7442601B2 | STRESS ENHANCED CMOS CIRCUITS AND METHODS FOR THEIR FABRICATION | 4/25/2003 | 9/6/2005 |
| US | 7534689B2 | STRESS ENHANCED MOS TRANSISTOR AND METHODS FOR ITS FABRICATION | 9/26/2003 | 1/24/2006 |



PATENT
REEL: 047014 FRAME: 0788

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| US | 7704840B2 | STRESS ENHANCED TRANSISTOR AND METHODS FOR ITS FABRICATION | 1/12/2004 | 2/28/2006 |
| US | 7745264B2 | SEMICONDUCTOR CHIP WITH STRATIFIED UNDERFILL | 6/1/2004 | 5/23/2006 |
| US | 7755194B1 | COMPOSITE BARRIER LAYERS WITH CONTROLLED COPPER INTERFACE SURFACE ROUGHNESS | 9/7/2004 | 1/2/2007 |
| US | 7767540B2 | TRANSISTOR HAVING A CHANNEL WITH TENSILE STRAIN AND ORIENTED ALONG A CRYSTALLOGRAPHIC ORIENTATION WITH INCREASED CHARGE CARRIER MOBILITY | 3/4/2005 | 11/20/2007 |
| US | 7880236B2 | SEMICONDUCTOR CIRCUIT INCLUDING A LONG CHANNEL DEVICE AND A SHORT CHANNEL DEVICE | 11/29/2005 | 4/8/2008 |
| US | 7893496B2 | STRESS ENHANCED TRANSISTOR | 11/14/2006 | 6/3/2008 |
| US | 7985687 | SYSTEM AND METHOD FOR IMPROVING RELIABILITY IN A SEMICONDUCTOR DEVICE | 11/21/2006 | 5/19/2009 |
| US | 7994014B2 | SEMICONDUCTOR DEVICES HAVING FACETED SILICIDE CONTACTS, AND RELATED FABRICATION METHODS | 12/15/2006 | 4/27/2010 |
| US | 7994020B2 | METHOD OF FORMING FINNED SEMICONDUCTOR DEVICES WITH TRENCH ISOLATION | 9/4/2007 | 6/29/2010 |



PATENT
REEL: 047014 FRAME: 0789

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| US | 8039878B2 | TRANSISTOR HAVING A CHANNEL WITH TENSILE STRAIN AND ORIENTED ALONG A CRYSTALLOGRAPHIC ORIENTATION WITH INCREASED CHARGE CARRIER MOBILITY | 6/2/2008 | 2/5/2013 |
| US | 8283718 | INTEGRATED CIRCUIT SYSTEM WITH METAL AND SEMI-CONDUCTING GATE | 5/21/2009 | 3/5/2013 |
| US | 8368221B2 | HYBRID CONTACT STRUCTURE WITH LOW ASPECT RATIO CONTACTS IN A SEMICONDUCTOR DEVICE | 7/22/2005 | 7/26/2011 |
| US | 8390127B2 | CONTACT TRENCHES FOR ENHANCING STRESS TRANSFER IN CLOSELY SPACED TRANSISTORS | 12/16/2006 | 10/9/2012 |
| US | 8431466B2 | METHOD OF FORMING FINNED SEMICONDUCTOR DEVICES WITH TRENCH ISOLATION | 10/4/2012 | 8/26/2014 |
| US | 8815727 | INTEGRATED CIRCUIT WITH METAL AND SEMI-CONDUCTING GATE | 12/17/2002 | 11/28/2007 |
| US | 9373548B2 | CMOS CIRCUIT HAVING A TENSILE STRESS LAYER OVERLYING AN NMOS TRANSISTOR AND OVERLAPPING A PORTION OF COMPRESSIVE STRESS LAYER | 12/20/2002 | 7/2/2008 |
| TW | 200416898A | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE | 1/15/2004 | 7/29/2009 |



PATENT
REEL: 047014 FRAME: 0790

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| TW | 201013928A | CONTACT TRENCHES FOR ENHANCING STRESS TRANSFER IN CLOSELY SPACED TRANSISTORS | 4/19/2006 | 11/23/2011 |
| TW | 526590B | INTEGRATION OF ORGANIC FILL FOR DUAL DAMASCENE PROCESS | 4/19/2006 | 2/22/2012 |
| TW | I292595B | SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION AND METHOD FOR FABRICATING THE SAME | 3/29/2007 | 6/15/2011 |
| TW | I294679B | | 11/16/2007 | 10/12/2011 |
| TW | I355733B | LOW STRESS SIDEWALL SPACER IN INTEGRATED CIRCUIT T | 12/13/2007 | 10/12/2011 |
| TW | I370518B | FORMATION OF ABRUPT JUNCTIONS IN DEVICES BY USING SILICIDE GROWTH DOPANT SNOWPLOW EFFECT | 10/5/2009 | 1/22/2014 |
| TW | I382493B | INTEGRATED CIRCUIT AND METHOD OF MANUFACTURE | 10/26/2004 | 3/16/2011 |
| TW | I409949B | A TRANSISTOR HAVING A CHANNEL WITH TENSILE STRAIN AND ORIENTED ALONG A CRYSTALLOGRAPHIC ORIENTATION WITH INCREASED CHARGE CARRIER MOBILITY | 10/29/2004 | 11/26/2009 |



PATENT
REEL: 047014 FRAME: 0791

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| TW | I440097B | STRESS ENHANCED MOS TRANSISTOR AND METHODS FOR ITS FABRICATION | 4/29/2005 | 3/29/2012 |
| TW | I443750B | A TECHNIQUE FOR FROMING A CONTACT INSULATION LAYER WITH ENHANCED STRESS TRANSFER EFFICIENCY | 1/31/2006 | 8/30/2007 |
| TW | I453828B | STRESS ENHANCED TRANSISTOR AND METHODS FOR ITS FABRICATION | 3/31/2006 | 3/10/2011 |
| TW | I498998B | METHOD OF FORMING FINNED SEMICONDUCTOR DEVICES WITH TRENCH ISOLATION | 4/28/2006 | 5/12/2011 |
| TW | I542001B | CONTACT TRENCHES FOR ENHANCING STRESS TRANSFER IN CLOSELY SPACED TRANSISTORS | 6/30/2009 | 7/11/2016 |
| KR | 100954874B1 | SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION AND METHOD FOR FABRICATING THE SAME | 6/30/2008 | 1/7/2010 |
| KR | 101132823B1 | A TRANSISTOR HAVING A CHANNEL WITH TENSILE STRAIN AND ORIENTED ALONG A CRYSTALLOGRAPHIC ORIENTATION WITH INCREASED CHARGE CARRIER MOBILITY | 3/28/2002 | 2/1/2007 |
| KR | 101229099B1 | INTEGRATED CIRCUIT AND METHOD OF MANUFACTURE | 12/17/2002 | 9/25/2008 |



PATENT
REEL: 047014 FRAME: 0792

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| KR | 101386711B1 | STRESS ENHANCED MOS TRANSISTOR AND METHODS FOR ITS FABRICATION | 10/26/2004 | 2/26/2009 |
| KR | 101415284B1 | STRESS ENHANCED TRANSISTOR AND METHODS FOR ITS FABRICATION | 12/21/2004 | 11/26/2009 |
| KR | 101638532B1 | METHOD OF FORMING FINNED SEMICONDUCTOR DEVICES WITH TRENCH ISOLATION | 7/21/2009 | 7/20/2016 |
| KR | 101639771B1 | SEMICONDUCTOR DEVICES HAVING FACETED SILICIDE CONTACTS, AND RELATED FABRICATION METHODS | 10/5/2009 | 7/14/2016 |
| KR | 20110049806A | METHOD OF FORMING FINNED SEMICONDUCTOR DEVICES WITH TRENCH ISOLATION | 12/13/2007 | 2/2/2012 |
| JP | 4597531B2 | DOPANT DISTRIBUTION OF THE CHANNEL FIELD THE OUTDATED GRADE IN THE 1ST PART OF THE SEMICONDUCTOR REGION WHICH WAS FORMED ON THE PRODUCTION | 11/16/2007 | 9/30/2010 |
| JP | 5096319B2 | THE INTEGRATED CIRCUIT AND ITS PRODUCTION MANNERED | 12/20/2002 | 12/22/2004 |
| JP | 5204645B2 | TECHNOLOGY OF FORMING A CONTACT INSULATING LAYER IN THE REINFORCED STRESS TRANSMISSION EFFICIENCY | 1/15/2004 | 11/9/2005 |



PATENT
REEL: 047014 FRAME: 0793

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| JP | 5265872B2 | SIDEWALL SPACER OF LOW STRESS IN INTEGRATED CIRCUIT TECHNOLOGY | 11/16/2007 | 8/18/2010 |
| JP | 5281014B2 | THE STRESS REINFORCEMENT TRANSISTOR AND ITS PRODUCTION MANNERED | 7/21/2009 | 4/20/2011 |
| JP | 5283233B2 | THE STRESS STRENGTHENING MOS TRANSISTOR AND THAT PRODUCTION MANNERED | 12/17/2002 | 4/20/2005 |
| JP | 5555698B2 | BEING TRENCH SEPARABLE MANNER FOR THE MANNERED NULL FIN DIE SEMICONDUCTOR | 10/26/2004 | 5/16/2007 |
| JP | 5785496B2 | SEMICONDUCTOR DEVICES AND RELATED MANUFACTURING METHOD HAS A FACET SILICIDE CONTACT | 12/21/2004 | 8/20/2008 |
| GB | 2401991B | METHOD AND APPARATUS FOR CONTROLLING DIE ATTACH FILLET HEIGHT TO REDUCE DIE SHEAR STRESS | 10/24/2007 | 8/11/2010 |
| GB | 2425404B | FORMATION OF ABRUPT JUNCTIONS IN DEVICES BY USING SILICIDE GROWTH DOPANT SNOWPLOW EFFECT | 3/29/2007 | 6/8/2011 |
| GB | 2425405B | LOW STRESS SIDEWALL SPACER IN INTEGRATED CIRCUIT TECHNOLOGY | 12/13/2007 | 7/6/2011 |



PATENT
REEL: 047014 FRAME: 0794

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| GB | 2439883B | INTEGRATED CIRCUIT AND METHOD OF MANUFACTURE | 12/20/2002 | |
| GB | 2450838B | A TRANSISTOR HAVING A CHANNEL WITH TENSILE STRAIN AND ORIENTED ALONG A CRYSTALLOGRAPHIC ORIENTATION WITH INCREASED CHARGE CARRIER MOBILITY | 4/19/2006 | |
| GB | 2457411B | STRESS ENHANCED TRANSISTOR AND METHODS FOR ITS FABRICATION | 4/19/2006 | |
| EP | 1488461A1 | SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION AND METHOD FOR FABRICATING THE SAME | 12/21/2004 | |
| EP | 1593161A1 | STRAINED CHANNEL FINFET | 12/13/2007 | |
| EP | 2095408B1 | STRESS ENHANCED MOS TRANSISTOR AND METHODS FOR ITS FABRICATION | 11/16/2007 | |
| EP | 2311077A1 | METHOD OF FORMING FINNED SEMICONDUCTOR DEVICES WITH TRENCH ISOLATION | 7/21/2009 | |
| DE | 102004052578B4 | A METHOD FOR PRODUCING A DIFFERENT MECHANICAL DEFORMATION IN THE DIFFERENT CHANNEL REGIONS BY FORMING A AN ETCHING STOP LAYER STACK WITH DIFFERENTLY MODIFIED INTERNAL TENSION | 10/5/2009 | |



PATENT
REEL: 047014 FRAME: 0795

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| DE | 102005020133B4 | A PROCESS FOR THE PREPARATION OF A TRANSISTOR CELL WITH ART FOR THE PRODUCTION OF A CONTACT INSULATION LAYER HAVING IMPROVED VOLTAGE TRANSMISSION EFFICIENCY | 12/20/2002 | |
| DE | 102006004412B3 | A METHOD FOR INCREASING THE ETCHING SELECTIVITY IN A CONTACT STRUCTURE IN A SEMICONDUCTOR | 3/29/2007 | |
| DE | 102006015087B4 | A METHOD FOR THE PRODUCTION OF TRANSISTORS | 4/19/2006 | |
| DE | 102006019835B4 | TRANSISTOR WITH A CHANNEL WITH TENSILE STRAIN, THE ALONG A CRYSTALLOGRAPHIC ORIENTATION IS ORIENTED AT AN INCREASED CHARGE CARRIER MOBILITY | 11/16/2007 | |
| DE | 102008030852A1 | GROOVES FOR THE SAKE OF BETTER BRACING BY TRANSMISSION IN TRANSISTORS WITH A SMALL DISTANCE | 12/13/2007 | |
| DE | 10214066B4 | SEMICONDUCTOR COMPONENT WITH RETROGRADE DOPING PROFILE IN A CHANNEL REGION AND A METHOD FOR PRODUCING THE SAME | 7/21/2009 | |
| DE | 10297642B4 | A METHOD FOR CONTROLLING THE HEIGHT OF THE CHIP SUPPORT EDGE SEAM, IN ORDER TO REDUCE SURFACE OF THE BORE-HOLE LOADS CHIP | 8/29/2003 | 9/1/2004 |



PATENT
REEL: 047014 FRAME: 0796

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| DE | 112004002401B4 | PRODUCTION OF AN ABRUPT TRANSITIONS IN STRUCTURAL ELEMENTS, WITH THE USE OF THE "DOPANT SNOW PLOW EFFECT" ("DOPANT SNOWPLOW EFFECT") IN THE CASE OF THE SILICIDE GROWTH | 6/30/2009 | 4/1/2010 |
| DE | 112004002638B4 | A METHOD FOR THE PRODUCTION OF AN INTEGRATED CIRCUIT WITH SIDES OF WALL DISTANCE HOLDERS WITH A SMALL CLAMPING | 1/18/2002 | 4/1/2003 |
| DE | 112007003116B4 | A PROCESS FOR THE PREPARATION OF A CLAMPED TRANSISTOR AND THE TRANSISTOR | 3/19/2003 | 1/11/2008 |
| DE | 602007008611D1 | VOLTAGE INCREASED MOS - TRANSISTOR AND A METHOD FOR ITS PRODUCTION | 1/9/2003 | 3/11/2008 |
| CN | 100352041C | METHOD AND APPARATUS FOR CONTROLLING DIE ATTACH FILLET HEIGHT TO REDUCE DIE SHEAR STRESS | 1/7/2005 | 1/1/2012 |
| CN | 100399576C | SEMICONDUCTOR DEVICE HAVING A RETROGRADE DOPANT PROFILE IN A CHANNEL REGION AND METHOD FOR FABRICATING THE SAME | 11/4/2004 | 8/11/2012 |
| CN | 100521230C | STRAINED CHANNEL FINFET | 5/1/2006 | 1/11/2013 |



PATENT
REEL: 047014 FRAME: 0797

| Country | Grant No. | Title | Filing Date | Issue Date |
|---|---|---|---|---|
| CN | 101167169B | TECHNIQUE FOR FORMING A CONTACT INSULATION LAYER WITH ENHANCED STRESS TRANSFER EFFICIENCY | 4/23/2007 | 9/21/2013 |
| CN | 101171671B | INTEGRATED CIRCUIT AND METHOD OF MANUFACTURE | 11/19/2007 | 6/1/2014 |
| CN | 101432882B | A TRANSISTOR HAVING A CHANNEL WITH TENSILE STRAIN AND ORIENTED ALONG A CRYSTALLOGRAPHIC ORIENTATION WITH INCREASED CHARGE CARRIER MOBILITY | 4/26/2006 | 7/1/2014 |
| CN | 101578690B | STRESS ENHANCED MOS TRANSISTOR AND METHODS FOR ITS FABRICATION | 12/13/2007 | 9/21/2014 |
| CN | 101663761B | STRESS ENHANCED TRANSISTOR AND METHODS FOR ITS FABRICATION | 7/20/2009 | 9/1/2015 |
| CN | 102177573B | SEMICONDUCTOR DEVICES HAVING FACETED SILICIDE CONTACTS, AND RELATED FABRICATION METHODS | 1/23/2003 | 10/12/2004 |
| CN | 1886838B | FORMATION OF ABRUPT JUNCTIONS IN DEVICES BY USING SILICIDE GROWTH DOPANT SNOWPLOW EFFECT | 10/29/2002 | 4/19/2005 |



RECORDED: 07/06/2018
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REEL: 047014 FRAME: 0798