PATENT ASSIGNMENT COVER SHEET

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Stylesheet Version v1.2

EPAS ID: PAT5374620

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
MORGAN STANLEY SENIOR FUNDING, INC.	02/11/2019

RECEIVING PARTY DATA

Name:	NXP B.V.
Street Address:	High Tech Campus 60
City:	Eindhoven
State/Country:	NETHERLANDS
Postal Code:	NL-5656 AG

PROPERTY NUMBERS Total: 182

Property Type	Number
Patent Number:	7726011
Patent Number:	7485916
Patent Number:	6551881
Patent Number:	6380721
Patent Number:	6222353
Patent Number:	6433622
Patent Number:	6326283
Patent Number:	6544860
Patent Number:	8159032
Patent Number:	7304526
Patent Number:	7728404
Patent Number:	7482669
Patent Number:	7485534
Patent Number:	7199010
Patent Number:	7262460
Patent Number:	7459750
Patent Number:	7265574
Patent Number:	7312526
Patent Number:	6861875
Patent Number:	6833583

Property Type	Number
Patent Number:	6936890
Patent Number:	6521498
Patent Number:	6559502
Patent Number:	6319777
Patent Number:	6600194
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Patent Number:	6498071
Patent Number:	6420755
Patent Number:	6368921
Patent Number:	6359308
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Patent Number:	7671440
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Patent Number:	8344448
Patent Number:	7504690
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Patent Number:	6057227
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Patent Number:	6100712
Patent Number:	9305789
Patent Number:	9230953

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Patent Number:	7907007

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Patent Number:	8169084
Patent Number:	7839209
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Patent Number:	8062974
Patent Number:	8093097
Patent Number:	7952333
Application Number:	14743038
Application Number:	14478866
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Application Number:	14725366
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Application Number:	14746612
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Application Number:	14848003
Application Number:	14849469
Application Number:	14530189
Application Number:	15049419
Application Number:	14527365
Application Number:	14801635
Application Number:	14984614
Application Number:	15044005
Application Number:	14984880
Application Number:	14874189
Application Number:	14802840
Application Number:	14668154
Application Number:	14704768
Application Number:	14322553
Application Number:	14835403
Application Number:	14693756
Application Number:	14450062
Application Number:	14704692
Application Number:	14059831
Application Number:	14499654
Application Number:	14249108

Property Type	Number
Application Number:	14293146
Application Number:	14072122
Application Number:	14056648
Application Number:	14714927
Application Number:	14180418
Application Number:	14644272
Application Number:	14703731
Application Number:	13288570
Application Number:	13502229
Application Number:	13264816

CORRESPONDENCE DATA

Fax Number: (512)895-6630

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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Email: angie.zalewski@nxp.com

Correspondent Name: INTELLECTUAL PROPERTY AND LICENSING NXP

Address Line 1: 6501 WILLIAM CANNON DRIVE WEST TX30/OE62

Address Line 4: AUSTIN, TEXAS 95134

ATTORNEY DOCKET NUMBER:	RELEASE OF SECURITY INTER
NAME OF SUBMITTER:	ANGIE ZALEWSKI
SIGNATURE:	/Angie Zalewski/
DATE SIGNED:	02/13/2019

Total Attachments: 10

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RELEASE OF SECURITY INTEREST IN INTELLECTUAL PROPERTY

THIS RELEASE OF LIEN (this "**Release**") is made as of February 11, 2019 (the "**Effective Date**") by Morgan Stanley Senior Funding, Inc., as collateral agent (the "**Agent**") in favor of NXP B.V., with its corporate seat in Eindhoven, the Netherlands (the "**Grantor**"). Capitalized terms not defined herein shall have the meanings ascribed to such terms in the Credit Agreement (as defined below).

WHEREAS, the Grantor entered into that certain revolving credit agreement (the "**Credit Agreement**"), dated as December 7, 2015 (as amended, amended and restated, supplemented or otherwise modified from time to time prior to the date hereof) among the Grantor, NXP Funding LLC, a Delaware limited liability company and the Agent;

WHEREAS, in connection with the its obligations under the Credit Agreement (the "**Obligations**"), the Grantor entered into that certain security agreement (the "**Security Agreement**"), dated as of September 29, 2006 as supplemented by the Supplement to the Security Agreement dated as of February 18, 2016 (and as further amended, amended and restated, supplemented or otherwise modified from time to time prior to the date hereof) among Philips Semiconductors USA Inc., NXP Funding LLC and the Agent; and

WHEREAS, in connection with the Obligations under the Credit Agreement and the Security Agreement, the Grantor entered into that certain patent security agreement (the "**Patent Security Agreement**"), dated as of September 29, 2006 (as amended, amended and restated, supplemented or otherwise modified from time to time prior to the date hereof) among the Grantor and the Agent, which assigned to the Agent, for its benefit, a continuing first priority security interest in and to all of its right, title and interest in, to and under the patents listed on Schedule A hereto (the "**Intellectual Property**") as security for the due and punctual payment and performance in full, whether at stated maturity, by required prepayment, declaration, acceleration, demand or otherwise, of the Obligations.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Agent hereby, on behalf of itself and its respective successors and assigns, hereby: (i) fully releases and discharges any and all liens, security interests, right, title and interest it may have, in whole or in part, in, to and under all of the Intellectual Property of the Grantor granted to the Agent pursuant to the IP Security Agreement, together with the goodwill of the business symbolized thereby and all applications and registrations related thereto; (ii) re-assigns to the Grantor any and all such right, title and interest that it may have in any such Intellectual Property; (iii) agrees that it shall execute all other documents and do all other acts necessary to relinquish and effect the release of such rights to the Grantor; and (iv) authorizes and requests that the United States Patent and Trademark Office and United States Copyright Office note and record the release hereby given and any other filings necessary to evidence the release and termination of the Agent's rights under each of the Credit Agreement and the IP Security Agreement, with respect to any such Intellectual Property.

Notwithstanding anything herein (or in any other document, communication or filing relating hereto by any person) to the contrary, the Agent is authorizing solely the release of the security interests granted pursuant to the Security Agreement, IP Security Agreement and the Grantor's obligations under the Credit Agreement, and not any other liens or security interests at any time granted by the Grantor or any other grantor in favor of Morgan Stanley Senior Funding, Inc. or in favor of any other person.

This Release may be executed in any number of counterparts and by different parties in separate counterparts, each of which when so executed shall be deemed to be an original and all of which taken together shall constitute one and the same agreement.

This Release shall be governed by, and construed and interpreted in accordance with, the laws of the State of New York.

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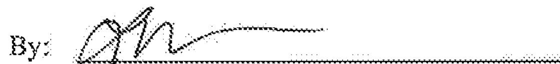
PATENT
REEL: 048328 FRAME: 0971

IN WITNESS WHEREOF, the Administrative Agent has caused this Release to be executed, on behalf of itself and the Lenders, by its duly authorized representative effective as of the Effective Date.

MORGAN STANLEY SENIOR FUNDING, INC.,
as Administrative Agent

By: 

Name: Lisa Hanson

Title: Vice President

Schedule A

PATENTS

NXP ReferenceNumber	Status	Title	Region	PriorityDate	FiledDate	ApplicationNumber	PublicationNumber	PatentNumber	Owners
000922US1	Granted	Method to improve accuracy, linearity and temperature drift of Current Sense MOSFETs	US	2005-06-01	2006-05-30	11/916110	US20080191779	US7952333	NXP B.V.
000990US1	Granted	Layer Sequence and Method of Manufacturing a Layer Sequence	US	2005-06-15	2006-06-12	11/917092	US20080206588	US8093097	NXP B.V.
001018CN1	Granted	Semiconductor Device with Grounding Structure	CN	2005-08-09	2006-07-31	200680029211.1		CN200680029211	NXP B.V.
001018US1	Granted	Semiconductor Device with Grounding Structure	US	2005-08-09	2006-07-31	11/997240	US20080217785	US8062974	NXP B.V.
001563US1	Granted	Area-efficient multiplexer based logic blocks for FPGAs	US	2005-09-05	2006-09-04	12/065634	US20080224732	US7696783	NXP B.V.
002087US3	Granted	4-Level Logic Decoder	US	2005-07-22	2006-07-21	11/996315	US20080211543	US7550997	NXP B.V.
003984CN04	Granted	A Substrate Isolated Integrated High Voltage Diode with Shallow Trench Isolation Inside the Unit Cel	CN	2005-12-19	2006-12-12	200680047677.4	CN101331612	CN200680047677	NXP B.V.
003984US2	Granted	A Substrate Isolated Integrated High Voltage Diode with Shallow Trench Isolation Inside the Unit Cel	US	2005-12-19	2006-12-12	12/158108	US20080265327	US7659584	NXP B.V.
006172CN	Granted	ESD protection for external decoupling grounds	CN	2006-06-20	2007-06-15	200780023275.5	CN101473437	CN200780023275	NXP B.V.
006172JP	Granted	ESD protection for external decoupling grounds	JP	2006-06-20	2007-06-15	2009-516033		JP5069745	NXP B.V.
006172US1	Granted	ESD protection for external decoupling grounds	US	2006-06-20	2007-06-15	12/305686	US20090185317	US7944658	NXP B.V.
006172US2	Granted	INTEGRATED CIRCUIT AND ASSEMBLY THEREWITH	US	2007-06-15	2007-06-15	13/030695	US20110141639	US8134815	NXP B.V.
006642CN	Granted	Buried SiGe Tunnel MOSFET	CN	2006-10-05	2007-10-03	200780036958.4	CN101523607	CN200780036958	NXP B.V.
006642US1	Granted	Buried SiGe Tunnel MOSFET	US	2006-10-05	2007-10-03	12/444140	US20100097135	US7839209	NXP B.V.
007085US1	Granted	Soft solder metal on top of passivation layer below top surface level	US	2006-11-13	2007-11-12	12/514269	US20100032848	US8169084	NXP B.V.
007085CN	Granted	Soft solder metal on top of passivation layer below top surface level	CN	2006-11-13	2007-11-12	200780042015.2	CN101536184	CN200780042015	NXP B.V.
007085DE03	Granted	Soft solder metal on top of passivation layer below top surface level	DE	2006-11-13	2007-11-12	07849095.0	EP2092561	DE602007029739	NXP B.V.
007288US	Granted	A commutating auto zero amplifier with low output noise and improved accuracy	US	2006-10-27	2007-10-19	12/447278	US20100045378	US7907007	NXP B.V.
007868US1	Granted	3D system level ESD protection in passive substrate	US	2007-02-12	2008-02-08	12/525179	US20100085672	US8184415	NXP B.V.
007868FR02	Granted	3D system level ESD protection in passive substrate	FR	2007-02-12	2008-02-08	08709970.1		FR2130226	NXP B.V.
007868DE03	Granted	3D system level ESD protection in passive substrate	DE	2007-02-12	2008-02-08	08709970.1		DE602008016170	NXP B.V.
007868GB04	Granted	3D system level ESD protection in passive substrate	GB	2007-02-12	2008-02-08	08709970.1		GB2130226	NXP B.V.
81049923CN03	Granted	Arrangement and Approach for Coupling Power Supplies Using Controlled Switching Techniques	CN	2007-11-30	2008-11-27	200880118109.8	CN101897100	CN200880118109	NXP B.V.
81049923US05	Granted	Arrangement and Approach for Coupling Power Supplies Using Controlled Switching Techniques	US	2007-11-30	2008-11-27	12/745275	US20100301673	US8264801	NXP B.V.
81049949EP03	Published	Current Flow Optimised Single Finger ESD Protection Structure	EP	2008-09-11	2009-09-09	09787147.9	EP2335283		NXP B.V.
81049949US04	Granted	current flow optimised single finger ESD protection structure	US	2008-09-11	2009-09-09	13/063189	US20110216459	US8390971	NXP B.V.
81050250EP2	Published	Meander resistor improvements for ESD purposes	EP	2008-07-02	2009-07-02	09773012.1	EP2308088		NXP B.V.
81050250US04	Granted	Meander resistor improvements for ESD purposes	US	2008-07-02	2009-07-02	13/002082	US20110241820	US8258916	NXP B.V.
81051180US04	Granted	Enhanced RESURF Stepped Oxide Concept	US	2007-10-29	2008-10-22	12/739341	US20100320532	US8357971	NXP B.V.
81051180FR05	Granted	Enhanced RESURF Stepped Oxide Concept	FR	2007-10-29	2008-10-22	08843598.7		FR2206154	NXP B.V.
81051180DE06	Granted	Enhanced RESURF Stepped Oxide Concept	DE	2007-10-29	2008-10-22	08843598.7		DE602008007988	NXP B.V.
81051180GB07	Granted	Enhanced RESURF Stepped Oxide Concept	GB	2007-10-29	2008-10-22	08843598.7		GB2206154	NXP B.V.
81057065EP03	Published	Trench Gate Semiconductor Device and Method of Manufacturing Thereof	EP	2008-05-28	2009-05-20	09754266.6	EP2286455		NXP B.V.
81342039CN03	Granted	Design- and processing method for building mesh-structured semiconductor devices with improved metal adhesion avoiding increased underetching and metal grooves	CN	2007-11-27	2008-10-22	200880117821.6	CN101874301	CN200880117821	NXP B.V.
81342039US05	Granted	Design- and processing method for building mesh-structured semiconductor devices with improved metal adhesion avoiding increased underetching and metal grooves	US	2007-11-27	2008-10-22	12/744368	US20100244275	US8809695	NXP B.V.
81344334US04	Granted	ESD protection devices with integrated capacitors with high capacitance density, high operating voltage and high accuracy resistors.	US	2008-10-28	2009-10-22	13/126233	US20110204480	US8901705	NXP B.V.
81346707US03	Granted	METHODS, SYSTEMS AND DEVICES FOR ELECTROSTATIC DISCHARGE PROTECTION	US	2009-11-26	2009-11-26	13/502807	US20120205780	US8810004	NXP B.V.
81350999EP03	Published	Low Voltage Non-Resurf Trenchmos	EP	2008-07-25	2009-07-27	09786726.1	EP2308095		NXP B.V.
81350999US04	Granted	Low Voltage Non-Resurf Trenchmos	US	2008-07-25	2009-07-27	13/055742	US20110121384	US8901638	NXP B.V.
81359596US04	Published	Lead passivation in PLZT cover layer for providing a smooth low-dielectric cover layer for the deposition of reliable high-quality resistors.	US	2009-04-20	2010-04-14	13/264816	US20120045881		NXP B.V.
81383262CN02	Granted	A 3D RESURF EDGE TERMINATION	CN	2010-08-16	2011-08-12	201110230833.3	CN102376750	CN201110230833	NXP B.V.
81383262US03	Granted	EDGE TERMINATION REGION	US	2010-08-16	2011-08-15	13/210308	US20120037980	US8513733	NXP B.V.
81383262DE04	Granted	A 3D RESURF EDGE TERMINATION	DE	2010-08-16	2010-08-16	10172933.3		DE602010026171	NXP B.V.
81387908US01	Granted	VOLTAGE REGULATOR WITH GATE RESISTOR FOR IMPROVED EFFICIENCY	US		2009-11-02	12/610959	US20110101952	US8324878	NXP B.V.
81390103CN03	Granted	Surge protection device manufactured in a double side process	CN	2009-10-22	2010-10-22	201080047531.6	CN102576740	CN201080047531	NXP B.V.
81390103US04	Published	Surge protection device manufactured in a double side process	US	2009-10-22	2010-10-22	13/502229	US20120200976		NXP B.V.
81394335US02	Granted	Improved Reliability of Gate Busbar under Clip	US	2010-09-21	2011-09-20	13/237878	US20120070983	US8652904	NXP B.V.
81394335DE03	Granted	Improved Reliability of Gate Busbar under Clip	DE	2010-09-21	2010-09-21	10178090.6		DE602010020096	NXP B.V.
81394335FR04	Granted	Improved Reliability of Gate Busbar under Clip	FR	2010-09-21	2010-09-21	10178090.6		FR2432023	NXP B.V.
81394335GB05	Granted	Improved Reliability of Gate Busbar under Clip	GB	2010-09-21	2010-09-21	10178090.6		GB2432023	NXP B.V.
81397787US01	Granted	ESD PROTECTION CIRCUIT	US		2011-01-07	12/986970	US20120175672	US8686470	NXP B.V.
81397787DE03	Granted	ESD PROTECTION CIRCUIT	DE	2011-01-07	2012-01-05	12150305.6		DE602012002603	NXP B.V.
81397787FR04	Granted	ESD PROTECTION CIRCUIT	FR	2011-01-07	2012-01-05	12150305.6		FR2475008	NXP B.V.
81397787GB05	Granted	ESD PROTECTION CIRCUIT	GB	2011-01-07	2012-01-05	12150305.6		GB2475008	NXP B.V.
81406887US01	Granted	ESD Protection Device	US		2011-01-28	13/016443	US20120193675	US8441031	NXP B.V.
81406887CN02	Granted	ESD Protection Device	CN	2011-01-28	2012-01-18	201210016467.6	CN102623449	CN201210016467	NXP B.V.
81406887EP03	Published	ESD Protection Device	EP	2011-01-28	2012-01-24	12152254.4	EP2482314		NXP B.V.

81406887DE04	Allowed	ESD Protection Device	DE	2011-01-28	2012-01-24	12152254.4			NXP B.V.
81409292US01	Published	CMOS ADJUSTABLE OVER VOLTAGE ESD AND SURGE PROTECTION FOR LED APPLICATION	US		2011-11-03	13/288570	US20130114169		NXP B.V.
81409292CN02	Granted	CMOS ADJUSTABLE OVER VOLTAGE ESD AND SURGE PROTECTION FOR LED APPLICATION	CN	2011-11-03	2012-10-29	201210422160.6	CN103094893	CN103094893	NXP B.V.
81409292DE04	Granted	CMOS Adjustable Over-Voltage, ESD and Surge Protection for LED Application	DE	2011-11-03	2012-08-13	12180332.4		DE602012001969	NXP B.V.
81409292FR05	Granted	CMOS Adjustable Over-Voltage, ESD and Surge Protection for LED Application	FR	2011-11-03	2012-08-13	12180332.4		FR2590218	NXP B.V.
81409292GB06	Granted	CMOS Adjustable Over-Voltage, ESD and Surge Protection for LED Application	GB	2011-11-03	2012-08-13	12180332.4		GB2590218	NXP B.V.
81409938US01	Granted	BACKDRIVE PROTECTION CIRCUIT	US		2011-03-21	13/052271	US20120242372	US8400193	NXP B.V.
81409938EP02	Published	Backdrive-Protection for PMOS Output Stages	EP	2011-03-21	2012-03-14	12159384.2	EP2503690		NXP B.V.
81413430CN02	Granted	Half Bridge Input Capacitance integrated into a Power MOSFET	CN	2011-08-02	2012-08-01	201210272108.7	CN102916010	CN102916010	NXP B.V.
81413430US03	Granted	Half Bridge Input Capacitance integrated into a Power MOSFET	US	2011-08-02	2012-07-16	13/549684	US20130181272	US8735957	NXP B.V.
81413430US04	Granted	Half Bridge Input Capacitance integrated into a Power MOSFET	US	2011-08-02	2012-07-16	14/249204	US20140220749	US9129991	NXP B.V.
81415814EP01	Published	Method for macroscopic modulation of the sheet resistance of AlGaN/GaN heterostructures for a better on-resistance / breakdown voltage trade-off.	EP		2011-12-19	11194254.6	EP2608268		NXP B.V.; TSMC
81415814CN02	Published	Method for macroscopic modulation of the sheet resistance of AlGaN/GaN heterostructures for a better on-resistance / breakdown voltage trade-off.	CN	2011-12-19	2012-12-17	201210548299.5	CN103165668		NXP B.V.; TSMC
81415814US04	Published	Semiconductor Device	US	2012-11-14	2015-05-04	14/703731	US20150236095		NXP B.V.; TSMC
81416301US01	Granted	Integrated Advance Copper Fuse Combined with ESD/Over-Voltage/Reverse Polarity Protection	US		2011-08-24	13/216328	US20130050883	US8711532	NXP B.V.
81416301CN02	Granted	Integrated Advance Copper Fuse Combined with ESD/Over-Voltage/Reverse Polarity Protection	CN	2011-08-24	2012-08-23	201210302940.7	CN102956635	CN201210302940	NXP B.V.
81416301EP03	Published	Integrated Advance Copper Fuse Combined with ESD/Over-Voltage/Reverse Polarity Protection	EP	2011-08-24	2012-08-02	12179026.5	EP2562812		NXP B.V.
81416751US01	Granted	PROTECTION CIRCUIT	US		2012-04-24	13/454862	US20130279053	US9203237	NXP B.V.
81416751CN02	Published	PROTECTION CIRCUIT	CN	2012-04-24	2013-04-23	201310143018.2	CN103490399		NXP B.V.
81418015US01	Granted	CURRENT-SENSING CIRCUIT	US		2011-08-16	13/211055	US20130043941	US8493097	NXP B.V.
81418015CN02	Granted	CURRENT-SENSING CIRCUIT	CN	2011-08-16	2012-08-13	201210286951.0	CN102955058	CN102955058	NXP B.V.
81421708CN02	Published	GROUP 13 NITRIDE SEMICONDUCTOR DEVICE AND METHOD OF ITS MANUFACTURE	CN	2012-05-09	2013-05-08	201310167053.8	CN103390639		NXP B.V.
81421708US03	Granted	GROUP 13 NITRIDE SEMICONDUCTOR DEVICE AND METHOD OF ITS MANUFACTURE	US	2012-05-09	2013-05-03	13/887065	US20130299846	US9147732	NXP B.V.
81421708DE04	Granted	GROUP 13 NITRIDE SEMICONDUCTOR DEVICE AND METHOD OF ITS MANUFACTURE	DE	2012-05-09	2012-05-09	12167365.1		DE602012006262	NXP B.V.
81421708FR05	Granted	GROUP 13 NITRIDE SEMICONDUCTOR DEVICE AND METHOD OF ITS MANUFACTURE	FR	2012-05-09	2012-05-09	12167365.1		FR2662884	NXP B.V.
81421708GB06	Granted	GROUP 13 NITRIDE SEMICONDUCTOR DEVICE AND METHOD OF ITS MANUFACTURE	GB	2012-05-09	2012-05-09	12167365.1		GB2662884	NXP B.V.
81422840US03	Granted	ADVANCED RESURF CONCEPT FOR LV TRENCHMOS ((HZG - ID380)	US	2011-12-07	2012-10-24	13/659678	US20130146967	US9006822	NXP B.V.
81422840US04	Published	ADVANCED RESURF CONCEPT FOR LV TRENCHMOS ((HZG - ID380)	US	2011-12-07	2015-03-11	14/644272	US20150187913		NXP B.V.
81423241US01	Granted	Circuit connector apparatus and method therefor	US		2011-12-02	13/309878	US20130140705	US8508035	NXP B.V.
81423241CN02	Granted	Circuit connector apparatus and method therefor	CN	2011-12-02	2012-11-28	201210495227.9	CN103137586	CN201210495227	NXP B.V.
81426343US01	Granted	LOW/HIGH VOLTAGE SELECTOR	US		2012-10-04	13/645339	US20140097686	US9130553	NXP B.V.
81427050CN02	Published	Spike Suppression in half bridge circuits through increased CGD achieved via isolation trench connection	CN	2011-12-07	2012-12-05	201210517752.6	CN103151352		NXP B.V.
81427050US04	Granted	SEMICONDUCTOR DEVICE HAVING ISOLATION TRENCHES	US	2011-12-07	2012-11-21	13/682792	US20130146972	US9048116	NXP B.V.
81476171US02	Granted	CASCODED SEMICONDUCTOR DEVICES	US	2012-07-30	2013-07-09	13/937451	US20140027785	US8847235	NXP B.V.
81476171DE03	Granted	CASCODED SEMICONDUCTOR DEVICES	DE	2012-07-30	2012-07-30	12178518.2		DE602012010268	NXP B.V.
81492812CN02	Published	ELECTRONIC DEVICE AND METHOD OF MANUFACTURING SUCH DEVICE	CN	2012-06-19	2013-06-17	201310238283.9	CN103515447		NXP B.V.
81494852EP01	Published	DISCRETE SEMICONDUCTOR DEVICE PACKAGE AND MANUFACTURING METHOD	EP		2012-06-01	12170528.9	EP2669936		NXP B.V.
81494852US02	Granted	DISCRETE SEMICONDUCTOR DEVICE PACKAGE AND MANUFACTURING METHOD	US	2012-06-01	2013-05-08	13/890055	US20130320551	US8981566	NXP B.V.
81494852CN03	Published	DISCRETE SEMICONDUCTOR DEVICE PACKAGE AND MANUFACTURING METHOD	CN	2012-06-01	2013-05-29	201310205500.4	CN103456706		NXP B.V.
81494852US03	Granted	DISCRETE SEMICONDUCTOR DEVICE PACKAGE AND MANUFACTURING METHOD	US	2012-06-01	2013-05-08	14/607587	US20150140739	US9263335	NXP B.V.
81494938US01	Published	TRANSISTOR WITH REDUCTED PARASITIC	US		2014-02-14	14/180418	US20150236090		NXP B.V.
81494938CN02	Published	TRANSISTOR WITH REDUCTED PARASITIC	CN	2014-02-14	2015-02-05	201510060791.1	CN104851914		NXP B.V.
81495073EP01	Published	HETEROJUNCTION SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD	EP		2012-05-22	12168884.0	EP2667415		NXP B.V.
81495073CN02	Published	HETEROJUNCTION SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD	CN	2012-05-22	2013-05-17	201310184881.2	CN103426914		NXP B.V.
81495073US03	Granted	HETEROJUNCTION SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD	US	2012-05-22	2013-05-15	13/895228	US20130320400	US9064847	NXP B.V.
81495073US04	Application	HETEROJUNCTION SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD	US	2012-05-22	2015-05-18	14/714927			NXP B.V.
81526196EP01	Published	Method for Leakage Matching in High Voltage GaN devices in Cascode arrangement	EP		2013-03-28	13161707.8	EP2784816		NXP B.V.
81526196CN02	Published	Method for Leakage Matching in High Voltage GaN devices in Cascode arrangement	CN	2013-03-28	2014-02-17	201410053613.1	CN104078461		NXP B.V.
81526196US03	Granted	Method for Leakage Matching in High Voltage GaN devices in Cascode arrangement	US	2013-03-28	2014-03-13	14/208180	US20140292287	US9268351	NXP B.V.
81526950EP01	Published	CASCODED SEIMICONDUCTOR DEVICES	EP		2012-11-23	12194083.7	EP2736171		NXP B.V.
81526950CN02	Published	CASCODED SEIMICONDUCTOR DEVICES	CN	2012-11-23	2013-11-20	201310587250.5	CN103840821		NXP B.V.
81526950US03	Published	CASCODED SEIMICONDUCTOR DEVICES	US	2012-11-23	2013-10-17	14/056648	US20140145208		NXP B.V.
81527056EP01	Published	ESD PROTECTION	EP		2012-12-06	12195904.3	EP2741330		NXP B.V.
81527056CN02	Published	ESD PROTECTION	CN	2012-12-06	2013-12-04	201310647833.2	CN103855703		NXP B.V.
81527056US03	Allowed	ESD PROTECTION	US	2012-12-06	2013-11-05	14/072122	US20140160607		NXP B.V.
81527347CN02	Published	CASCODED SEMICONDUCTOR DEVICES	CN	2012-11-23	2013-11-19	201310581564.4	CN103855919		NXP B.V.
81527347US03	Granted	CASCODED SEMICONDUCTOR DEVICES	US	2012-11-23	2013-11-19	14/084441	US20140146428	US9190826	NXP B.V.
81527347DE04	Granted	CASCODED SEMICONDUCTOR DEVICES	DE	2012-11-23	2012-11-23	12194065.4		DE602012008012	NXP B.V.
81527347GB05	Granted	CASCODED SEMICONDUCTOR DEVICES	GB	2012-11-23	2012-11-23	12194065.4		GB2736170	NXP B.V.
81527756US01	Granted	A PROPORTIONAL-INTEGRAL DERIVATIVE (PID) ANALOG CONTROLLER AND A METHOD FOR TESTING A PID ANALOG CONTROLLER OF A DC/DC CONVERTER	US		2012-12-05	13/705508	US20140152339	US9091741	NXP B.V.
81527756EP02	Published	A PROPORTIONAL-INTEGRAL DERIVATIVE (PID) ANALOG CONTROLLER AND A METHOD FOR TESTING A PID ANALOG CONTROLLER OF A DC/DC CONVERTER	EP	2012-12-05	2013-10-02	13187114.7	EP2841408		NXP B.V.
81530905EP01	Published	A Field Emission ESD Protection Device with Field Enhanced Electrode Structure	EP		2013-06-26	13173864.3	EP2819165		NXP B.V.
81530905CN02	Published	A Field Emission ESD Protection Device with Field Enhanced Electrode Structure	CN	2013-06-26	2014-06-25	201410290791.6	CN104253022		NXP B.V.

81530905US03	Allowed	A Field Emission ESD Protection Device with Field Enhanced Electrode Structure	US	2013-06-26	2014-06-02	14/293146	US20150001671		NXP B.V.
81531494EP01	Published	A lateral field emission ESD protection device with well defined cathode-anode distance	EP		2013-06-26	13173868.4	EP2819166		NXP B.V.
81531494CN02	Published	A lateral field emission ESD protection device with well defined cathode-anode distance	CN	2013-06-26	2014-06-19	201410276234.9	CN104253021		NXP B.V.
81531494US03	Granted	ELECTRIC FIELD GAP DEVICE AND MANUFACTURING METHOD	US	2013-06-26	2014-06-11	14/301445	US20150002966	US9236734	NXP B.V.
81531809CN02	Published	GaN HEMTs AND GaN DIODES	CN	2012-12-19	2013-12-19	201310706281.8	CN103887334		NXP B.V.
81531809US03	Granted	GaN HEMTs AND GaN DIODES	US	2012-12-19	2013-12-16	14/108042	US20140167064	US8962461	NXP B.V.
81533159US01	Granted	Electrode Coating for Electron Emission Devices with Cavities	US		2014-04-24	14/261246	US20150311024	US9190237	NXP B.V.
81533159CN02	Published	Electrode Coating for Electron Emission Devices with Cavities	CN	2014-04-24	2015-04-23	201510199715.9	CN105006413		NXP B.V.
81533159EP03	Published	Electrode Coating for Electron Emission Devices with Cavities	EP	2014-04-24	2015-03-26	15161025.0	EP2937887		NXP B.V.
81533360CN02	Published	CASCODE CIRCUIT	CN	2012-12-17	2013-12-13	201310684492.6	CN103872006		NXP B.V.
81533360US03	Granted	CASCODE CIRCUIT	US	2012-12-17	2013-12-03	14/094890	US20140167822	US9171837	NXP B.V.
81536838EP01	Published	Integrated gate circuit to enable reverse conduction of GaN cascode switch configurations	EP		2013-04-05	13162597.2	EP2787641		NXP B.V.
81536838CN02	Published	Integrated gate circuit to enable reverse conduction of GaN cascode switch configurations	CN	2013-04-05	2014-04-04	201410136435.9	CN104104384		NXP B.V.
81536838US03	Granted	Integrated gate circuit to enable reverse conduction of GaN cascode switch configurations	US	2013-04-05	2014-03-17	14/215243	US20140300410	US9116533	NXP B.V.
81536884EP01	Published	The use of TiW(N) in NXP's GaN Schottky process platform	EP		2013-04-15	13163745.6	EP2793265		NXP B.V.
81536884CN02	Published	The use of TiW(N) in NXP's GaN Schottky process platform	CN	2013-04-15	2014-04-14	201410147952.6	CN104103684		NXP B.V.
81536884US03	Allowed	The use of TiW(N) in NXP's GaN Schottky process platform	US	2013-04-15	2014-04-09	14/249108	US20140306232		NXP B.V.
81546142EP01	Published	SiGe diode with Reduced Surface Field Effect structure	EP		2013-10-02	13187183.2	EP2858117		NXP B.V.
81546142CN02	Published	SiGe diode with Reduced Surface Field Effect structure	CN	2013-10-02	2014-09-29	201410514957.8	CN104518035		NXP B.V.
81546142US03	Published	SiGe diode with Reduced Surface Field Effect structure	US	2013-10-02	2014-09-29	14/499654	US20150091023		NXP B.V.
81588804US01	Published	ANTENNA RESONANCE FREQUENCY CONTROL DRIVER	US		2013-10-22	14/059831	US20150108848		NXP B.V.
81588804CN02	Published	ANTENNA RESONANCE FREQUENCY CONTROL DRIVER	CN	2013-10-22	2014-10-21	201410563005.5	CN104577358		NXP B.V.
81589015EP02	Published	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD	EP	2014-05-08	2014-07-10	14176489.4	EP2942815		NXP B.V.
81589015CN03	Application	Diffusion barrier capping layers on Ni Schottky gate based devices	CN	2014-05-08	2015-05-06	201510226968.0			NXP B.V.
81589015US04	Published	Diffusion barrier capping layers on Ni Schottky gate based devices	US	2014-05-08	2015-05-05	14/704692	US20150325698		NXP B.V.
81591088EP01	Published	Proposal to use parallel power mosfets in softstart / hotswap and other current controlled applications such that the safe operating area of each device is protected	EP		2013-08-30	13182494.8	EP2843496		NXP B.V.
81591088CN02	Published	Proposal to use parallel power mosfets in softstart / hotswap and other current controlled applications such that the safe operating area of each device is protected	CN	2013-08-30	2014-08-22	201410418576.X	CN104426515		NXP B.V.
81591088US03	Published	Proposal to use parallel power mosfets in softstart / hotswap and other current controlled applications such that the safe operating area of each device is protected	US	2013-08-30	2014-08-01	14/450062	US20150061620		NXP B.V.
81592616CN03	Application	Trench Schottky Diode with Wide Trench Termination	CN	2014-05-14	2015-05-13	201510240970.3			NXP B.V.
81592616US04	Published	Trench Schottky Diode with Wide Trench Termination	US	2014-05-14	2015-04-22	14/693756	US20150333133		NXP B.V.
81617121EP01	Published	Unidirectional ESD protection device based on a vertical SCR	EP		2013-10-21	13189593.0	EP2863432		NXP B.V.
81617121CN02	Published	Unidirectional ESD protection device based on a vertical SCR	CN	2013-10-21	2014-10-17	201410553798.2	CN104576638		NXP B.V.
81617121US03	Granted	Unidirectional ESD protection device based on a vertical SCR	US	2013-10-21	2014-10-17	14/516978	US20150108536	US9230953	NXP B.V.
81625066EP02	Published	Schottky barrier tuning with nitrogen in TiWN gates on GaN	EP	2014-05-08	2014-07-09	14176284.9	EP2942805		NXP B.V.
81625066CN03	Published	Schottky barrier tuning with nitrogen in TiWN gates on GaN	CN	2014-05-08	2015-04-15	201510178296.0	CN105097900		NXP B.V.
81625066US04	Granted	Schottky barrier tuning with nitrogen in TiWN gates on GaN	US	2014-05-08	2015-04-22	14/693118	US20150325667	US9305789	NXP B.V.
81625333EP01	Published	Electronic slope-control circuit for cascoded power semiconductor devices	EP		2014-09-25	14186451.2	EP3001563		NXP B.V.
81625333CN02	Application	Electronic slope-control circuit for cascoded power semiconductor devices	CN	2014-09-25	2015-09-23	201510613256.4			NXP B.V.
81625333US03	Published	Electronic slope-control circuit for cascoded power semiconductor devices	US	2014-09-25	2015-08-25	14/835403	US20160094218		NXP B.V.
81625347EP01	Application	Integrated clamp circuit for insulated gate cascoded power semicondutor devices	EP		2015-08-27	15182739.1			NXP B.V.
81626973CN02	Published	Exposed-Die Quad Flat No-Leads (QFN) Package	CN	2014-07-02	2015-07-01	201510378353.X	CN105244294		NXP B.V.
81626981US01	Application	Exposed-Heatsink Quad Flat No-Leads (QFN) Package	US		2014-07-02	14/322553			NXP B.V.
81626981CN02	Published	Exposed-Heatsink Quad Flat No-Leads (QFN) Package	CN	2014-07-02	2015-07-01	201510378835.5	CN105304506		NXP B.V.
81627757EP02	Published	Capacitance reduction of ESD protection devices	EP	2014-05-19	2014-07-10	14176616.2	EP2947691		NXP B.V.
81627757CN03	Published	Capacitance reduction of ESD protection devices	CN	2014-05-19	2015-05-18	201510251633.4	CN105097787		NXP B.V.
81627757US04	Published	Capacitance reduction of ESD protection devices	US	2014-05-19	2015-05-05	14/704768	US20150333119		NXP B.V.
81627855EP01	Published	The use of sacrificial PECVD nitride for better manufacturability of NXP's GaN Schottky process of record	EP		2014-04-11	14164449.2	EP2930754		NXP B.V.
81627855US02	Published	The use of sacrificial PECVD nitride for better manufacturability of NXP's GaN Schottky process of record	US	2014-04-11	2015-03-25	14/668154	US20150295051		NXP B.V.
81628762EP01	Published	Symmetric HV EDMOS with split gate-field plate	EP		2014-08-05	14179923.9	EP2983210		NXP B.V.
81628762CN02	Published	Symmetric HV EDMOS with split gate-field plate	CN	2014-08-05	2015-07-31	201510462961.9	CN105336788		NXP B.V.
81628762US03	Published	Symmetric HV EDMOS with split gate-field plate	US	2014-08-05	2015-07-17	14/802840	US20160043708		NXP B.V.
81629304CN02	Application	LEADLESS SEMICONDUCTOR DEVICE AND METHOD OF MAKING THEROF	CN	2014-10-29	2015-10-27	201510706346.8			NXP B.V.
81633299EP01	Application	Packaging solution to obtain low current-collapse for GaN Schottky-Barrier Diodes	EP		2014-12-03	14196049.2			NXP B.V.
81633299CN02	Application	Packaging solution to obtain low current-collapse for GaN Schottky-Barrier Diodes	CN	2014-12-03	2015-12-02	201510868768.5			NXP B.V.
81633299US03	Application	Packaging solution to obtain low current-collapse for GaN Schottky-Barrier Diodes	US	2014-12-03	2015-10-02	14/874189			NXP B.V.
81637732EP01	Application	Hybrid SiGe / Si Schottky Diode	EP		2015-01-30	15153336.1			NXP B.V.
81637732US02	Application	Hybrid SiGe / Si Schottky Diode	US	2015-01-30	2015-12-30	14/984880			NXP B.V.
81637737EP01	Application	Shockley Diode used in an ESD/EOS protection device	EP		2015-03-09	15158272.3			NXP B.V.
81637737US02	Application	Shockley Diode used in an ESD/EOS protection device	US	2015-03-09	2016-02-15	15/044005			NXP B.V.
81638315EP01	Application	a fully symmetric common mode choke	EP		2015-01-20	15151828.9			NXP B.V.
81638315CN02	Application	a fully symmetric common mode choke	CN	2015-01-20	2016-01-19	201610034290.0			NXP B.V.
81638315US03	Application	a fully symmetric common mode choke	US	2015-01-20	2015-12-30	14/984614			NXP B.V.

81640640EP01	Published	Connecting wire for side solderable multiple leads terminal (support market demand for DSN package of side solderable on multiple leads end)	EP		2014-08-01	14179517.9	EP2980845		NXP B.V.
81640640CN02	Published	Connecting wire for side solderable multiple leads terminal (support market demand for DSN package of side solderable on multiple leads end)	CN	2014-08-01	2015-07-29	201510454935.1	CN105321919		NXP B.V.
81640640US03	Published	Connecting wire for side solderable multiple leads terminal (support market demand for DSN package of side solderable on multiple leads end)	US	2014-08-01	2015-07-16	14/801635	US20160035651		NXP B.V.
81641854US01	Application	PACKAGE WITH MULTIPLE I/O SIDE-SOLDERABLE TERMINALS	US		2014-10-29	14/527365			NXP B.V.
81641854CN02	Application	PACKAGE WITH MULTIPLE I/O SIDE-SOLDERABLE TERMINALS	CN	2014-10-29	2015-10-28	201510711207.4			NXP B.V.
81644279EP01	Application	Expose Die & Clip Chip Scale Package embedded with encapsulated mold compounc	EP		2015-03-06	15157936.4			NXP B.V.
81644279CN02	Application	Expose Die & Clip Chip Scale Package embedded with encapsulated mold compounc	CN	2015-03-06	2016-03-04	201610124596.5			NXP B.V.
81644279US03	Application	Expose Die & Clip Chip Scale Package embedded with encapsulated mold compounc	US	2015-03-06	2016-02-22	15/049419			NXP B.V.
81645442US01	Application	Autonomous Power Supply	US		2014-10-31	14/530189			NXP B.V.
81645442CN02	Application	Autonomous Power Supply	CN	2014-10-31	2015-10-30	201510727366.3			NXP B.V.
81645442EP03	Published	Autonomous Power Supply	EP	2014-10-31	2015-09-22	15186263.8	EP3016242		NXP B.V.
81645442JP04	Application	Autonomous Power Supply	JP	2014-10-31	2015-09-09	2015--177421			NXP B.V.
81647296EP01	Published	Via-on-via metallization to reduce capacitance	EP		2014-10-08	14188213.4	EP3007224		NXP B.V.
81647296CN02	Application	Via-on-via metallization to reduce capacitance	CN	2014-10-08	2015-10-08	201510645378.1			NXP B.V.
81647296US03	Application	Via-on-via metallization to reduce capacitance	US	2014-10-08	2015-09-09	14/849469			NXP B.V.
81647304EP01	Published	Integrated SCR and Diode as bidirectional ESD protection	EP		2014-10-08	14188198.7	EP3007232		NXP B.V.
81647304CN02	Application	Integrated SCR and Diode as bidirectional ESD protection	CN	2014-10-08	2015-09-29	201510632924.8			NXP B.V.
81647304US03	Application	Integrated SCR and Diode as bidirectional ESD protection	US	2014-10-08	2015-09-08	14/848003			NXP B.V.
81648912EP01	Application	chip scale semiconductor device	EP		2015-01-27	15152673.8			NXP B.V.
81648912CN02	Application	chip scale semiconductor device	CN	2015-01-27	2016-01-26	201610052223.1			NXP B.V.
81648912US03	Application	chip scale semiconductor device	US	2015-01-27	2016-01-05	14/988443			NXP B.V.
81649286US01	Application	Built-up lead frame / substrate DFN Package with side solderable terminals	US		2015-06-22	14/746612			NXP B.V.
81649482EP01	Application	Poly Field Plate Design for Trench MOS Components	EP		2014-12-10	14197250.5			NXP B.V.
81649482CN02	Application	Poly Field Plate Design for Trench MOS Components	CN	2014-12-10	2015-12-10	201510916758.4			NXP B.V.
81649482US03	Application	Poly Field Plate Design for Trench MOS Components	US	2014-12-10	2015-10-09	14/879394			NXP B.V.
81649956US01	Application	INTERFACE APPARATUS WITH LEAKAGE MITIGTATION	US		2015-05-29	14/725366			NXP B.V.
81652148EP01	Application	Spatial distribution of different types of passivation layers on III-N semiconductors	EP		2015-12-10	15199187.4			NXP B.V.
81652603EP01	Application	Proper metal contact to p-GaN layer to reduce dynamic on-resistance	EP		2015-11-27	15196730.4			NXP B.V.
81662221EP01	Application	Leadframe Package with Cladded Metal Insert Structure on Leadframe	EP		2015-12-21	15201716.6			NXP B.V.
81663020EP01	Application	wafer back grooving before metal application	EP		2015-11-20	15195639.8			NXP B.V.
81672043EP01	Application	Chip-scale package transistor with front-side contact solder pads	EP		2015-09-29	15187379.1			NXP B.V.
81675054EP01	Application	DEEP (B+) Graded Profile Engineering HV for 3 and 4 terminal TrenchMOS	EP		2015-09-11	15184799.3			NXP B.V.
81676497EP01	Application	full-wafer-moulded dual-half-cut chip-scale-package process	EP		2015-07-27	15178458.4			NXP B.V.
81678210CN01	Application	Laser ablation method to make solderable side lead of leadless packages with 3 or more IO leads at a axis	CN		2015-12-01	201510867964.0			NXP B.V.
81678647CN01	Application	Dual Side Solderable Pads (SSP-2) Package concept	CN		2015-08-21	201510518287.1			NXP B.V.
81678953EP01	Application	Packaging solution to obtain shielding against electromagnetic interference for GaN HEMTs used as high-side switches	EP		2015-11-11	15194122.6			NXP B.V.
81679773CN01	Application	Frameless Package	CN		2015-12-11	201510919622.9			NXP B.V.
81688408EP01	Application	Controlling of GaN Cascode Floating-Node Voltage	EP		2016-01-18	16151746.1			NXP B.V.
81689549EP01	Application	Use of a "graded body contact" to ensure optimal device triggering in GGNmost ESD protections.	EP		2015-10-27	15191760.6			NXP B.V.
81689575EP01	Application	DSN0603LV side protection – Wafer level Package Concept I (Laser Via)	EP		2015-11-11	15194136.6			NXP B.V.
81690973EP01	Application	SIDEWALL ISOLATION FOR WAFER LEVEL- CHIP-SCALE PACKAGE DEVICES	EP		2015-12-15	15200095.6			NXP B.V.
81692019EP01	Application	Insulated-gate GaN HEMTs with local Schottky contacts to improve device robustness	EP		2016-01-05	16150164.8			NXP B.V.
81693027EP01	Application	Integrated Resistor on a GaN Die	EP		2016-01-18	16151749.5			NXP B.V.
81694981US01	Application	Plasma diced overmolded chip scale package	US		2016-03-03	15/060548			NXP B.V.
A 001317US	Granted	OUTPUT DRIVER CIRCUIT WITH JUMP START FOR CURRENT SINK	US		1997-12-17	08/992290		US6100712	NXP B.V.
A 023763US	Granted	METHOD FOR A CONSISTENT SHALLOW TRENCH ETCH PROFILE	US		1999-10-04	09/411758		US6342428	NXP B.V.
A 023880KR	Granted	BI-DIRECTIONAL ESD STRUCTURE.	KR	1999-12-17		2001-7010388	KR20010102184	KR0751104	NXP B.V.
A 023880TW	Granted	BI-DIRECTIONAL ESD STRUCTURE.	TW	1999-12-17	2000-12-08	089126209	TW478134	TW151311	NXP B.V.
A 023881KR	Granted	IMPROVED ESD DIODE STRUCTURE.	KR	1999-12-17		2001-7010364	KR20010102167	KR0678781	NXP B.V.
A 023881TW	Granted	IMPROVED ESD DIODE STRUCTURE.	TW	1999-12-17	2000-12-08	089126223	TW477055	TW150627	NXP B.V.
A 023881US	Granted	IMPROVED ESD DIODE STRUCTURE.	US		1999-12-17	09/466411		US6674129	NXP B.V.
A 050690US	Granted	SHALLOW TRENCH ISOLATION STRUCTURE AND METHOD FOR MAKING SAME	US		1996-09-30	08/723903		US5753561	NXP B.V.
A 050755US	Granted	SILICON-ENRICHED SHALLOW TRENCH OXIDE FOR REDUCED RECESS DURING LDD SPACER ETCH	US		1997-08-06	08/907099		US6013558	NXP B.V.
A 050821US	Granted	OXIDE ETCH STOP TECHNIQUES FOR UNIFORM DAMASCENE TRENCH DEPT	US		1997-06-23	08/880580		US6057227	NXP B.V.
A 050887US	Granted	DIFFERENTIAL MOS CURRENT-MODE LOGIC CIRCUIT HAVING HIGH GAIN AND FAST SPEED	US		1997-10-20	08/955012		US5977800	NXP B.V.
A 050973US	Granted	SEMICONDUCTOR DEVICE HAVING LOAD DEVICE WITH TRENCH ISOLATIO	US		1998-05-20	09/083251		US6140188	NXP B.V.
A 050976US	Granted	SHALLOW TRENCH CAPACITIVE STRUCTURES FOR SUPPRESSING INDUCTI	US		1998-03-31	09/052865		US6010939	NXP B.V.
A 050990US	Granted	METHOD FOR FORMING ALIGNED VIAS UNDER TRENCHES IN A DUAL DAM	US		1998-06-19	09/100639		US6221759	NXP B.V.
A 050991USA	Granted	MOSFET STRUCTURE HAVING IMPROVED SOURCE/DRAIN JUNCTION PERFORMANCE	US	1998-09-01	1998-09-01	09/836936		US6465311	NXP B.V.
A 051190US	Granted	HIGH DIFFERENTIAL IMPEDANCE LOAD	US		1999-09-01	09/388034		US6154018	NXP B.V.
A 051231US	Granted	NON-POWER-OF-TWO GREY-CODE COUNTER AND BINARY INCREMENTER TH	US		1999-11-04	09/434218		US6314154	NXP B.V.
A 051241US	Granted	TRENCH-DIFFUSION CORNER ROUNDING IN SHALLOW-TRENCH (STI) PRO	US		1999-12-16	09/465151		US6150234	NXP B.V.
B 034178US	Granted	POWER S/C TEMPERATURE SENSE (DIODE+MOST) CIRCUIT	US	1997-08-08	1998-08-06	09/129809		US6084462	NXP B.V.

B 034205US	Granted	VOLTAGE REGULATOR + REF. FOR S/C POWER DEVICES	US	1997-10-17	1998-10-16	09/174222		US6060871	NXP B.V.
B 034265US	Granted	TRENCH MOST WITH POLYSILICON SIDEWALL SOURCE	US	1998-07-11	1999-07-07	09/348960		US6251730	NXP B.V.
B 034272US	Granted	MOSFET/IGBT WITH SILICON-GERMANIUM SOURCE	US	1998-08-14	1999-08-12	09/372961		US6255692	NXP B.V.
B 034274US	Granted	DIFFERENTIAL TEMPERATURE SENSE CELLS IN POWER MOS	US	1998-08-20	1999-08-19	09/377359		US6144085	NXP B.V.
B 034370US	Granted	DC-DC CONVERTER WITH SELF-ADJUSTING POWER FET	US	1999-07-02	2000-06-29	09/606340		US6175225	NXP B.V.
B 034430US	Granted	COOL D-MOSFETS USING SELECTIVE EPITAXIAL GROWTH	US	1999-12-15	2000-12-14	09/738921	US20010006831	US6495421	NXP B.V.
D 096109US	Granted	COMPONENT WITH A CAPACITOR	US	1996-07-31	1997-07-30	08/903143		US6125027	NXP B.V.
DE000016US	Granted	SEMICONDUCTORS DEVICE WITH METAL LAYER	US	2000-01-27	2001-01-25	09/769179	US20010017421	US6417564	NXP B.V.
DE000053US	Granted	SCHOTTKY DIODE	US	2000-03-30	2001-03-28	09/819281	US20010042862	US6583485	NXP B.V.
DE030189US1	Granted	MONOLITHIC INTEGRATED PUNCH-THROUGH-DIODE	US	2003-05-27	2004-05-25	10/561895	US20060158801	US7528459	NXP B.V.
DE030275US1	Granted	OPERATION AND CIRCUITRY OF A POWER CONVERSION AND CONTROL..	US	2003-08-12	2004-08-09	10/567396	US20080150609	US7579900	NXP B.V.
DE030313US1	Granted	FAILURE PREDICTION FOR PARALLEL MOSFETS	US	2003-09-03	2004-08-20	10/570211	US20070007519	US7330046	NXP B.V.
F 095520US	Granted	LOW VOLTAGE LOGIC CELL	US	1995-04-12	1996-04-12	08/631385		US5717347	NXP B.V.
GB000159US	Granted	TRENCH MOS STRUCTURE WITH LOW CGD AND GATE PROTECTION	US	2000-11-17	2001-11-16	09/993201		US6566708	NXP B.V.
GB010045US	Granted	RESURF LATERAL MOS WITH LOW QCD/CGD	US	2001-03-23	2002-03-15	10/099688	US20020135016	US6664593	NXP B.V.
GB010052GB	Granted	AUTONOMOUS SYNCHRONOUS RECTIFIER	GB	2001-03-28		02714378.3		GB1388208	NXP B.V.
GB010080EP	Published	MOSFET DRIVER WITH DUAL FLOATING GATES, LOCAL SOURCE CONNECT	EP	2001-02-06		02715637.1	EP1360763		NXP B.V.
GB010080KR	Granted	MOSFET DRIVER WITH DUAL FLOATING GATES, LOCAL SOURCE CONNECT	KR	2001-02-06		2002-7013347	KR20020093025	KR0863879	NXP B.V.
GB010080US	Granted	MOSFET DRIVER WITH DUAL FLOATING GATES, LOCAL SOURCE CONNECT	US	2001-02-06	2002-02-04	10/066991	US20020175661	US6603291	NXP B.V.
GB010080JP	Granted	MOSFET DRIVER WITH DUAL FLOATING GATES, LOCAL SOURCE CONNECT	JP	2001-02-06		2002-563598		JP4067967	NXP B.V.
GB010080DE07	Allowed	MOSFET DRIVER WITH DUAL FLOATING GATES, LOCAL SOURCE CONNECT	DE	2001-02-06		02715637.1			NXP B.V.
GB010121US	Granted	PROUD SILICIDE POLYSILICON TRENCH-GATE MOSFET	US	2001-07-24	2002-07-17	10/197651	US20030020102	US6707100	NXP B.V.
GB010121USA	Granted	PROUD SILICIDE POLYSILICON TRENCH-GATE MOSFET	US	2001-07-24	2002-07-17	10/733214	US20040124461	US6855601	NXP B.V.
GB010124US	Granted	Manufacture of Semiconductor Devices with Schottky Barriers	US	2001-07-24	2002-07-19	10/199000	US20030022474	US6825105	NXP B.V.
GB010146US	Granted	Trench-Gate Semiconductor Devices and their Manufacture	US	2001-09-13	2002-08-06	10/213460	US20030047779	US6800900	NXP B.V.
GB010184US	Granted	MOSFET PRECISION CURRENT LIMIT/MEASURE SCHEME	US	2001-02-22	2002-02-07	10/068920	US20020114116	US6717787	NXP B.V.
GB010184FR07	Granted	MOSFET PRECISION CURRENT LIMIT/MEASURE SCHEME	FR	2001-02-22		02711159.0		FR1366569	NXP B.V.
GB010184DE08	Granted	MOSFET PRECISION CURRENT LIMIT/MEASURE SCHEME	DE	2001-02-22		02711159.0		DE60240387	NXP B.V.
GB010184GB09	Granted	MOSFET PRECISION CURRENT LIMIT/MEASURE SCHEME	GB	2001-02-22		02711159.0		GB1366569	NXP B.V.
GB010192US	Granted	EDGE TERMINATION BELOW CONNECTION FINGERS IN MOSFET	US	2001-09-04	2002-08-26	10/227672	US20030042556	US6780714	NXP B.V.
GB010210US	Granted	ASCOT MOSFET PLANARISED TEOS CAPPING	US	2001-04-28	2002-04-26	10/134213	US20020160573	US6534367	NXP B.V.
GB020153US	Granted	REDUCING LOSSES IN TRENCHMOS WITH INTRINSIC REGIONS	US	2002-09-20	2002-11-12	10/293991	US20030094650	US6784488	NXP B.V.
GB020162CN	Granted	COMPENSATED SENSEMOS	CN	2002-09-28		03822899.8	CN1685519	CN03822899	NXP B.V.
GB020162US	Granted	COMPENSATED SENSEMOS	US	2002-09-28	2003-09-12	10/528941	US20060163652	US7439582	NXP B.V.
GB020183US	Granted	TRENCHMOS WITH N/P HALO	US	2002-11-06	2003-10-24	10/533725	US20060043434	US7253459	NXP B.V.
GB020212US	Granted	FEEDBACK SIGNAL FOR POWER SWITCHING CIRCUIT	US	2002-11-29	2003-11-19	10/536244	US20060066288	US7102337	NXP B.V.
GB020212DE08	Granted	FEEDBACK SIGNAL FOR POWER SWITCHING CIRCUIT	DE	2002-11-29		03812224.8		DE60342503	NXP B.V.
GB020218US	Granted	TRENCHFET WITH TRENCHED FIELD PLATE BELOW GATE	US	2002-05-31	2003-05-21	10/515748	US20050173758	US7122860	NXP B.V.
GB020218FR07	Granted	TRENCHFET WITH TRENCHED FIELD PLATE BELOW GATE	FR	2002-05-31		03725542.9		FR1525621	NXP B.V.
GB020218DE08	Granted	TRENCHFET WITH TRENCHED FIELD PLATE BELOW GATE	DE	2002-05-31		03725542.9		DE60338736	NXP B.V.
GB020218GB09	Granted	TRENCHFET WITH TRENCHED FIELD PLATE BELOW GATE	GB	2002-05-31		03725542.9		GB1525621	NXP B.V.
GB020239US	Granted	TRENCHMOS - DMOS HYBRID	US	2002-10-04	2003-09-15	10/529731	US20060001084	US7504690	NXP B.V.
GB030081US1	Granted	EDGE TERMINATION USING LATERAL MOSFETS	US	2003-05-31	2004-05-21	10/561531	US20110291185	US8344448	NXP B.V.
GB030096CN1	Granted	BI-DIRECTIONAL TRENCHFET	CN	2003-06-20		200480017151.2	CN1809931	CN200480017151	NXP B.V.
GB030096US1	Granted	BI-DIRECTIONAL TRENCHFET	US	2003-06-20	2004-06-10	10/562254	US20060202305	US7629647	NXP B.V.
GB030097US1	Granted	BI-DIRECTIONAL TRENCHFETS WITH SURFACE FIELD REDUCING STRUCT	US	2003-06-20	2004-06-10	10/561732	US20080203473	US7671440	NXP B.V.
GB030211US1	Granted	SUBCHANNEL p REGION WITH FIELD PLATE	US	2003-11-29	2004-11-26	10/580624	US20070132014	US7408223	NXP B.V.
GB030213CN1	Granted	DEEP TRENCH DIELECTRIC WITH GRADED DOPING	CN	2003-11-29		200480035223.6	CN1886836	CN200480035223	NXP B.V.
GB030213US1	Granted	DEEP TRENCH DIELECTRIC WITH GRADED DOPING	US	2003-11-29	2004-11-26	10/580619	US20070108515	US7696599	NXP B.V.
GB040053US1	Granted	Trench Field Effect Transistor and Method of Making It	US	2004-03-03	2005-02-23	10/591192	US20070181940	US7579649	NXP B.V.
GB040056CN1	Granted	RSI TRENCHFET PROCESS	CN	2004-03-10		200580007471.4	CN1930689	CN200580007471	NXP B.V.
GB040056US1	Granted	RSI TRENCHFET PROCESS	US	2004-03-10	2005-02-28	10/591352	US20070181975	US7361555	NXP B.V.
GB040056US2	Granted	Trench-Gate Transistors and their Manufacture	US	2004-03-10	2005-02-28	12/041117	US20080150021	US8222693	NXP B.V.
GB040080CN1	Granted	RESURF MOSFET WITH SI CAPPING LAYER	CN	2004-03-31		200580010342.0	CN1947261	CN200580010342	NXP B.V.
GB040080US1	Granted	RESURF MOSFET WITH SI CAPPING LAYER	US	2004-03-31	2005-03-29	10/594487	US20070222019	US7394144	NXP B.V.
GB040080JP1	Granted	RESURF MOSFET WITH SI CAPPING LAYER	JP	2004-03-31		2007-505726		JP4932701	NXP B.V.
GB040152US1	Granted	POWERMOS WITH CELLS OF DIFFERENT THRESHOLD VOLTAGE	US	2004-07-20	2005-07-18	11/658223	US20080315278	US7737507	NXP B.V.
GB040153US1	Granted	DIVIDED GATE DRIVE FOR HIGH GAIN MOSFETS	US	2004-07-20	2005-07-18	11/658224	US20090212846	US7843259	NXP B.V.
GB040173US1	Granted	A LOW VOLTAGE TUNEABLE TRENCH MOSFET	US	2004-09-08	2005-09-06	11/574973	US20080064166	US7504307	NXP B.V.
GB050036CN1	Granted	3 TERMINAL MOSFET WITH TEMPERATURE SENSE FACILITY	CN	2005-03-15		200680008339.X		CN200680008339	NXP B.V.
GB050036US1	Granted	3 TERMINAL MOSFET WITH TEMPERATURE SENSE FACILITY	US	2005-03-15	2006-03-14	11/908664	US20090066404	US8742825	NXP B.V.
GB050041US1	Granted	BURIED LAYERS IN A SILICON PROCESS	US	2005-03-24	2006-03-21	11/909446	US20080277764	US7772100	NXP B.V.
N 015307US	Granted	SMD DIODE PACKAGE WITH CONDUCTIVE STRIPS	US	1995-05-12	1996-05-13	08/645436		US5712197	NXP B.V.
N 015595US	Granted	SMD PACKAGE FOR OSP DIODE WITH CONTACT PIN	US	1995-12-14	1996-12-10	08/762515		US5930653	NXP B.V.
N 016143US	Granted	HV - LDMOST WITH INACTIVE FINGERTIPS	US	1996-12-23	1997-12-22	08/995467		US5910670	NXP B.V.
N 016298US	Granted	MAKING A DEVICE WITH SHALLOW TRENCH ISOLATION	US	1997-04-07	1998-03-19	09/044499		US5966616	NXP B.V.
N 016509US	Granted	FABRICATION METHOD FOR SCHOTTBY DIODES	US	1997-09-03	1998-08-27	09/141644		US6218222	NXP B.V.
N 017214US	Granted	TRENCHMOST USING RESURF	US	1998-11-28	1999-11-29	09/450229		US6541817	NXP B.V.

N 017572US	Granted	TRENCH MOST EDGE TERMINATION BY WIDE/DEEP TRENCH	US	1999-07-22	2000-07-24	09/624481		US6359308	NXP B.V.
N 017666US	Granted	SELF-ALIGNED TRENCH FET PROCESS USING SOURCE DIFFUSION	US	1999-09-28	2000-09-28	09/671888		US6368921	NXP B.V.
N 017731US	Granted	CSP FOR POWER TRANSISTORS	US	1999-11-11	2000-11-10	09/709663		US6420755	NXP B.V.
N 017786US	Granted	SELF-ALIGNED TRENCH MOST PROCESS WITH SIDE-WALL SOURCE	US	1999-11-30	2000-11-29	09/725410	US20010009800	US6498071	NXP B.V.
NL000065US	Granted	MULTI-RESURF DIODE WITH SEMI-INSULATING LAYERS	US	2000-02-12	2001-02-12	09/781498	US20010013613	US6436779	NXP B.V.
NL000131US	Granted	LV-MOSFET WITH 1-OF-N DRAIN CONNECTION PLUG	US	2000-03-10	2001-03-09	09/803325		US6600194	NXP B.V.
NL000162FR	Granted	LATERAL DEEP-TRENCH RESURF MOS DEVICE	FR	2000-03-23		01915329.5		FR1208600	NXP B.V.
NL000162DE	Granted	LATERAL DEEP-TRENCH RESURF MOS DEVICE	DE	2000-03-23		01915329.5		DE60132158	NXP B.V.
NL000162GB	Granted	LATERAL DEEP-TRENCH RESURF MOS DEVICE	GB	2000-03-23		01915329.5		GB1208600	NXP B.V.
NL000247US	Granted	STEPPED OXIDE FABRICATION IN INVERSE TRENCH MOS	US	2000-04-26	2001-04-24	09/840816		US6319777	NXP B.V.
NL000247FR	Granted	STEPPED OXIDE FABRICATION IN INVERSE TRENCH MOS	FR	2000-04-26		01936228.4		FR1281200	NXP B.V.
NL000247DE	Granted	STEPPED OXIDE FABRICATION IN INVERSE TRENCH MOS	DE	2000-04-26		01936228.4		DE60130647	NXP B.V.
NL000247GB	Granted	STEPPED OXIDE FABRICATION IN INVERSE TRENCH MOS	GB	2000-04-26		01936228.4		GB1281200	NXP B.V.
NL000299US	Granted	LATERAL TRENCH MOS GATE COOL-MOS EXTENSIONS	US	2000-05-20	2001-05-18	09/860311	US20010045578	US6559502	NXP B.V.
NL000299GB2	Granted	LATERAL TRENCH MOS GATE COOL-MOS EXTENSIONS	GB	2000-05-20		01943310.1		GB1295342	NXP B.V.
NL000299DE1	Granted	LATERAL TRENCH MOS GATE COOL-MOS EXTENSIONS	DE	2000-05-20		01943310.1		DE60121331	NXP B.V.
NL000299FR1	Granted	LATERAL TRENCH MOS GATE COOL-MOS EXTENSIONS	FR	2000-05-20		01943310.1		FR1295342	NXP B.V.
NL010060US	Granted	SELF-ALIGNED TRENCH MOS FABRICATION	US	2001-01-23	2002-06-04	10/055350	US20020137291	US6521498	NXP B.V.
NL010060DE09	Granted	SELF-ALIGNED TRENCH MOS FABRICATION	DE	2001-01-23		02734870.5		DE60232855	NXP B.V.
NL010663US	Granted	EDGE TERMINATIONS FOR RESURF TRENCH-GATE MOSFETS	US	2001-09-13	2002-09-06	10/236175	US20030047776	US6936890	NXP B.V.
NL010664US	Granted	EDGE TERMINATION FOR RESURF TRENCH-GATE MOSFETS	US	2001-09-13	2002-09-10	10/238795	US20030047777	US6833583	NXP B.V.
NL010926US	Granted	Combination of a Control Unit and a Logic Application, in which the Combination is Connected to a System Clock	US	2001-12-18	2002-12-12	10/317386	US20030155956	US6861875	NXP B.V.
NL020953CN	Granted	MOSFET WITH TWO-STEPPED BOTTOM FRAME	CN	2002-10-07		03823866.7	CN1689157	CN03823866	NXP B.V.
NL020953US	Granted	MOSFET WITH TWO-STEPPED BOTTOM FRAME	US	2002-10-07	2003-09-18	10/530304	US20070096301	US7312526	NXP B.V.
NL021021US	Granted	FAILSAFE METHOD AND CIRCUIT	US	2002-10-21	2003-09-19	10/531398	US20050285632	US7265574	NXP B.V.
NL021358US1	Granted	INTEGRATED HALF-BRIDGE POWER CIRCUIT.	US	2002-12-10	2003-12-08	10/537575	US20060054967	US7459750	NXP B.V.
NL021416US	Granted	TRENCH MOSFET WITH SIDEWALL GATE	US	2002-12-14	2003-12-08	10/538216	US20060049453	US7262460	NXP B.V.
NL021416FR08	Granted	TRENCH MOSFET WITH SIDEWALL GATE	FR	2002-12-14		03813280.9		FR1573824	NXP B.V.
NL021416DE09	Granted	TRENCH MOSFET WITH SIDEWALL GATE	DE	2002-12-14		03813280.9		DE60340451	NXP B.V.
NL021416GB10	Granted	TRENCH MOSFET WITH SIDEWALL GATE	GB	2002-12-14		03813280.9		GB1573824	NXP B.V.
NL021417US	Granted	THICK TRENCH BOTTOM OXIDE BY OXIDATION OF POLY-SI	US	2002-12-14	2003-12-08	10/538212	US20060017097	US7199010	NXP B.V.
NL021418US	Granted	THICK TRENCH BOTTOM OXIDE BY OXIDISING POROUS Si	US	2002-12-14	2003-12-08	10/538217	US20060024891	US7485534	NXP B.V.
NL030173US1	Granted	PUNCH-THROUGH DIODES; CONTROLLING THE CLAMPING	US	2003-02-18	2004-02-12	10/545622	US20060145191	US7482669	NXP B.V.
NL030173US2	Granted	PUNCH-THROUGH DIODES; CONTROLLING THE CLAMPING	US	2003-02-18	2004-02-12	12/239267	US20090026500	US7728404	NXP B.V.
NL031245CN1	Granted	SWITCH	CN	2003-10-23		200480031154.1	CN1871771	CN200480031154	NXP B.V.
NL031245US1	Granted	SWITCH	US	2003-10-23	2004-10-13	10/577085	US20070080737	US7304526	NXP B.V.
NL031245FR02	Granted	SWITCH	FR	2003-10-23		04770248.5		FR1678828	NXP B.V.
NL031245DE03	Granted	SWITCH	DE	2003-10-23		04770248.5		DE602004037647	NXP B.V.
NL031245GB04	Granted	SWITCH	GB	2003-10-23		04770248.5		GB1678828	NXP B.V.
NL040812CN1	Granted	STACKED DIE PACKAGE (IC ON ESD DEVICE)	CN	2004-07-13		200580023520.3	CN1985370	CN200580023520	NXP B.V.
NL040812US1	Granted	STACKED DIE PACKAGE (IC ON ESD DEVICE)	US	2004-07-13	2005-07-06	11/632511	US20090001607	US8159032	NXP B.V.
US008009US	Granted	SHALLOW TRENCH ISOLATION METHOD FOR FORMING	US		2000-03-06	09/519310		US6544860	NXP B.V.
US008024US	Granted	TRENCH-DIFFUSION CORNER ROUNDING IN A	US		2000-03-07	09/519908		US6326283	NXP B.V.
US008045US	Granted	VOLTAGE STABILIZED LOW LEVEL DRIVER	US		2000-08-17	09/642181		US6433622	NXP B.V.
US008045FR07	Granted	VOLTAGE STABILIZED LOW LEVEL DRIVER	FR	2000-08-17		01958069.5		FR1312166	NXP B.V.
US008045DE08	Granted	VOLTAGE STABILIZED LOW LEVEL DRIVER	DE	2000-08-17		01958069.5		DE60138392	NXP B.V.
US008606US	Granted	VOLTAGE REGULATOR CIRCUIT	US		2000-05-31	09/583325		US6222353	NXP B.V.
US008606USA	Granted	VOLTAGE REGULATOR CIRCUIT	US	2000-05-31	2000-05-31	09/783478	US20010048293	US6380721	NXP B.V.
US010469US	Granted	A SELF-ALIGNED DUAL-OXIDE UMOSFET DEVICE AND A METHOD OF FABRICATING SAME	US		2001-10-01	09/968142	US20030062569	US6551881	NXP B.V.
US030345US2	Granted	DYNAMIC CONTROL OF CAPACITANCE ELEMENTS IN FIELD EFFECT STRUCTURES	US	2003-09-22	2004-09-21	10/572924	US20070080389	US7485916	NXP B.V.
81633417US01	Published	PNEUMATIC WAFER EXPANSION	US		2014-09-05	14/478866	US20160071748		NXP B.V.
81633417WO03	Published	PNEUMATIC WAFER EXPANSION	WO	2014-09-05	2015-09-02	CN2015/088840	WO2016034124		NXP B.V.
81633417TW04	Application	PNEUMATIC WAFER EXPANSION	TW	2014-09-05	2015-09-04	104129366			NXP B.V.
81639954US01	Application	AIR-GUIDED TAPE-AND-REEL SYSTEM AND METHOD	US		2015-06-18	14/743038			NXP B.V.
81639954WO02	Application	AIR-GUIDED TAPE-AND-REEL SYSTEM AND METHOD	WO	2015-06-18	2016-05-12	EP2016/060753			NXP B.V.
81664734EP01	Application	Backend taping using fluid assisted fixation	EP		2015-12-03	15197754.3			NXP B.V.
81680259US01	Instructed	High Precision High Speed Wafer Stage with Mass Compensation	US						NXP B.V.
NL030041US	Granted	CHIP TRANSFER METHOD AND APPARATUS	US	2003-01-16	2003-12-11	10/561397	US20070137031	US7726011	NXP B.V.
NL030041CN	Granted	CHIP TRANSFER METHOD AND APPARATUS	CN	2003-01-16		200380108904.6	CN1739186	CN200380108904	NXP B.V.
NL030041FR09	Granted	CHIP TRANSFER METHOD AND APPARATUS	FR	2003-01-16		03815128.8		FR1588402	NXP B.V.
NL030041DE10	Granted	CHIP TRANSFER METHOD AND APPARATUS	DE	2003-01-16		03815128.8		DE60338308	NXP B.V.
NL030041GB11	Granted	CHIP TRANSFER METHOD AND APPARATUS	GB	2003-01-16		03815128.8		GB1588402	NXP B.V.