# PATENT ASSIGNMENT COVER SHEET

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| **SUBMISSION TYPE:** | NEW ASSIGNMENT |
| **NATURE OF CONVEYANCE:** | ASSIGNMENT |

**CONVEYING PARTY DATA**

| Name | Execution Date |
|---|---|
| NXP USA, INC. | 02/01/2019 |

**RECEIVING PARTY DATA**

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|---|---|
| **Name:** | VLSI TECHNOLOGY LLC |
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| **City:** | WILMINGTON |
| **State/Country:** | DELAWARE |
| **Postal Code:** | 19801 |

**PROPERTY NUMBERS Total: 1**

| Property Type | Number |
|---|---|
| **Patent Number:** | 8312253 |

**CORRESPONDENCE DATA**

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| **ATTORNEY DOCKET NUMBER:** | VLSIP164 |
| **NAME OF SUBMITTER:** | ERIC SCHEUERLEIN |
| **SIGNATURE:** | /Eric Scheuerlein/ |
| **DATE SIGNED:** | 02/20/2019 |

**Total Attachments: 3**
source=20190220_VLSIP164_Patent_Assignment_Agmt_(NXP_US_Inc_to_VLSI_Technology_LLC)2019.02.01#page1.t
source=20190220_VLSIP164_Patent_Assignment_Agmt_(NXP_US_Inc_to_VLSI_Technology_LLC)2019.02.01#page2.t
source=20190220_VLSIP164_Patent_Assignment_Agmt_(NXP_US_Inc_to_VLSI_Technology_LLC)2019.02.01#page3.t

# PATENT ASSIGNMENT AGREEMENT

This Assignment by NXP USA, Inc., f/k/a Freescale Semiconductor, Inc., a corporation duly authorized under the laws of the State of Delaware (hereinafter the "Assignor") is made pursuant to the terms of the Patent Purchase and Cooperation Agreement (the "Initial Agreement"), dated June 30, 2016, among VLSI Technology LLC, NXP B.V., Assignor and SigmaTel LLC (prior to its merger with Assignor), as previously amended by Amendment No. 1 to the Initial Agreement ("Amendment No. 1"), dated December 4, 2017, and as previously amended by Amendment No. 2 to the Initial Agreement ("Amendment No. 2"), dated December 21, 2018. The Patents and Applications assigned hereunder are designated as Assigned Patents under the Agreement.

WITNESSETH:

WHEREAS, Assignor is the owner of certain rights, title and interest in and to the patents and patent applications set forth on Schedule A hereto (hereinafter the "Patents and Applications");

WHEREAS, VLSI Technology LLC, a limited liability company duly organized under and pursuant to the laws of the State of Delaware, (hereinafter the "Assignee"), is desirous of acquiring the entire right, title and interest in and to said Patents and Applications for Letters Patent of the United States or foreign, and in and to any Letters Patent or Patents, United States or foreign, to be obtained there for and thereon;

NOW, THEREFORE, for good and valuable consideration, the receipt and adequacy of which is hereby acknowledged, said Assignor has sold, assigned, transferred and set over, and by these presents does sell, assign, transfer and set over, unto said Assignee, its successors, legal representatives and assigns, Assignor's interest in the entire right, title and interest in and to the above-mentioned Patents and Applications, application for Letters Patent, and any and all Letters Patent or Patents in the United States of America and all foreign countries which may be granted there for and thereon, and in and to any and all divisions, continuations, and continuations-in-part of said application, or reissues or extensions of said Letters Patent or Patents, and all rights under the International Convention for the Protection of Industrial Property, the same to be held and enjoyed by said Assignee, for its own use and behalf and the use and behalf of its successors, legal representatives and assigns, to the full end of the term or terms for which Letters Patent or Patents may be granted, as fully and entirely as the same would have been held and enjoyed by the Assignor, had this sale and assignment not been made. Assignor does hereby sell, assign, transfer, and convey to Assignee, its successors, legal representatives, and assigns all claims for damages and all remedies arising out of any violation of the rights assigned hereby that may have accrued prior to the date of assignment to Assignee, or may accrue hereafter including, but not limited to, the right to sue, recover, collect, and retain damages for past, present, and future infringement of the said Patents and Applications before or after issuance.

**IN TESTIMONY WHEREOF,** 1st day of February, 2019.

NXP USA, INC., F/K/A FREESCALE SEMICONDUCTOR, INC.

By: 

Name: Jennifer Wuamett

Title: President of NXP USA, Inc.

## Schedule A

| Family | Country Code | Application Number | Filed Date | Publication Number | Patent Number | Application Title |
|---|---|---|---|---|---|---|
| MT10266TS | US | 11/461200 | 7/31/2006 | N/A | 7292485 | SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR |
| | TW | 096118282 | 5/23/2007 | N/A | N/A | SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR |
| | PCT | PCT/US2007/068677 | 5/10/2007 | WO2008/016737 | N/A | SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR |
| | CN | 200780028190.6 | 5/10/2007 | 101496107 | 200780028190.6 | SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR |
| | JP | 2009-522905 | 5/10/2007 | 2009-545834 | 5179496 | SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR |
| SC14296EI | US | 12/094123 | 11/17/2005 | 20080256297 | 8219761 | MULTI-PORT HIGH-LEVEL CACHE UNIT AND A METHOD FOR RETRIEVING INFORMATION FROM A MULTI-PORT HIGH-LEVEL CACHE UNIT |
| | PCT | PCT/IB2005/053804 | 11/17/2005 | WO2007/057726 | N/A | MULTI-PORT HIGH-LEVEL CACHE UNIT AND A METHOD FOR RETRIEVING INFORMATION FROM A MULTI-PORT HIGH-LEVEL CACHE UNIT |
| NC10080TC | US | 11/468458 | 8/30/2006 | 20080082873 | 7523373 | MINIMUM MEMORY OPERATING VOLTAGE TECHNIQUE |
| TS48254ZC | US | 12/035961 | 2/22/2008 | 20090217010 | 8312253 | DATA PROCESSOR DEVICE HAVING TRACE CAPABILITIES AND METHOD |
| SIG000284 | US | 11/542,410 | 10/3/2006 | 20080084781 | 7379356 | MEMORY, INTEGRATED CIRCUIT AND METHODS FOR ADJUSTING A SENSE AMP ENABLE SIGNAL USED THEREWITH |
| SC13286EI | US | 10/955,220 | 9/30/2004 | 20060069877 | 7434009 | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |
| | PCT | PCT/IB2005/053109 | 9/21/2005 | WO2006035370 | N/A | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |

| Family | Country Code | Application Number | Filed Date | Publication Number | Patent Number | Application Title |
|---|---|---|---|---|---|---|
| | TW | 094133644 | 9/28/2005 | 200638199 | 1402674 | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |
| | JP | 2007-534139 | 9/21/2005 | 2008-515075 | 4796580 | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |
| | EP | 05798898 | 9/21/2005 | 1805624 | 1805624 | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |
| | DE | 60 2005 051 739.1 | 9/21/2005 | 1805624 | 1805624 | APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS |
| NC10086TC | US | 11/464,124 | 8/11/2006 | 20080037343 | 7668029 | MEMORY HAVING SENSE TIME OF VARIABLE DURATION |
| NM45976HH | US | 13/162,835 | 6/17/2011 | 20120324209 | 8458447 | BRANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR |
| | JP | 2012-135889 | 6/15/2012 | 2013-004101 | 5933360 | BRANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR |
| | CN | 201210201083 | 6/15/2012 | 102841777A | 102841777 | BRANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR |
| NC45169TH | US | 11/733,978 | 4/11/2007 | 20080256339 | 9195462 | TECHNIQUES FOR TRACING PROCESSES IN A MULTI-THREADED PROCESSOR |
| AI20252HH | US | 13/843,090 | 3/15/2013 | 20140281735 | 9304880 | SYSTEM AND METHOD FOR MULTICORE PROCESSING |
| | CN | 201410094015 | 3/14/2014 | 104050066A | 104050066 | SYSTEM AND METHOD FOR MULTICORE PROCESSING |

**Each family transferred will include all family members of any of the patents identified above, in all countries of the world, whether or not all such family members are individually listed above.**