# PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1 Stylesheet Version v1.2 EPAS ID: PAT5384904

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

### **CONVEYING PARTY DATA**

Name	<b>Execution Date</b>
NXP USA, INC.	02/01/2019

## **RECEIVING PARTY DATA**

Name:	VLSI TECHNOLOGY LLC
Street Address:	1209 ORANGE STREET
City:	WILMINGTON
State/Country:	DELAWARE
Postal Code:	19801

### **PROPERTY NUMBERS Total: 1**

Property Type	Number
Patent Number:	7379356

### **CORRESPONDENCE DATA**

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ATTORNEY DOCKET NUMBER:	VLSIP165
NAME OF SUBMITTER:	ERIC SCHEUERLEIN
SIGNATURE:	/Eric Scheuerlein/
DATE SIGNED:	02/20/2019

### **Total Attachments: 3**

PATENT 505338123 REEL: 048389 FRAME: 0064

### PATENT ASSIGNMENT AGREEMENT

This Assignment by NXP USA, Inc., f/k/a Freescale Semiconductor, Inc., a corporation duly authorized under the laws of the State of Delaware (hereinafter the "Assignor") is made pursuant to the terms of the Patent Purchase and Cooperation Agreement (the "Initial Agreement"), dated June 30, 2016, among VLSI Technology LLC, NXP B.V., Assignor and SigmaTel LLC (prior to its merger with Assignor), as previously amended by Amendment No. 1 to the Initial Agreement ("Amendment No. 1"), dated December 4, 2017, and as previously amended by Amendment No. 2 to the Initial Agreement ("Amendment No. 2"), dated December 21, 2018. The Patents and Applications assigned hereunder are designated as Assigned Patents under the Agreement.

### WITNESSETH:

WHEREAS, Assignor is the owner of certain rights, title and interest in and to the patents and patent applications set forth on <u>Schedule A</u> hereto (hereinafter the "Patents and Applications");

WHEREAS, VLSI Technology LLC, a limited liability company duly organized under and pursuant to the laws of the State of Delaware, (hereinafter the "Assignee"), is desirous of acquiring the entire right, title and interest in and to said Patents and Applications for Letters Patent of the United States or foreign, and in and to any Letters Patent or Patents, United States or foreign, to be obtained there for and thereon:

NOW, THEREFORE, for good and valuable consideration, the receipt and adequacy of which is hereby acknowledged, said Assignor has sold, assigned, transferred and set over, and by these presents does sell, assign, transfer and set over, unto said Assignee, its successors, legal representatives and assigns, Assignor's interest in the entire right, title and interest in and to the above-mentioned Patents and Applications, application for Letters Patent, and any and all Letters Patent or Patents in the United States of America and all foreign countries which may be granted there for and thereon, and in and to any and all divisions, continuations, and continuations-in-part of said application, or reissues or extensions of said Letters Patent or Patents, and all rights under the International Convention for the Protection of Industrial Property, the same to be held and enjoyed by said Assignee, for its own use and behalf and the use and behalf of its successors, legal representatives and assigns, to the full end of the term or terms for which Letters Patent or Patents may be granted, as fully and entirely as the same would have been held and enjoyed by the Assignor, had this sale and assignment not been made. Assignor does hereby sell, assign, transfer, and convey to Assignee, its successors, legal representatives, and assigns all claims for damages and all remedies arising out of any violation of the rights assigned hereby that may have accrued prior to the date of assignment to Assignee, or may accrue hereafter including, but not limited to, the right to sue, recover, collect, and retain damages for past, present, and future infringement of the said Patents and Applications before or after issuance.

IN TESTIMONY WHEREOF, 1<sup>st</sup> day of February, 2019.

NXP USA, INC., F/K/A FREESCALE SEMICONDUCTOR, INC.

Name: Jennifer Wuamett

Title: President of NXP USA, Inc.

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# Schedule A

Family	Country	Amplication Number	Filed Date	Publication Number   Patent Number	Patent Number	Anolication Title
MT10266TS	ns	11/461200	7/31/2006	N/A	7292485	SUPPLY AND METHOD THEREFOR
	TW	096118282	5/23/2007	N/A	N/A	SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR
	PCT	PCT/US2007/068677	5/10/2007	WO2008/016737	N/A	SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR
	CS	200780028190.6	5/10/2007	101496107	200780028 90.6	SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR
	ď	2009-522905	5/10/2007	2009-545834	5179496	SRAM HAVING VARIABLE POWER SUPPLY AND METHOD THEREFOR
SC14296EI	Sn	12/094123	11/17/2005	20080256297	8219763	MULTI-PORT HIGH-LEVEL CACHE UNIT AND A METHOD FOR RETRIEVING INFORMATION FROM A MULTI-PORT HIGH-LEVEL CACHE UNIT
	PCT	PCT/IB2005/053804	11/17/2005	WO2007/057726	N/A	MULTI-PORT HIGH-LEVEL CACHE UNIT AND A METHOD FOR RETRIEVING INFORMATION FROM A MULTI-PORT HIGH-LEVEL CACHE UNIT
NC10080TC	sa	11/468458	8/30/2006	20080082873	7523373	MINIMUM MEMORY OPERATING VOLTAGE TECHNIQUE
TS48254ZC	US	12/035961	2/22/2008	20090217010	8312253	DATA PROCESSOR DEVICE HAVING TRACE CAPABILITIES AND METHOD
SIG000284	sn.	11/542,410	10/3/2006	20080084781	7379356	MEMORY, INTEGRATED CIRCUIT AND METHODS FOR ADJUSTING A SENSE AMP ENABLE SIGNAL USED THEREWITH
SC13286EI	SO	10/955,220	9/30/2004	20060069877	7434009	APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS
	PCT	PCT/IB2005/053109	9/21/2005	WO2006035370	A/X	APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS

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2007-534139       9/21/2005       2008-515075         2007-534139       9/21/2005       1805624         60 2005 051 739.1       9/21/2005       1805624         11/464,124       8/11/2006       20080037343         13/162,835       6/17/2011       20120324209         2012-135889       6/15/2012       2013-004101         201210201083       6/15/2012       102841777A         11/733,978       4/11/2007       20080256339	4796580 1805624 1805624 3 7668029 9 8458447	CACHE MODULE USING FETCH BURSTS APPARATUS AND METHOD FOR ROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS APPARATUS AND METHOD FOR PROVIDING INFORMATION TO A CACHE MODULE USING FETCH BURSTS MEMORY HAVING SENSE TIME OF VARIABLE DURATION
9/21/2005 9/21/2005 8/11/2006 6/15/2012 6/15/2012 6/15/2012	1805624 1805624 7668029 8458447	ARATUS AND METHOD FOR VIDING INFORMATION TO A HE MODULE USING FETCH STS ARATUS AND METHOD FOR VIDING INFORMATION TO A HE MODULE USING FETCH STS ACRY HAVING SENSE TIME OF IABLE DURATION
8/11/2006 8/11/2006 6/17/2011 6/15/2012 6/15/2012	1805624 7668029 8458447 5933360	ARATUS AND METHOD FOR VIDING INFORMATION TO A HE MODULE USING FETCH STS  AORY HAVING SENSE TIME OF IABLE DURATION
6/17/2011 6/15/2012 6/15/2012 4/11/2007	8458447 5933360	AORY HAVING SENSE TIME OF TABLE DURATION
6/17/2011 6/15/2012 6/15/2012 4/11/2007	5933360	ATOM TO THE DISTRIBUTE
6/15/2012 6/15/2012 4/11/2007	5933360	BKANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR
6/15/2012	AUUK	BRANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR
4/11/2007	1028417/7	BRANCH TARGET BUFFER ADDRESSING IN A DATA PROCESSOR
· · · · · · · · · · · · · · · · · · ·	9195462	TECHNIQUES FOR TRACING PROCESSES IN A MULTI-THREADED PROCESSOR
13/843,090 3/15/2013 20140281735	9304880	SYSTEM AND METHOD FOR MULTICORE PROCESSING
201410094015 3/14/2014 104050066A	104050366	SYSTEM AND METHOD FOR MULTICORE PROCESSING

Each family transferred will include all family members of any of the patents identified above, in all countries of the world, whether or not all such family members are individually listed above.

**RECORDED: 02/20/2019** 

PATENT REEL: 048389 FRAME: 0067