PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
BITMICRO NETWORKS, INC.	06/30/2017

RECEIVING PARTY DATA

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PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	16056563

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Total Attachments: 8
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RECORDABLE ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, **BiTMICRO Networks, Inc.**, a California company having offices at 47929 Fremont Blvd., Fremont, CA 94538 (***"Assignor"***) and **BiTMICRO LLC**, a Delaware Company having offices at 1620 N. Waccamaw Drive, Suite 109, Murrells Inlet, SC 29576 does hereby sell, assign, transfer, and convey unto (hereafter "***Assignee***") all its right, title, and interest in and to any and all of the following (collectively, the **"*Patent Rights*"**):

(a) the patent applications and patents listed in the table below and any issued patent or patent application that directly or indirectly claims or is amended to claim priority to any of the above, in whole or in part (the "***Patents***");

(b) to the extent not included in Section (a) above, all issued patents, rights to inventions and pending and future applications for patents under U.S. law or regulation or any foreign country with respect to the patentable inventions from which such Patents arise, including without limitation, utility patents, utility models, design patents, invention certificates, provisional, reissues, reexaminations, extensions, continuations, continuations-in-part, continuing prosecution applications, requests for continuing examinations, divisionals, renewals, and registrations in all countries of the world, as well as any patents and patent applications to which any of the Patents or the foregoing directly or indirectly claim priority, in whole or in part;

(c) all related patent filing and prosecution documents;

(d) rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any of the Patents and the inventions, invention disclosures, and discoveries therein;

(e) all inventions and discoveries described in any of the Patents or subject matter capable of being reduced to a patent claim in any of the Patents based on the specification of any of the Patents;

(f) priority rights in any and all patent filings available from and/or through the Patents; and

(g) causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of any of the Patents or of any patent that issues from any of the Patents, including, without limitation, all causes of action and other enforcement rights for (1) damages, (2) injunctive relief, and (3) any other remedies of any kind for past, current and future infringement and all of the proceeds from the foregoing, that are accrued and unpaid or that are hereafter accruing;

(h) rights to collect royalties or other payments under or on account of any of the Patents and/or any of the foregoing categories (a) through (g); and

(i) rights of cooperation assigned or granted by any third party under or on account of any of the Patents and/or any of the foregoing categories (a) through (h).

Assignor represents, warrants and covenants that:

Assignor has the full power and authority, and has obtained all third-party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Fremont, CA on 30 June 2017.

Assignor:

BiTMICRO Networks, Inc.

By: _____

Name: Steven P Ulmer

Title: President & Chief Officer

STATE OF CALIFORNIA)
) ss.
COUNTY OF Alameda)

On June 30th, 2017, before me, DAPINDER BHAGRATH, Notary Public in and for said State, personally appeared STEPHEN P. ULMER, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

Signature _____ (Seal)

DAPINDER BHAGRATH
COMM. #2176448
NOTARY PUBLIC - CALIFORNIA
ALAMEDA COUNTY
My Comm. Exp. Jan. 18, 2021

Group No. 1: PowerGuard and Data Recovery				NVM-only, (Volatile RAM + NVM) Solutions
Group No.	Country	Patent Number	Issue/Priority	Title
1	(A) US	6496939**	2002-12-17/ 1999-09-21	Method and System for Controlling data in a Computer System in the event of a power failure
1	(A) Taiwan	189445	2004-02-20 / 1999-09-21	Method and System for Controlling data in a Computer System
1	(A) Canada	2,388,496	2002-12-17/ 1999-09-21	Method and System for Controlling data in a Computer System
1	(A) EP	App. No: 00961417.3	Filed 2002-04-18 / Priority 1999-09-21	Method and System for Controlling data in a Computer System
1	(B) US	9,372,755	2106-06-21/ 2011-10-05	Adaptive power cycle sequences for data recovery
1	(B) US	App. No. 15/176,156	Filed 2016-06-08 / Priority 2011-10-05	Adaptive power cycle sequences for data recovery
1	US	6,970,890	2005-11-29/ 2000-12-20	Method and apparatus for data recovery

(A & B) Identifies Different Priority Families; All Others Are Single Patents

Group No. 2: Networking+ Flash				Networked-attached Storage Devices (Filesystem / Block IO)
Group No.	Country	Patent Number	Issue/Priority	
2	US	6981070**	2005-12-27/ 2000-07-12 (+552 PTA)	Network storage device having solid-state non-volatile memory
2	US	7,729,370	2010-06-01/ 2005-08-19 (+861 PTA)	Apparatus for networking devices having fibre channel node functionality

Group No. 3: Casings, PCB, and ASIC				SSD/Acceleration Devices/ASIC design
Group No.	Country	Patent Number	Issue/Priority	
3	(C) US	7826243**	2010-11-2 / 2005-12-29 (+747 PTA)	Multiple chip module and package stacking for storage devices
3	(C) US	8093103	2012-1-10 / 2005-12-29	Multiple chip module and package stacking for storage devices
3	(C) Taiwan	I332701B53	2010-11-1 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Korea	10-1391068	2014-4-24 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Japan	5,745,730	2015-04-27 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) Japan	5,859,181	2015-12-08 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(C) China	1013753918	2010-12-28 / 2005-12-29	Multiple Chip Module and Package Stacking Method For Storage Devices
3	(D) US	6317330	2001-11-13 / 2000-2-15	Printed circuit board assembly
3	(D) China	CN 1423917	2006-02-08 / 2000-2-15	Printed circuit board assembly
3	(D) Israel	151278	2007-06-01 / 2000-2-15	Printed circuit board assembly
3	(D) Taiwan	I228211	2005-02-21 / 2000-2-15	Printed circuit board assembly
3	(D) Japan	4,397,143	2009-10-30 / 2000-2-15	Printed circuit board assembly
3	(E) US	9,423,457	2016-8-23 / 2013-3-14 (+102 PTA)	Self-Test Solution For Delay Locked Loops
3	(E) US	App. No. 15/232,801	Filed 2016-08-09 / priority 2013-3-14	Self-Test Solution For Delay Locked Loops
3	(F) US	8665601	2014-3-4 / 2009-9-4 (+500 PTA)	Solid state drive with improved enclosure assembly
3	(F) US	9,552,848	Filed 2014--2-18 / priority 2010-9-4	Solid state drive with improved enclosure assembly

3	(F) US	App. No. 15/414,504	Filed 2017--1-24 / priority 2010-9-4	Solid state drive with improved enclosure assembly
3	US	6,744,635	2004-6-1 / 2000-2-15	Removable Visual Indication Structure For A Printed Circuit Board

(C thru F) Identifies Different Priority Families; All Others Are Single Patents

Group No. 4: DMA and Security				Performance, Hardware Acceleration, Security for NVM and Non-NVM
Group No.	Country	Patent Number	Issue/Priority	
4	US	7716389	2010-05-11 / 2006-03-17	Direct memory access controller with encryption and decryption for non-blocking high bandwidth I/O transactions
4	US	8165301	2012-04-24 / 2006-04-04	Input-output device and storage controller handshake protocol using key exchange for data security
4	US	7620748	2009-11-17 / 2006-04-06	Hardware assisted non-volatile memory-to-input/output direct memory access (DMA) transfer
4	(G) US	9400617	2016-07-26 / 2013-03-15	Hardware-assisted DMA transfer with dependency table configured to permit-in parallel-data drain from cache without processor intervention when filled or drained
4	(G) US	App. No. 15/217,947	Filed 2016-07-22 / Priority 2013-03-15	Hardware-Assisted DMA Transfer with Dependency
4	(G) US	9672178	2017-06-06 / Priority 2013-03-15	Bit-Mapped Dependency Table
4	(G) US	App. No. 15/603,434	Filed 2017-05-23 / Priority 2013-03-15	Bit-Mapped Dependency Table

(G) Identifies A Priority Family; All Others Are Single Patents

Group No. 5: Flash-and-ECC related Patents				SSDs / FlashDevices (Flash, Profile, ECC, Firmware)
Group No.	Country	Patent Number	Issue/Priority	
5	(H) US	9043669++	2015-05-26 / 2012-05-18	Distributed ECC engine for storage media
5	(H) US	App. No. 14/708,246	Filed 2015-05-09 / Priority 2012-05-18	Storage System With Distributed ECC Capability
5	(I) US	8959307++	2015-02-17 / 2007-11-16	Reduced latency memory read transactions in storage devices

S	(I) US	App. No. 14/616,700	Filed 2015-02-02 / Priority 2007-11-16	Memory Transaction With Reduced Latency
S	(I) US	App. No. 14/866,946	Filed 2015-09-26 / Priority 2007-11-16	Reduced latency memory read transactions in storage devices
S	(I) US	App. No. 15/268,533	Filed 2016-09-16/ Priority 2007-11-16	Memory Interface With An Expandable Architecture That Provides Reduced Latency
S	(I) US	App. No. 15/268,536	Filed 2016-09-16/ Priority 2007-11-16	Multi-Dimensional Memory
S	(I) US	App. No. 15/368,598	Filed 2016-12-03 / Priority 2006-11-16	Computer Storage System With Reduced Latency
S	(J) US	7613876++	2009-11-03 / 2006-06-08	HYBRID MULTI-TIERED CACHING STORAGE SYSTEM
S	(J) US	8032700++	2011-10-04 / 2006-06-08	HYBRID MULTI-TIERED CACHING STORAGE SYSTEM
S	(J) Taiwan	I438628	2014-05-21 / 2006-06-08	DATA STORAGE SYSTEM AND DATA STORAGE MEDIUM
S	(J) Taiwan	I525431	Filed 2014-02-17 / 2006-06-08	Data Storage System, Data Structure and Data Storage Method
S	(N) Taiwan	I420307	2013-12-21 / 2006-06-08	Optimized placement policy for solid state storage devices
S	(N) Taiwan	I540430	2016-07-01 / 2005-06-08	Method for data storage
S	(K) US	9430386++	2016-08-30 / 2013-03-15	Multi-leveled cache management in a hybrid storage system
S	(K) US	App. No. 15/249,475	Filed 2016-08-29 / Priority 2013-03-15	Multi-leveled cache management in a hybrid storage system
S	(K) US	App. No. 14/689,045	Filed 2015-04-16/ Priority 2013-03-15	Write Buffering
S	(L) US	6000006	1999-12-07 / 1997-08-25	UNIFIED RE-MAP AND CACHE-INDEX TABLE WITH DUAL WRITE-COUNTERS FOR WEAR-LEVELING OF NON-VOLATILE FLASH RAM MASS STORAGE

S	(L) US	5822251	1998-10-13 / 1997-09-29	Expandable flash-memory mass-storage using shared buddy lines and intermediate flash-bus between device-specific buffers and flash-intelligent DMA controllers
S	(M) US	9099187	2015-08-04 / 2009-09-14	Reducing erase cycles in an electronic storage device that uses at least one erase-limited memory device
S	(M) US	8560804	2013-10-15 / 2009-09-14	Reducing erase cycles in an electronic storage device that uses at least one erase-limited memory device
S	(M) US	9484103	2016-11-1/ 2009-09-14	Electronic Storage Device
S	(M) US	App. No. 15/268,967	Filed 2016-09-19 / priority 2009-09-14	Electronic Storage Device
S	(N) US	8010740	2011-08-30/ 2008-11-25	Optimizing memory operations in an electronic storage device
S	(N) US	7506098	2009-03-17 / 2006-06-08	Optimized placement policy for solid state storage devices
S	(O) US	8447908	2013-04-21 / 2009-09-07	Multilevel memory bus system for solid-state mass storage
S	(O) US	8788725	2014-7-22 / 2009-09-07	Multilevel memory bus system for solid-state mass storage
S	(O) US	App. No. 14/297,628	2014-06-06 / 2009-09-07	Multilevel memory bus system
S	US	6529416	2003-03-04 / 2000-11-30	Parallel erase operations in memory systems
S	US	5956743	1999-09-21 / 1997-09-29	TRANSPARENT MANAGEMENT AT HOST INTERFACE OF FLASH-MEMORY OVERHEAD-BYTES USING FLASH-SPECIFIC DMA HAVING PROGRAMMABLE PROCESSOR-INTERRUPT OF HIGH-LEVEL OPERATIONS
S	US	9135190	2015-09-15 / 2009-09-04	Multi-profile memory controller for computing devices
S	US	6757845	2004-06-29 / 2000-11-30	Method and apparatus for testing a storage device
S	US	Appl. No. 15/482,684	Filed 2017-04-07	Multi-Dimensional Computer Storage System Note: this application was decided to be filed without any priority claim; option available for this application to be a continuation application that claims benefit to 15/268,536 and/or 15/268,533 (family (I))

(H thru O) Identifies Different Priority Families; All Others Are Single Patents