PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5547280

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
ACORN SEMI LLC	05/02/2019

RECEIVING PARTY DATA

Name:	THE PETER NORTON LIVING TRUST DATED APRIL 28, 1989,
Street Address:	7 TIMES SQUARE
Internal Address:	O'MELVENY & MYERS C/O T. BOGGS / V. FERRITO
City:	NEW YORK
State/Country:	NEW YORK
Postal Code:	10036

PROPERTY NUMBERS Total: 56

Property Type	Number
Patent Number:	6198113
Patent Number:	7615402
Patent Number:	7084423
Patent Number:	7462860
Patent Number:	7884003
Patent Number:	10090395
Patent Number:	10186592
Patent Number:	8431469
Patent Number:	9425277
Patent Number:	8766336
Patent Number:	9209261
Patent Number:	9905691
Patent Number:	9461167
Patent Number:	9812542
Patent Number:	7176483
Patent Number:	6833556
Patent Number:	7112478
Patent Number:	7883980
Patent Number:	8377767

Property Type	Number
Patent Number:	8916437
Patent Number:	9583614
Patent Number:	6891234
Patent Number:	7382021
Patent Number:	7902029
Patent Number:	8263467
Patent Number:	7816240
Patent Number:	8658523
Patent Number:	8263466
Patent Number:	8212336
Patent Number:	9362376
Patent Number:	9755038
Patent Number:	9484426
Patent Number:	8731017
Patent Number:	9036672
Patent Number:	9270083
Patent Number:	10008827
Patent Number:	10193307
Patent Number:	8395213
Patent Number:	9406798
Patent Number:	9673327
Patent Number:	10084091
Patent Number:	10147798
Patent Number:	9620611
Patent Number:	10170627
Patent Number:	8450133
Patent Number:	9029686
Application Number:	15728002
Application Number:	15418360
Application Number:	15684707
Application Number:	16213876
Application Number:	16105277
Application Number:	16175637
Application Number:	15655710
Application Number:	16283578
Application Number:	16202507
Application Number:	15877273

CORRESPONDENCE DATA

Fax Number: (949)823-6994

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 949-760-9600
Email: IPNB@omm.com
Correspondent Name: O'MELVENY & MYERS LLP / A. VIDAURRI
Address Line 1: 400 S HOPE ST
Address Line 2: 18TH FLOOR
Address Line 4: LOS ANGELES, CALIFORNIA 90071

ATTORNEY DOCKET NUMBER:	628,184-001
NAME OF SUBMITTER:	ADRIAN A. VIDAURRI
SIGNATURE:	/Adrian A Vidaurri/
DATE SIGNED:	05/30/2019

Total Attachments: 14
source=Acorn - Patent Security Agreement (Executed)#page1.tif
source=Acorn - Patent Security Agreement (Executed)#page2.tif
source=Acorn - Patent Security Agreement (Executed)#page3.tif
source=Acorn - Patent Security Agreement (Executed)#page4.tif
source=Acorn - Patent Security Agreement (Executed)#page5.tif
source=Acorn - Patent Security Agreement (Executed)#page6.tif
source=Acorn - Patent Security Agreement (Executed)#page7.tif
source=Acorn - Patent Security Agreement (Executed)#page8.tif
source=Acorn - Patent Security Agreement (Executed)#page9.tif
source=Acorn - Patent Security Agreement (Executed)#page10.tif
source=Acorn - Patent Security Agreement (Executed)#page11.tif
source=Acorn - Patent Security Agreement (Executed)#page12.tif
source=Acorn - Patent Security Agreement (Executed)#page13.tif
source=Acorn - Patent Security Agreement (Executed)#page14.tif

ACORN SEMI LLC
PATENT SECURITY AGREEMENT

THIS PATENT SECURITY AGREEMENT ("***Patent Security Agreement***"), made as of May 2nd, 2019, is by and between ACORN SEMI LLC, a Delaware limited liability company ("***Grantor***"), on the one hand, and The Peter Norton Living Trust Dated April 28, 1989, a California trust (the "**Secured Party**").

WHEREAS, the parties have entered into a Security Agreement dated as of the date hereof, whereby Grantor granted a security interest in certain property to Secured Party including a security interest in the Patents, Patent Applications and other patent rights and rights pertaining thereto as identified below.

NOW, THEREFORE, in confirmation of the terms of the Security Agreement and in consideration of the premises set forth herein and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, Grantor and Secured Party agree as follows:

1. Incorporation of Security Agreement. The Security Agreement and the provisions thereof are hereby incorporated herein in their entirety. Capitalized terms used but not defined herein shall have the respective meanings given in the Security Agreement.

2. Grant and Confirmation of Grant of Security Interest. To secure the complete and timely satisfaction of the terms of the Security Agreement, Grantor hereby grants to Secured Party, and hereby confirms the prior grant in the Security Agreement of, a continuing security interest in Grantor's entire right, title and interest in and to the United States Patents and patent applications listed in Schedule A, as may be amended from time to time, including without limitation: (i) all reissues, divisionals, continuations, continuations-in-part, extensions, renewals, and reexaminations thereof and any Patents resulting therefrom, (ii) the inventions and improvements described or claimed therein and all rights pertaining thereto, (iii) the right to sue or otherwise recover for any past, present and future infringement or other violation thereof, (iv) all Patent Licenses relating to and all Proceeds of the foregoing, including, without limitation, license fees, royalties, income, payments, claims, damages, and proceeds of any suit now or hereafter due and/or payable with respect thereto, and (v) all other rights of any kind accruing thereunder including the right to make, use, practice, sell or offer for sale, import or otherwise license, transfer or dispose of the Patents or inventions and improvements disclosed or claimed therein.

3. New Patents. Secured Party is authorized to use this Patent Security Agreement for the purpose of perfecting a security interest in any after acquired Patents or patent applications filed after the date of this Patent Security Agreement that are within the scope of the security interest granted in the Security Agreement, including any Patents or patent applications for improvements or modifications of or substitutions for the Patents and Patent applications listed in Schedule A and the inventions and improvements described or claimed therein as well as for the purpose of perfecting a security interest in any Patents or patent applications that were inadvertently omitted from Schedule A. The provisions of this Patent Security Agreement and

the Security Agreement shall apply in full to all New Patents.

4. Term. The term of the security interest granted herein shall extend until the Security Agreement has been terminated in accordance with its terms.

5. Effect on Other Agreements: Cumulative Remedies. At any time an event of default exists or has occurred and is continuing under the terms of the Security Agreement or this Patent Security Agreement, Secured Party shall have all rights and remedies provided in this Security Agreement, any other related documents, the UCC and other applicable law, all of which rights and remedies may be exercised without notice to or consent by Grantor, except as such notice or consent is expressly provided for hereunder or in the Security Agreement or related documents or as required by applicable law. Grantor acknowledges and agrees that this Patent Security Agreement is not intended to limit or restrict in any way the rights and remedies of Secured Party under the Security Agreement but rather is intended to supplement and facilitate the exercise of such rights and remedies. All of the rights and remedies of Secured Party with respect to the Patents, whether established hereby, by the Security Agreement, by any other agreements, or by law, shall be cumulative and may be exercised singularly or concurrently.

6. Binding Effect and Benefits. This Patent Security Agreement shall be binding upon Grantor and its successors and assigns, and shall inure to the benefit of Secured Party and its successors and assigns.

7. APPLICABLE LAW; SEVERABILITY. THIS SECURITY AGREEMENT SHALL BE CONSTRUED IN ALL RESPECTS IN ACCORDANCE WITH, AND GOVERNED BY, ALL OF THE PROVISIONS OF THE NEW YORK UNIFORM COMMERCIAL CODE AND BY THE OTHER INTERNAL LAWS (AS OPPOSED TO CONFLICT OF LAWS PROVISIONS) OF THE STATE OF NEW YORK. WHENEVER POSSIBLE, EACH PROVISION OF THIS PATENT SECURITY AGREEMENT SHALL BE INTERPRETED IN SUCH A MANNER AS TO BE EFFECTIVE AND VALID UNDER APPLICABLE LAW, BUT IF ANY PROVISION OF THIS PATENT SECURITY AGREEMENT SHALL BE PROHIBITED BY OR INVALID UNDER APPLICABLE LAW, SUCH PROVISION SHALL BE INEFFECTIVE ONLY TO THE EXTENT OF SUCH PROHIBITION OR INVALIDITY, WITHOUT INVALIDATING THE REMAINDER OF SUCH PROVISIONS OR THE REMAINING PROVISIONS OF THIS PATENT SECURITY AGREEMENT.

[Signature page follows]

IN WITNESS WHEREOF, the parties have executed and delivered this Patent Security Agreement as of the date first written above.

GRANTOR:

ACORN SEMI LLC

By:_____
Name: Tom Horgan
Title: President

SECURED PARTY:

THE PETER NORTON LIVING TRUST
DATED APRIL 28, 1989

By:_____
Name: Peter Norton
Title: Trustee

IN WITNESS WHEREOF, the parties have executed and delivered this Patent Security Agreement as of the date first written above.

GRANTOR:

ACORN SEMI LLC

By:_____
Name: Tom Horgan
Title: President

SECURED PARTY:

THE PETER NORTON LIVING TRUST
DATED APRIL 28, 1989

By: DocuSigned by: Peter Norton
20370AB2B0B8415...
Name: Peter Norton
Title: Trustee

SCHEDULE A

PATENTS

Patent Description	Registration No.	Issue Date
ELECTROSTATICALLY OPERATED TUNNELING TRANSISTOR	6,198,113	06-Mar-2001
ELECTROSTATICALLY OPERATED TUNNELING TRANSISTOR	7,615,402	10-Nov-2009
ELECTROSTATICALLY CONTROLLED TUNNELING TRANSISTOR	DE60034328.6	11-Apr-2007
ELECTROSTATICALLY CONTROLLED TUNNELING TRANSISTOR	EP1173896	11-Apr-2007
ELECTROSTATICALLY CONTROLLED TUNNELING TRANSISTOR	GB1173896	11-Apr-2007
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	7,084,423	01-Aug-2006
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	7,462,860	09-Dec-2008
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	CN100530682	19-Aug-2009
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	7,884,003	08-Feb-2011
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	10,090,395	02-Oct-2018
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	10,186,592	22-Jan-2019

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	8,431,469	30-Apr-2013
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,425,277	23-Aug-2016
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	8,766,336	01-Jul-2014
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,209,261	08-Dec-2015
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,905,691	27-Feb-2018
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,461,167	04-Oct-2016
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	9,812,542	07-Nov-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	DE60350090.0	05-Apr-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	EP1543561	05-Apr-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	GB1543561	05-Apr-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	IE1543561	05-Apr-2017

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	JP4847699	21-Oct-2011
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	KR10-1025378	21-Mar-2011
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	NL1543561	05-Apr-2017
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	TW I327376	11-Jul-2010
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	7,176,483	13-Feb-2007
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING	TW I286343	01-Sep-2007
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	6,833,556	21-Dec-2004
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	CN100557816	04-Nov-2009
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	7,112,478	26-Sep-2006
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	7,883,980	08-Feb-2011
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	8,377,767	19-Feb-2013

INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	8,916,437	23-Dec-2014
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	9,583,614	28-Feb-2017
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	JP4713884	01-Apr-2011
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	KR10-1018103	21-Feb-2011
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	TW I310608	01-Jun-2009
TRANSISTOR WITH WORKFUNCTION-INDUCED CHARGE LAYER	6,891,234	10-May-2005
TRANSISTOR WITH WORKFUNCTION-INDUCED CHARGE LAYER	DE602004046314.0	10-Dec-2014
TRANSISTOR WITH WORKFUNCTION-INDUCED CHARGE LAYER	EP1709689	10-Dec-2014
INSULATED GATE FIELD-EFFECT TRANSISTOR HAVING III-VI SOURCE/DRAIN LAYER(S)	7,382,021	03-Jun-2008
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	7,902,029	08-Mar-2011
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	8,263,467	11-Sep-2012

PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	DE602005030278.6	28-Sep-2011
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	EP1787320	28-Sep-2011
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	FR1787320	28-Sep-2011
PROCESS FOR FABRICATING A SELF-ALIGNED DEPOSITED SOURCE/DRAIN INSULATED GATE FIELD-EFFECT TRANSISTOR	GB1787320	28-Sep-2011
METHOD FOR MAKING SEMICONDUCTOR INSULATED-GATE FIELD-EFFECT TRANSISTOR HAVING MULTILAYER DEPOSITED METAL SOURCE(S) AND/OR DRAIN(S)	7,816,240	19-Oct-2010
METHOD FOR MAKING SEMICONDUCTOR INSULATED-GATE FIELD-EFFECT TRANSISTOR HAVING MULTILAYER DEPOSITED METAL SOURCE(S) AND/OR DRAIN(S)	8,658,523	25-Feb-2014
CHANNEL STRAIN INDUCED BY STRAINED METAL IN FET SOURCE OR DRAIN	8,263,466	11-Sep-2012
FIELD EFFECT TRANSISTOR SOURCE OR DRAIN WITH A MULTI-FACET SURFACE	8,212,336	03-Jul-2012
METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	9,362,376	07-Jun-2016
METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	9,755,038	05-Sep-2017
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	CN104170058	08-Aug-2017

METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	9,484,426	01-Nov-2016
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	GB2526951	20-Apr-2016
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	GB2526950	29-Apr-2016
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	KR10-1898027	06-Sep-2018
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	GB2511245	20-Jan-2016
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	8,731,017	20-May-2014
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	9,036,672	19-May-2015
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	9,270,083	23-Feb-2016
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	10,008,827	26-Jun-2018
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	10,193,307	29-Jan-2019
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	CN102957091	17-Jun-2015

TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	CN105047735	12-Apr-2017
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	FR2979037	07-Dec-2018
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	KR1374485	07-Mar-2014
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	8,395,213	12-Mar-2013
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	9,406,798	02-Aug-2016
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	9,673,327	06-Jun-2017
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	10,084,091	25-Sep-2018
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	DE112011102840	18-Feb-2016
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	KR10-1476066	17-Dec-2014
MIS CONTACT STRUCTURE WITH METAL OXIDE CONDUCTOR	10,147,798	04-Dec-2018
MIS CONTACT STRUCTURE WITH METAL OXIDE CONDUCTOR	9,620,611	11-Apr-2017

NANOWIRE TRANSISTOR WITH SOURCE AND DRAIN INDUCED BY ELECTRICAL CONTACTS WITH NEGATIVE SCHOTTKY BARRIER HEIGHT	10,170,627	01-Jan-2019
STRAINED-ENHANCED SILICON PHOTON-TO-ELECTRON CONVERSION DEVICES	8,450,133	28-May-2013
STRAINED-ENHANCED SILICON PHOTON-TO-ELECTRON CONVERSION DEVICES	9,029,686	12-May-2015

PATENT APPLICATIONS

Application Description	Application No.	Application Date
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	EP16156295.4	08-Aug-2003
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	EP16154220.4	08-Aug-2003
METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS	15/728,002	09-Oct-2017
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	15/418,360	27-Jan-2017
INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL	EP3785158.1	08-Aug-2003
METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	15/684,707	23-Aug-2017
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	CN201710569473.7	13-Jul-2017

IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	DE112012004882.2	18-Oct-2012
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	KR10-2014-7017274	18-Oct-2012
IMPROVING METAL CONTACTS TO GROUP IV SEMICONDUCTORS BY INSERTING INTERFACIAL ATOMIC MONOLAYERS	TW102116259	07-May-2013
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	16/213,876	07-Dec-2018
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	DE102012025727.9	02-Aug-2012
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	DE102012015309.0	02-Aug-2012
TENSILE STRAINED SEMICONDUCTOR PHOTON EMISSION AND DETECTION DEVICES AND INTEGRATED PHOTONICS SYSTEM	FR18 59821	24-Oct-2018
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	16/105,277	20-Aug-2018
STRAINED SEMICONDUCTOR USING ELASTIC EDGE RELAXATION OF A STRESSOR COMBINED WITH BURIED INSULATING LAYER	DE112011106092.0	25-Aug-2011
MIS CONTACT STRUCTURE WITH METAL OXIDE CONDUCTOR	16/175,637	30-Oct-2018
SOI WAFERS AND DEVICES WITH BURIED STRESSOR	15/655,710	20-Jul-2017
SOI WAFERS AND DEVICES WITH BURIED STRESSOR	16/283,578	22-Feb-2019
NANOWIRE TRANSISTOR WITH SOURCE AND DRAIN INDUCED BY ELECTRICAL CONTACTS WITH NEGATIVE SCHOTTKY BARRIER HEIGHT	16/202,507	28-Nov-2018
NANOWIRE TRANSISTOR WITH SOURCE AND DRAIN INDUCED BY ELECTRICAL CONTACTS WITH NEGATIVE SCHOTTKY BARRIER HEIGHT	PCT/US2017/062296	17-Nov-2017

STRAINED-ENHANCED SILICON PHOTON-TO-ELECTRON CONVERSION DEVICES	DE112010002206.2	02-Mar-2010
STRAINED SEMICONDUCTOR-ON-INSULATOR BY DEFORMATION OF BURIED INSULATOR INDUCED BY BURIED STRESSOR	15/877,273	22-Jan-2018
STRAINED SEMICONDUCTOR-ON-INSULATOR BY DEFORMATION OF BURIED INSULATOR INDUCED BY BURIED STRESSOR	PCT/US2018/014740	22-Jan-2018