

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT5567208

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY INTEREST
CONVEYING PARTY DATA	
Name	Execution Date
VISHAY DALE ELECTRONICS, INC.	06/05/2019
DALE ELECTRONICS, INC.	06/05/2019
VISHAY DALE ELECTRONICS, LLC	06/05/2019
VISHAY-DALE, INC.	06/05/2019
VISHAY INTERTECHNOLOGY, INC.	06/05/2019
SILICONIX INCORPORATED	06/05/2019
VISHAY-SILICONIX, INC.	06/05/2019
VISHAY-SILICONIX	06/05/2019
VISHAY SPRAGUE, INC.	06/05/2019
VISHAY EFI, INC.	06/05/2019
SPRAGUE ELECTRIC COMPANY	06/05/2019
VISHAY GENERAL SEMICONDUCTOR, INC.	06/05/2019
RECEIVING PARTY DATA	
Name:	JPMORGAN CHASE BANK, N.A., AS ADMINISTRATIVE AGENT
Street Address:	IL1-1145/54/63, P.O. BOX 6026
City:	CHICAGO
State/Country:	ILLINOIS
Postal Code:	60603-6026
PROPERTY NUMBERS Total: 327	
Property Type	Number
Patent Number:	6946944
Patent Number:	7034645
Patent Number:	7221249
Patent Number:	7263761
Patent Number:	7345562
Patent Number:	7921546
Patent Number:	7986207
Patent Number:	6401329
Patent Number:	6441718

Property Type	Number
Patent Number:	6725529
Patent Number:	6901655
Patent Number:	6510605
Patent Number:	7170389
Patent Number:	7038572
Patent Number:	7102484
Patent Number:	6925704
Patent Number:	7042328
Patent Number:	7190252
Patent Number:	8018310
Patent Number:	8242878
Patent Number:	8248202
Patent Number:	8198977
Patent Number:	8344843
Patent Number:	8581687
Patent Number:	8378772
Patent Number:	8525637
Patent Number:	9001512
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Patent Number:	8319598
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Patent Number:	8878643
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Patent Number:	D758970
Patent Number:	8823483
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Patent Number:	9400294
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Patent Number:	10147524
Patent Number:	9865532
Patent Number:	9502171

Property Type	Number
Patent Number:	10217550
Patent Number:	6873028
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Patent Number:	7154370
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Patent Number:	6621142
Patent Number:	6621143
Patent Number:	6271060
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Patent Number:	6562647
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Patent Number:	7416947
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Patent Number:	7326995
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Patent Number:	7268032
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Patent Number:	7012005
Patent Number:	7009247

Property Type	Number
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Patent Number:	6764906
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Property Type	Number
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Patent Number:	9831336
Patent Number:	9887259
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Patent Number:	10229988
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Patent Number:	6159817
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Application Number:	13600770
Application Number:	13720618
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Application Number:	09591179
Application Number:	10378766
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Property Type	Number
Application Number:	15634739
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Application Number:	16002413
Application Number:	16019282
Application Number:	16262598
Application Number:	16291996
Application Number:	12759769
Application Number:	12107349
Application Number:	12189492
Application Number:	12052251
Application Number:	15906698

CORRESPONDENCE DATA

Fax Number: (800)494-7512

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 202-370-4756

Email: ipteam@cogencyglobal.com

Correspondent Name: JAY DASILVA

Address Line 1: 1025 VERMONT AVE NW, SUITE 1130

Address Line 2: COGENCY GLOBAL INC.

Address Line 4: WASHINGTON, D.C. 20005

ATTORNEY DOCKET NUMBER: 1093893 PT

NAME OF SUBMITTER: ELIZABETH WAGENBACH

SIGNATURE: /Elizabeth Wagenbach/

DATE SIGNED: 06/12/2019

Total Attachments: 67

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PATENT SECURITY AGREEMENT dated as of June 5, 2019 (this "Agreement"), among Vishay Intertechnology, Inc. (the "Borrower"), the other Subsidiary Loan Parties which are signatories hereto (each, a "Grantor") and JPMorgan Chase Bank, N.A. ("JPMCB"), as Administrative Agent.

Reference is made to (a) the Credit Agreement dated as of June 5, 2019, (as amended, restated, supplemented or otherwise modified from time to time, the "Credit Agreement"), among the Borrower, the Lenders from time to time party thereto and JPMCB, as Administrative Agent, and (b) the Guarantee and Collateral Agreement dated as of June 5, 2019 (as amended, restated, supplemented or otherwise modified from time to time, the "Collateral Agreement"), among the Borrower, the other Subsidiary Loan Parties from time to time party thereto and JPMCB, as Administrative Agent. The Lenders and the Issuing Banks have agreed to extend credit to the Borrower subject to the terms and conditions set forth in the Credit Agreement. The obligations of the Lenders and the Issuing Banks to extend such credit are conditioned upon, among other things, the execution and delivery of this Agreement. The Grantors party hereto (other than the Borrower) are Affiliates of the Borrower, will derive substantial benefits from the extension of credit to the Borrower pursuant to the Credit Agreement and are willing to execute and deliver this Agreement in order to induce the Lenders and the Issuing Banks to extend such credit. Accordingly, the parties hereto agree as follows:

SECTION 1. Terms. Each capitalized term used but not otherwise defined herein shall have the meaning specified in the Credit Agreement or the Collateral Agreement, as applicable. The rules of construction specified in Section 1.03 of the Credit Agreement also apply to this Agreement, *mutatis mutandis*.

SECTION 2. Grant of Security Interest. As security for the payment or performance, as the case may be, in full of the Secured Obligations, each Grantor pursuant to the Collateral Agreement did, and hereby does, grant to the Administrative Agent, its successors and assigns, for the benefit of the Secured Parties, a security interest in all right, title and interest in, to and under any and all of the following assets now owned or at any time hereafter acquired by such Grantor or in, to or under which such Grantor now has or at any time hereafter may acquire any right, title or interest (collectively, the "Patent Collateral"):

(a) all letters patent of the United States of America, all registrations and recordings thereof, and all applications for letters patent of the United States of America, including registrations, recordings and pending applications in the United States Patent and Trademark Office, including those listed on Schedule I; and

(b) all reissues, continuations, divisionals, continuations-in-part, renewals or extensions thereof, and the inventions disclosed or claimed therein, including the right to make, have made, use, sell, offer to sell, import or export the inventions disclosed or claimed therein.

SECTION 3. Collateral Agreement. The security interests granted to the Administrative Agent herein are granted in furtherance, and not in limitation of, the security interests granted to the Administrative Agent pursuant to the Collateral Agreement. Each Grantor hereby acknowledges and affirms that the rights and remedies of the Administrative Agent with respect to the Patent Collateral are more fully set forth in the Collateral Agreement, the terms and provisions of which are hereby incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Agreement and the Collateral Agreement, the terms of the Collateral Agreement shall govern.

SECTION 4. Recordation. Each Grantor hereby authorizes and requests that the Commissioner of Patents and Trademarks record this Agreement.

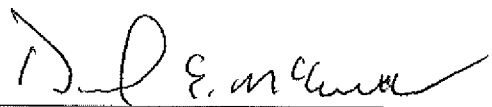
SECTION 5. Counterparts. This Agreement may be executed in counterparts (and by different parties hereto on different counterparts), each of which shall constitute an original, but all of which when taken together shall constitute a single contract. Delivery of an executed counterpart of a signature page of this Agreement by facsimile or other electronic imaging shall be effective as delivery of a manually executed counterpart of this Agreement.

SECTION 6. GOVERNING LAW. THIS AGREEMENT SHALL BE GOVERNED BY, AND CONSTRUED IN ACCORDANCE WITH, THE LAWS OF THE STATE OF NEW YORK.


[Signature Pages Follow]

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement
as of the day and year first above written.

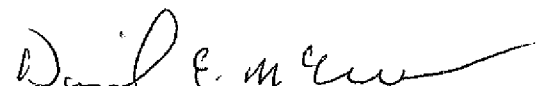
VISHAY INTERTECHNOLOGY, INC.,

By 
Name: David E. McConnell
Title: Senior Vice President and Corporate
Treasurer

VISHAY GSI, INC.
SILICONIX INCORPORATED
VISHAY SPRAGUE, INC.
VISHAY BCCOMPONENTS HOLDINGS LTD.
VISHAY AMERICAS, INC.
VISHAY HIREL SYSTEMS LLC
VISHAY SILICONIX, LLC

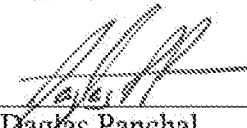
By 
Name: David E. McConnell
Title: Treasurer

VISHAY DALE ELECTRONICS, LLC

By 
Name: David E. McConnell
Title: Manager

JPMORGAN CHASE BANK, N.A., as
Administrative Agent,

by



Name: Douglas Panchal
Title: Executive Director

[Signature Page to Patent Security Agreement]

[[S202038]]

PATENT
REEL: 049440 FRAME: 0891

SCHEDULE I

United States Patents and Patent Applications

Vishay Dale Electronics, LLC

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (<u>Patent Description</u>)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
1.	UTL	10/244,777	6,946,944	INDUCTOR COIL AND METHOD FOR MAKING SAME	ISSUED	9/16/2002	9/20/2005	Vishay Dale Electronics, Inc.
2.	UTL	11/038,880	7,034,645	INDUCTOR COIL AND METHOD FOR MAKING SAME	ISSUED	1/20/2005	4/25/2006	Vishay Dale Electronics, Inc.
3.	UTL	11/409,651	7,221,249	INDUCTOR COIL	ISSUED	4/24/2006	5/22/2007	Vishay Dale Electronics, Inc.
4.	UTL	11/609,165	7,263,761	METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR	ISSUED	12/11/2006	9/4 /2007	Vishay Dale Electronics, Inc.
5.	UTL	11/782,020	7,345,562	METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR	ISSUED	7/24/2007	3/18/2008	Vishay Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (<u>Patent Description</u>)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
6.	UTL	12/013,725	7,921,546	METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR	ISSUED	1/1/14/200 8	4/12/2011	Vishay Dale Electronics, Inc.
7.	UTL	12/535,757	7,986,207	METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR	ISSUED	8/5/2009	7/26/2011	Vishay Dale Electronics, Inc.
8.	UTL	09/471,622	6,401,329	METHOD FOR MAKING OVERLAY SURFACE MOUNT RESISTOR	ISSUED	12/21/1999	6/11/2002	Vishay Dale Electronics, Inc.
9.	UTL	09/715,252	6,441,718	OVERLAY SURFACE MOUNT RESISTOR	ISSUED	11/17/2000	8/27/2002	Vishay Dale Electronics, Inc.
10.	UTL	10/078,311	6,725,529	METHOD FOR MAKING OVERLAY SURFACE MOUNT RESISTOR	ISSUED	2/18/2002	4/27/2004	Vishay Dale Electronics, Inc.
11.	UTL	10/797,866	6,901,655	METHOD FOR MAKING OVERLAY SURFACE MOUNT RESISTOR	ISSUED	3/10/2004	6/7 /2005	Vishay Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
12.	UTL	09/471,617	6,510,605	METHOD FOR MAKING FORMED SURFACE MOUNT RESISTOR	ISSUED	12/21/1999	1/28/2003	Vishay Dale Electronics, Inc.
13.	UTL	10/079,010	7,170,389	APPARATUS FOR TANTALUM PENTOXIDE MOISTURE BARRIER IN FILM RESISTORS	ISSUED	2/19/2002	1/30/2007	Vishay Dale Electronics, Inc.
14.	UTL	09/811,844	7,038,572	POWER CHIP RESISTOR	ISSUED	3/19/2001	5/2/2006	Vishay Dale Electronics, Inc.
15.	UTL	10/441,649	7,102,484	HIGH POWER RESISTOR HAVING AN IMPROVED OPERATING TEMPERATURE RANGE AND METHOD OF MAKING SAME	ISSUED	5/20/2003	9/5/2006	Vishay Dale Electronics, Inc.
16.	UTL	10/744,846	6,925,704	METHOD FOR MAKING HIGH POWER RESISTOR HAVING IMPROVED OPERATING TEMPERATURE RANGE	ISSUED	12/23/2003	8/9/2005	Vishay Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
17.	UTL	11/123,508	7,042,328	HIGH POWER RESISTOR HAVING AN IMPROVED OPERATING TEMPERATURE RANGE	ISSUED	5/5/2005	5/9/2006	Vishay Dale Electronics, Inc.
18.	UTL	11/066,865	7,190,252	SURFACE MOUNT ELECTRICAL RESISTOR WITH THERMALLY CONDUCTIVE, ELECTRICALLY INSULATIVE FILLER AND METHOD FOR USING SAME	ISSUED	2/25/2005	3/13/2007	Vishay Dale Electronics, Inc.
19.	UTL	11/535,758	8,018,310	INDUCTOR WITH THERMALLY STABLE RESISTANCE	ISSUED	9/27/2006	9/13/2011	Vishay Dale Electronics, Inc.
20.	UTL	12/026,939		RESISTOR AND METHOD FOR MAKING SAME	ISSUED	2/6/2008	3/22/2011	Vishay Dale Electronics, Inc.
21.	UTL	12/205,197	8,242,878	RESISTOR AND METHOD FOR MAKING SAME	ISSUED	9/5/2008	8/14/2012	Vishay Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
22.	UTL	12/536,792	8,248,202	METAL STRIP RESISTOR FOR MITIGATING EFFECTS OF THERMAL EMF	ISSUED	8/6/2009	8/21/2012	Vishay Dale Electronics, Inc.
23.	UTL	12/874,514	8,198,977	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION	ISSUED	9/2/2010	6/12/2012	Vishay Dale Electronics, Inc.
24.	UTL	13/051,585	8,344,843	RESISTOR AND METHOD FOR MAKING SAME	ISSUED	3/18/2011	1/1/2013	Vishay Dale Electronics, Inc.
25.	UTL	13/127,838	8,581,687	FOUR-TERMINAL RESISTOR WITH FOUR RESISTORS AND ADJUSTABLE TEMPERATURE COEFFICIENT OF RESISTANCE	ISSUED	5/5/2011	11/12/2013	Dale Electronics, Inc.
26.	UTL	13/109,576		METHOD FOR MAKING A HIGH CURRENT LOW PROFILE INDUCTOR	PENDING	5/17/2011		Vishay Dale Electronics, Inc.
27.	UTL	13/198,274	8,378,772	INDUCTOR WITH THERMALLY STABLE RESISTANCE	ISSUED	8/4/2011	2/19/2013	Vishay Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
28.	UTL	13/213,877		HIGH POWERED INDUCTORS USING A MAGNETIC BIAS	PENDING	8/19/2011		Vishay Dale Electronics, Inc.
29.	UTL	13/493,402	8,525,637	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION	ISSUED	6/11/2012	9/3/2013	Vishay Dale Electronics, Inc.
30.	UTL	13/462,958	9,001,512	HEAT SPREADER FOR ELECTRICAL COMPONENTS	ISSUED	5/3/2012	4/7/2015	Vishay Dale Electronics, LLC
31.	UTL	13/600,770		HIGHLY COUPLED INDUCTOR	PENDING	8/31/2012		Vishay Dale Electronics, Inc.
32.	UTL	13/569,721	8,686,828	RESISTOR AND METHOD FOR MAKING SAME	ISSUED	8/8/2012	4/1/2014	Dale Electronics, Inc.
33.	UTL	12,950,177	8,319,598	POWER RESISTOR	ISSUED	11/19/2010	11/27/2012	Vishay Dale Electronics, Inc.
34.	UTL	13/720,618		METHOD FOR MAKING INDUCTOR COIL STRUCTURE	PENDING	12/19/2012		Vishay Dale Electronics, Inc.
35.	UTL	13/768,039	8,975,994	INDUCTOR WITH THERMALLY STABLE RESISTANCE	ISSUED	2/15/2013	3/10/2015	Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
36.	UTL	13/750,404		INTEGRATED CIRCUIT ELEMENT AND ELECTRONIC CIRCUIT FOR LIGHT EMITTING DIODE APPLICATIONS	PENDING	1/25/2013		Vishay Dale Electronics, Inc.
37.	UTL	13/750,762		LOW PROFILE HIGH CURRENT COMPOSITE TRANSFORMER	PENDING	1/25/2013		Vishay Dale Electronics, Inc.
38.	UTL	14/015,488	8,878,643	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION	ISSUED	8/30/2013	11/4/2014	Vishay Dale Electronics, Inc.
39.	UTL	14/228,780	9,251,936	RESISTOR AND METHOD FOR MAKING SAME	ISSUED	3/28/2014	2/2/2016	Dale Electronics, Inc.
40.	UTL	14/203,234	9,396,849B 1	RESISTOR AND METHOD OF MANUFACTURE	ISSUED	3/10/2014	7/19/2016	Vishay-Dale, Inc.
41.	UTL	13/730,155	8,730,003	RESISTOR AND METHOD FOR MAKING SAME	ISSUED	12/28/2012	5/20/2014	Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
42.	UTL	14/242,982	10,026,540	MAGNETIC COMPONENTS AND METHODS FOR MAKING SAME	ISSUED	4/2/2014	1/17/2018	Dale Electronics, Inc.
43.	UTL	14/280,230	9,378,872	RESISTOR AND METHOD FOR MAKING SAME	ISSUED	5/16/2014	6/28/2016	Dale Electronics, Inc.
44.	UTL	14/287,883	9,396,847	EDGE-WOUND RESISTOR, RESISTOR ASSEMBLY, AND METHOD OF MAKING SAME	ISSUED	5/27/2014	7/19/2016	Dale Electronics, Inc.
45.	Design	29/491,946	D758,970	EDGE-WOUND RESISTOR	ISSUED	5/27/2014	6/14/2016	Dale Electronics, Inc.
46.	UTL	13/725,018	8,823,483	POWER RESISTOR WITH INTEGRATED HEAT SPREADER	ISSUED	12/21/2012	9/2/2014	Dale Electronics, Inc.
47.	UTL	14/473,118	9,502,161	POWER RESISTOR WITH INTEGRATED HEAT SPREADER	ISSUED	8/29/2014	11/22/2016	Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (Patent Description)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
48.	UTL	14/531,505	9,400,294	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSTATION	ISSUED	11/3/2014	7/26/2016	Vishay Dale Electronics, Inc.
49.	UTL	14/563,560		THERMALLY SPRAYED THIN FILM RESISTOR AND METHOD OF MAKING	PENDING	12/8/2014		Vishay Dale Electronics, Inc.
50.	UTL	14/928,893	10,083,781	SURFACE MOUNT RESISTORS AND METHODS OF MANUFACTURING SAME	ISSUED	10/30/2015	9/25/2018	Dale Electronics, Inc.
51.	UTL	15/012,386	9,916,921	RESISTOR AND METHOD FOR MAKING SAME	ISSUED	2/1/2016	3/13/2018	Dale Electronics, Inc.
52.	UTL	15/134,078		SHIELDED INDUCTOR AND METHOD OF MANUFACTURING	PENDING	4/20/2016		Dale Electronics, Inc.
53.	UTL	15/148,736		NESTED FLAT WOUND COILS FORMING WINDINGS FOR TRANSFORMERS AND INDUCTORS	PENDING	5/6/2016		Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (<u>Patent Description</u>)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
54.	DESIGN	29/567,803		EDGE-WOUND RESISTOR	PENDING	6/13/2016		Dale Electronics, Inc.
55.	UTL	15/213,199	9,934,891	RESISTOR AND METHOD OF MANUFACTURE	ISSUED	7/18/2016	4/3/2018	Vishay-Dale, Inc.
56.	UTL	15/193,530	10,147,524	RESISTOR AND METHOD FOR MAKING SAME	ISSUED	6/27/2016	12/4/2018	Dale Electronics, Inc.
57.	UTL	15/218,219		RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION	PENDING	7/25/2016		Dale Electronics, Inc.
58.	UTL	15/229,556	9,865,532	MOLDED PASSIVE COMPONENT FOR HIGH VOLTAGE APPLICATIONS	ISSUED	8/5/2016	1/9/2018	Dale Electronics, Inc.
59.	UTL	14/642,892	9,502,171	INDUCTOR WITH THERMALLY STABLE RESISTANCE	ISSUED	3/10/2015	11/22/2016	Dale Electronics, Inc.
60.	UTL	15/692,134		INDUCTOR HAVING HIGH CURRENT COIL WITH LOW DIRECT CURRENT RESISTANCE	PENDING	8/31/2017		Dale Electronics, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (Patent Description)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
61.	UTL	15/864,337		MOLDED BODY AND ELECTRICAL DEVICE HAVING A MOLDED BODY FOR HIGH VOLTAGE APPLICATIONS	PENDING	1/8/2018		Dale Electronics, Inc.
62.	UTL	16/139,654		SURFACE MOUNT RESISTORS AND METHODS OF MANUFACTURING SAME	PENDING	9/24/2018		Vishay Dale Electronics, LLC
63.	UTL	15/722,536	10,217,550	RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION	ISSUED	10/2/2017	2/26/2019	Vishay Dale Electronics, LLC
64.	UTL	16/181,006		RESISTOR WITH UPPER SURFACE HEAT DISSIPATION	PENDING	11/5/2018		Vishay Dale Electronics, LLC
65.	UTL	16/284,592		RESISTOR WITH TEMPERATURE COEFFICIENT OF RESISTANCE (TCR) COMPENSATION	PENDING	2/25/2019		Vishay Dale Electronics, LLC

Vishay Intertechnology, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (Patent Description)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
1.	UTL	10/002,868	6,873,028	SURGE CURRENT CHIP RESISTOR	ISSUED	11/15/2001	3/29/2005	Vishay Intertechnology, Inc.
2.	UTL	10/233,184	6,727,798	FLIP CHIP RESISTOR AND ITS MANUFACTURING METHOD	ISSUED	9/3 /2002	4/27/2004	Vishay Intertechnology, Inc.
3.	UTL	10/440,941	7,089,652	METHOD OF MANUFACTURING FLIP CHIP RESISTOR	ISSUED	5/19/2003	8/15/2006	Vishay Intertechnology, Inc.
4.	UTL	10/304,261	6,892,443	METHOD OF MANUFACTURING A RESISTOR	ISSUED	11/25/2002	5/17/2005	Vishay Intertechnology, Inc.
5.	UTL	10/762,609	7,154,370	HIGH PRECISION POWER RESISTORS	ISSUED	1/22/2004	12/26/2006	Vishay Intertechnology, Inc.
6.	UTL	10/967,883	7,278,201	METHOD OF MANUFACTURING A RESISTOR	ISSUED	10/18/2004	10/9/2007	Vishay Intertechnology, Inc.
7.	UTL	10/208,121	6,621,142	PRECISION HIGH-FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	ISSUED	7/29/2002	9/16/2003	Vishay Intertechnology, Inc.

PATENT

REEL: 049440 FRAME: 0903

PATENT

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (<u>Patent Description</u>)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
8.	UTL	10/208,59 9	6,621,143	PRECISION HIGH-FREQUENCY CAPACITOR ON SEMICONDUCTOR SUBSTRATE	ISSUED	7/29/2001	9/16/2003	Vishay Intertechnology, Inc.
9.	UTL	09/395,09 5	6,271,060	PROCESS OF FABRICATING A CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE	ISSUED	9/13/1999	8/7/2001	Vishay Intertechnology, Inc.
10.	UTL	09/395,09 4	6,316,287	CHIP SCALE SURFACE MOUNT PACKAGES FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME	ISSUED	9/13/1999	11/13/2001	Vishay Intertechnology, Inc.
11.	UTL	09/844,93 4	6,562,647	CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME	ISSUED	4/26/2001	5/13/2003	Vishay Intertechnology, Inc.
12.	UTL	10/157,58 4	6,876,061	CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME	ISSUED	5/28/2002	4/5/2005	Vishay Intertechnology, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
13.	UTL	09/688,300	6,970,496	RF MODEM AND COMMUNICATIONS TRANSCIEVER UTILIZING SAW DEVICE AND PULSE SHAPING	ISSUED	10/13/2000	11/29/2005	Vishay Intertechnology, Inc.
14.	UTL	09/419,824	6,535,545	RF MODEM UTILIZING SAW RESONATOR AND CORRELATOR AND COMMUNICATIONS TRANSCIEVER CONSTRUCTED THEREFROM	ISSUED	10/15/1999	3/18/2003	Vishay Intertechnology, Inc.
15.	UTL	12/030,281		SULFURATION RESISTANT CHIP RESISTOR AND METHOD FOR MAKING SAME	PENDING	2/13/2008		Vishay Intertechnology, Inc.
16.	UTL	12/035,472		SURFACE MOUNTED CHIP RESISTOR WITH FLEXIBLE LEADS	PENDING	2/22/2008		Vishay Intertechnology, Inc.
17.	UTL	09/395,095	6,271,060	PROCESS OF FABRICATING A CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE	ISSUED	9/13/1999	8/7/2001	Vishay Intertechnology, Inc.

PATENT

REEL: 049440 FRAME: 0905

PATENT

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (<u>Patent Description</u>)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
18.	UTL	09/733,823	6,441,475	CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME	ISSUED	12/8/2000	8/27/2002	Vishay Intertechnology, Inc.
19.	UTL	11/082,080	7,211,877	CHIP SCALE SURFACE MOUNT PACKAGE FOR SEMICONDUCTOR DEVICE AND PROCESS OF FABRICATING THE SAME	ISSUED	3/15/2005	5/1/2007	Vishay Intertechnology, Inc.
20.	UTL	10/456,018	7,151,036	PRECISION HIGH-FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	ISSUED	6/5/2003	12/19/2006	Vishay Intertechnology, Inc.
21.	UTL	11/601,501	8,004,063	PRECISION HIGH-FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	ISSUED	11/16/2006	8/23/2011	Vishay Intertechnology, Inc.
22.	UTL	10/208,121	6,621,142	PRECISION HIGH-FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	ISSUED	7/29/2002	9/16/2003	Vishay Intertechnology, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue</u> <u>Date</u>	<u>Domestic Loan Party</u>
23.	UTL	13/075,75 2	8,324,711	PRECISION HIGH FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	ISSUED	3/30/2011	12/4/2012	Vishay Intertechnology, Inc.
24.	UTL	13/592,09 1		PRECISION HIGH- FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	PENDING	12/3/2012		Vishay Intertechnology, Inc.

PATENT

REEL: 049440 FRAME: 0907

Siliconix incorporated

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
1.	UTL	08/047,723	5,410,170	DMOS POWER TRANSISTORS WITH REDUCED NUMBER OF CONTACTS USING INTEGRATED BODY-SOURCE CONNECTIONS	ISSUED	4/14/1993	4/25/1995	Siliconix incorporated
2.	UTL	07/762,103	5,298,442	TRENCH DMOS POWER TRANSISTOR WITH FIELD-SHAPING BODY PROFILE AND THREE-DIMENSIONAL GEOMETRY	ISSUED	9/18/1991	3/29/1994	Siliconix incorporated
3.	UTL	07/910,864	5,298,781	VERTICAL CURRENT FLOW FIELD EFFECT TRANSISTOR WITH THICK INSULATOR OVER NON-CHANNEL AREAS	ISSUED	7/8/1992	3/29/1994	Siliconix incorporated

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
4.	UTL	11/698,519	7,557,409	SUPER TRENCH MOSFET INCLUDING BURIED SOURCE ELECTRODE	ISSUED	1/26/2007	7/7/2009	Siliconix incorporated
5.	UTL	10/872,931	7,435,650	PROCESS FOR MANUFACTURING TRENCH MIS DEVICE HAVING IMPLANTED DRAIN-DRIFT REGION AND THICK BOTTOM OXIDE	ISSUED	6/21/2004	10/14/2008	Siliconix incorporated
6.	UTL	11/335,747	7,416,947	METHOD OF FABRICATING TRENCH MIS DEVICE WITH THICK OXIDE LAYER IN BOTTOM OF TRENCH	ISSUED	1/19/2006	8/26/2008	Siliconix incorporated

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
7.	UTL	10/996,148	7,394,150	SEMICONDUCTOR PACKAGE INCLUDING DIE INTERPOSED BETWEEN CUP-SHAPED LEAD FRAME AND LEAD FRAME HAVING MESAS AND VALLEYS	ISSUED	11/23/2004	7/1/2008	Siliconix incorporated
8.	UTL	11/158,382	7,326,995	TRENCH MIS DEVICE HAVING IMPLANTED DRAIN-DRIFT REGION AND THICK BOTTOM OXIDE	ISSUED	6/22/2005	2/5/2008	Siliconix incorporated
9.	UTL	10/454,031	7,291,884	TRENCH MIS DEVICE HAVING IMPLANTED DRAIN-DRIFT REGION AND THICK BOTTOM OXIDE	ISSUED	6/4/2003	11/6/2007	Siliconix incorporated
10.	UTL	11/232,613	7,268,032	TERMINATION FOR TRENCH MIS DEVICE HAVING IMPLANTED DRAIN-DRIFT REGION	ISSUED	9/21/2005	9/11/2007	Siliconix incorporated

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (<u>Patent Description</u>)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
11.	UTL	10/996,149	7,238,551	METHOD OF FABRICATING SEMICONDUCTOR PACKAGE INCLUDING DIE INTERPOSED BETWEEN CUP- SHAPED LEAD FRAME HAVING MESAS AND VALLEYS	ISSUED	11/23/2004	7/3/2007	Siliconix incorporated
12.	UTL	11/150,016	7,233,043	TRIPLE-DIEFUSED TRENCH MOSFET	ISSUED	6/10/2005	6/19/2007	Siliconix incorporated
13.	UTL	10/836,833	7,183,610	SUPER TRENCH MOSFET INCLUDING BURIED SOURCE ELECTRODE AND METHOD OF FABRICATING THE SAME	ISSUED	4/30/2004	2/27/2007	Siliconix incorporated
14.	UTL	11/141,942	7,118,953	PROCESS OF FABRICATING TERMINATION REGION FOR TRENCH MIS DEVICE	ISSUED	6/1/2005	10/10/2006	Siliconix incorporated

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (<u>Patent Description</u>)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
15.	UTL	10/810,031	7,045,857	TERMINATION FOR TRENCH MIS DEVICE HAVING IMPLANTED DRAIN-DRIFT REGION	ISSUED	3/26/2004	5/16/2006	Siliconix incorporated
16.	UTL	10/326,311	7,033,876	TRENCH MIS DEVICE HAVING IMPLANTED DRAIN-DRIFT REGION AND THICK BOTTOM OXIDE AND PROCESS FOR MANUFACTURING THE SAME	ISSUED	12/19/2002	4/25/2006	Siliconix incorporated
17.	UTL	10/180,154	7,012,005	SELF-ALIGNED DIFFERENTIAL OXIDATION IN TRENCHES BY ION IMPLANTATION	ISSUED	6/25/2002	3/14/2006	Siliconix incorporated
18.	UTL	10/722,984	7,009,247	TRENCH MIS DEVICE WITH THICK OXIDE LAYER IN BOTTOM OF GATE CONTACT TRENCH	ISSUED	11/25/2003	3/7/2006	Siliconix incorporated

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (<u>Patent Description</u>)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
19.	UTL	10/811,443	6,927,451	TERMINATION FOR TRENCH MIS DEVICE HAVING IMPLANTED DRAIN-DRIFT REGION	ISSUED	3/26/2004	8/9/2005	Siliconix incorporated
20.	UTL	10/264,816	6,921,697	METHOD FOR MAKING TRENCH MIS DEVICE WITH REDUCED GATE-TO-DRAIN CAPACTANCE	ISSUED	10/3/2002	7/26/2005	Siliconix incorporated
21.	UTL	10/657,830	6,913,977	TRIPLE-DIFFUSED TRENCH MOSFET AND METHOD OF FABRICATING THE SAME	ISSUED	9/8/2003	7/5/2005	Siliconix incorporated
22.	UTL	10/291,153	6,909,170	SEMICONDUCTOR ASSEMBLY WITH PACKAGE USING CUP-SHAPED LEAD FRAME	ISSUED	11/7/2002	6/21/2005	Siliconix incorporated
23.	UTL	10/106,812	6,903,412	TRENCH MIS DEVICE WITH GRADUATED GATE OXIDE LAYER	ISSUED	3/26/2002	6/7/2005	Siliconix incorporated

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> (<u>Patent Description</u>)	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
24.	UTL	09/927,320	6,882,000	TRENCH MIS DEVICE WITH REDUCED GATE- TO-DRAIN CAPACITANCE	ISSUED	8/10/2001	4/19/2005	Siliconix incorporated
25.	UTL	10/106,896	6,875,657	METHOD OF FABRICATING TRENCH MIS DEVICE WITH GRADUATED GATE OXIDE LAYER	ISSUED	3/26/2002	4/5/2005	Siliconix incorporated
26.	UTL	09/927,143	6,849,898	TRENCH MIS DEVICE WITH ACTIVE TRENCH CORNERS AND THICK BOTTOM OXIDE AND METHOD OF MAKING THE SAME	ISSUED	8/10/2001	2/1/2005	Siliconix incorporated
27.	UTL	10/104,811	6,838,722	STRUCTURES OF AND METHODS OF FABRICATING TRENCH-GATED MIS DEVICES	ISSUED	3/22/2002	1/4/2005	Siliconix incorporated
28.	UTL	10/317,568	6,764,906	METHOD FOR MAKING TRENCH MOSFET HAVING IMPLANTED DRAIN- DRIFT REGION	ISSUED	12/12/2002	7/20/2004	Siliconix incorporated

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29.	UTL	09/468,249	6,744,124	SEMICONDUCTOR DIE PACKAGE INCLUDING CUP-SHAPED LEADFRAME	ISSUED	12/10/1999	6/1/2004	Siliconix incorporated
30.	UTL	10/176,570	6,709,930	THICKER OXIDE FORMATION AT THE TRENCH BOTTOM BY SELECTIVE OXIDE DEPOSITION	ISSUED	6/21/2002	3/23/2004	Siliconix incorporated
31.	UTL	08/851,608	6,627,950	TRENCH DMOS POWER TRANSISTOR WITH FIELD-SHAPING BODY PROFILE AND THREE-DIMENSIONAL GEOMETRY	ISSUED	5/5/1997	9/30/2003	Siliconix incorporated
32.	UTL	10/211,438	6,600,193	TRENCH MOSFET HAVING IMPLANTED DRAIN-DRIFT REGION	ISSUED	8/2/2002	7/29/2003	Siliconix incorporated
33.	UTL	08/800,972	6,590,440	LOW-SIDE BIDIRECTIONAL BATTERY DISCONNECT SWITCH	ISSUED	2/19/1997	7/8/2003	Siliconix incorporated

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
34.	UTL	09/898,652	6,569,738	PROCESS FOR MANUFACTURING TRENCH GATED MOSFET HAVING DRAIN/DRIFT REGION	ISSUED	7/3/2001	5/27/2003	Siliconix incorporated
35.	UTL	09/816,717	6,534,366	METHOD OF FABRICATING TRENCH-GATED POWER MOSFET	ISSUED	3/21/2001	3/18/2003	Siliconix incorporated
36.	UTL	10/094,476	6,509,233	METHOD OF MAKING TRENCH- GATED MOSFET HAVING CESIUM GATE OXIDE LAYER	ISSUED	3/7/2002	1/21/2003	Siliconix incorporated
37.	UTL	09/545,287	6,392,290	VERTICAL STRUCTURE FOR SEMICONDUCTOR WAFER-LEVEL CHIP SCALE PACKAGES	ISSUED	4/7/2000	5/21/2002	Siliconix incorporated
38.	UTL	09/476,320	6,285,060	BARRIER ACCUMULATION MODE MOSFET	ISSUED	12/30/1999	9/4/2001	Siliconix incorporated

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title:</u> <u>(Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
39.	UTL	09/293,380	6,277,695	METHOD OF FORMING VERTICAL PLANAR DMOSFET WITH SELF-ALIGNED CONTACT	ISSUED	4/16/1999	8/21/2001	Siliconix incorporated
40.	UTL	09/089,250	6,204,533	VERTICAL TRENCH-GATED POWER MOSFET HAVING STRIPE GEOMETRY AND HIGH CELL DENSITY	ISSUED	6/2/1998	3/20/2001	Siliconix incorporated
41.	UTL	08/487,789	5,925,411	GAS-BASED SUBSTRATE DEPOSITION PROTECTION	ISSUED	6/7/1995	7/20/1999	Siliconix incorporated]
42.	UTL	09/481,135	6,444,527	METHOD OF OPERATION OF PUNCH-THROUGH FIELD EFFECT TRANSISTOR	ISSUED	1/11/2000	9/3/2002	Siliconix incorporated
43.	UTL	09/502,546	6,300,744	HIGH-EFFICIENCY BATTERY CHARGER	ISSUED	2/10/2000	10/9/2001	Siliconix incorporated
44.	DESIGN	29/151,024	D,466,873	SEMICONDUCTOR CHIP PACKAGE	ISSUED	10/31/2002	12/10/2002	Siliconix incorporated
45.	DESIGN	29/151,069	D,472,528	SEMICONDUCTOR CHIP PACKAGE	ISSUED	10/31/2002	4/1/2003	Siliconix incorporated

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46.	UTL	07/498,170	5,132,753	OPTIMIZATION OF BV AND RDS-ON BY GRADED DOPING IN LDD AND OTHER HIGH VOLTAGE ICs	ISSUED	3/23/1990	7/21/1992	Siliconix incorporated
47.	UTL	08/318,027	5,514,608	METHOD OF MAKING LIGHTLY-DOPED DRAIN DMOS WITH IMPROVED BREAKDOWN CHARACTERISTICS	ISSUED	10/4/1994	5/7/1996	Siliconix incorporated
48.	UTL	07/451,518	5,108,940	A MOS TRANSISTOR WITH A CHARGE INDUCED DRAIN EXTENSION	ISSUED	12/15/1989	4/28/1992	Siliconix incorporated
49.	UTL	08/647,073	5,648,281	METHOD FOR FORMING AN ISOLATION STRUCTURE AND A BIPOLAR TRANSISTOR ON A SEMICONDUCTOR SUBSTRATE	ISSUED	5/8/1996	7/15/1997	Siliconix incorporated
50.	UTL	06/757,582	4,682,405	METHOD FOR FORMING AN ELECTRICAL CONTACT IN A TRANSISTOR	ISSUED	7/22/1985	7/28/1987	Siliconix incorporated

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51.	UTL	98111605.6	895,290	METHOD FOR MAKING TERMINATION STRUCTURE FOR POWER MOSFET	ISSUED	12/21/1995	10/30/2002	Siliconix incorporated
52.	UTL	06/816,593	4,766,469	INTEGRATED BURIED ZENER DIODE AND TEMPERATURE COMPENSATION TRANSISTOR	ISSUED	1/6/1986	8/23/1988	Siliconix incorporated
53.	UTL	06/890,218	4,978,631	CURRENT SOURCE WITH A PROCESS SELECTABLE TEMPERATURE COEFFICIENT	ISSUED	7/25/1986	12/18/1990	Siliconix incorporated
54.	UTL	07/010,924	4,824,795	METHOD FOR OBTAINING REGIONS OF DIELECTRICALLY ISOLATED SINGLE CRYSTAL SILICON	ISSUED	2/5/1987	4/25/1989	Siliconix incorporated
55.	UTL	07/084,541	4,759,836	ION IMPLANTATION OF THIN FILM CRSIZ AND SIC RESISTORS	ISSUED	8/12/1987	7/26/1988	Siliconix incorporated
56.	UTL	06/808,904	4,779,123	INSULATED GATE TRANSISTOR ARRAY	ISSUED	12/13/1985	10/18/1998	Siliconix incorporated

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57.	UTL	07/243,166	4,896,196	VERTICAL DMOS POWER TRANSISTOR WITH AN INTEGRAL OPERATING CONDITION SENSOR	ISSUED	9/8/1988	1/23/1990	Siliconix incorporated
58.	UTL	06/838,217	4,798,810	METHOD FOR MANUFACTURING A POWER MOS TRANSISTOR	ISSUED	3/10/1986	1/17/1989	Siliconix incorporated
59.	UTL	06/894,418	4,707,909	MANUFACTURE OF TRIMMABLE HIGH VALUE POLYCRYSTALLINE SILICON RESISTORS	ISSUED	8/8/1986	11/24/1987	Siliconix incorporated
60.	UTL	08/415,009	5,592,005	PUNCH-THROUGH FIELD EFFECT TRANSISTOR	ISSUED	3/31/1995	1/7/1997	Siliconix incorporated
61.	UTL	06/808,575	4,674,020	POWER SUPPLY HAVING DUAL RAMP CONTROL CIRCUIT	ISSUED	12/13/1985	6/16/1987	Siliconix incorporated
62.	UTL	07/138,989	4,816,882	POWER MOS TRANSISTOR WITH EQUIPOTENTIAL RING	ISSUED	12/29/1987	3/28/1989	Siliconix incorporated

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63.	UTL	06/871,006	4,716,126	FABRICATION OF DOUBLE DIFFUSED METAL OXIDE SEMICONDUCTOR TRANSISTOR	ISSUED	6/5/1986	12/29/1987	Siliconix incorporated
64.	UTL	09/978,603	6,744,119	LEADFRAME HAVING SLOTS IN A DIE PAD	ISSUED	10/15/2001	6/1/2004	Siliconix incorporated
65.	UTL	07/036,777	4,853,563	SWITCH INTERFACE CIRCUIT FOR POWER MOSFET GATE DRIVE CONTROL	ISSUED	4/10/1987	8/1/1989	Siliconix incorporated
66.	UTL	07/195,436	4,794,436	HIGH VOLTAGE DRIFTED-DRAIN MOS TRANSISTOR	ISSUED	5/16/1988	12/27/1988	Siliconix incorporated
67.	UTL	07/246,937	4,920,388	TRANSISTOR WITH INTEGRATED GATE RESISTOR	ISSUED	9/19/1988	4/24/1990	Siliconix incorporated
68.	UTL	07/014,961	4,799,100	METHOD AND APPARATUS FOR INCREASING BREAKDOWN OF A PLANAR JUNCTION	ISSUED	2/17/1987	1/17/1989	Siliconix incorporated

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69.	UTL	06/927,882	4,827,324	IMPLANTATION OF IONS INTO AN INSULATING LAYER TO INCREASE PLANAR PN JUNCTION BREAKDOWN VOLTAGE	ISSUED	11/6/1986	5/2/1989	Siliconix incorporated
70.	UTL	10/113,526	6,856,006	ENCAPSULATION METHOD AND LEADFRAME FOR LEADLESS SEMICONDUCTOR PACKAGES (as amended)	ISSUED	3/28/2002	2/15/2005	Siliconix incorporated
71.	UTL	10/789,799	7,501,086B2	ENCAPSULATION METHOD FOR LEADLESS SEMICONDUCTOR PACKAGES	ISSUED	2/27/2004	3/10/2009	Siliconix incorporated
72.	UTL	12/401,549	8,928,157B2	LEADLESS SEMICONDUCTOR PACKAGES	ISSUED	3/10/2009	1/6/2015	Siliconix incorporated
73.	UTL	09/135,716		MULTILAYER SOLDER/BARRIER ATTACH FOR SEMICONDUCTOR CHIP	PENDING	8/17/1998		Siliconix incorporated

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74.	UTL	07/849,723	5,218,228	METHOD FOR FABRICATING A HIGH VOLTAGE MOS TRANSISTOR	ISSUED	3/11/1992	6/8/1993	Siliconix incorporated
75.	UTL	07/678,578	5,132,235	METHOD FOR FABRICATING A HIGH VOLTAGE MOS TRANSISTOR	ISSUED	3/29/1991	7/21/1992	Siliconix incorporated
76.	UTL	08/832,012	6,078,090	TRENCH-GATED SCHOTTKY DIODE WITH INTEGRAL CLAMPING DIODE	ISSUED	4/2/1997	6/20/2000	Siliconix incorporated
77.	UTL	07/095,481	4,791,462	DENSE VERTICAL J- MOS TRANSISTOR	ISSUED	9/10/1987	12/13/1988	Siliconix incorporated
78.	UTL	07/138,999	4,914,058	GROOVED DMOS PROCESS WITH VARYING GATE DIELECTRIC THICKNESS	ISSUED	12/19/1987	4/3/1990	Siliconix incorporated
79.	UTL	07/167,617	4,967,245	TRENCH POWER MOSFET DEVICE	ISSUED	3/14/1988	10/30/1990	Siliconix incorporated
80.	UTL	07/453,367	4,958,204	JUNCTION FIELD- EFFECT TRANSISTOR WITH A NOVEL GATE	ISSUED	12/21/1989	9/18/1990	Siliconix incorporated

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81.	UTL	07/141,877	4,936,930	METHOD FOR IMPROVED ALIGNMENT FOR SEMICONDUCTOR DEVICES WITH BURIED LAYERS	ISSUED	1/6/1988	6/26/1990	Siliconix incorporated
82.	UTL	09/314,621	6,268,242	METHOD OF FORMING VERTICAL MOSFET DEVICE HAVING VOLTAGE CLAMPED GATE AND SELF-ALIGNED CONTACT	ISSUED	5/19/1999	7/31/2001	Siliconix incorporated
83.	UTL	07/089,184	4,774,196	METHOD OF BONDING SEMICONDUCTOR WAFERS	ISSUED	8/25/1987	9/27/1988	Siliconix incorporated
84.	UTL	07/334,806	4,929,991	RUGGED LATERAL DMOS TRANSISTOR STRUCTURE	ISSUED	4/5/1989	5/29/1990	Siliconix incorporated
85.	UTL	07/099,452	4,835,586	DUAL-GATE HIGH DENSITY FET	ISSUED	9/21/1987	5/30/1989	Siliconix incorporated
86.	UTL	07/115,076	4,845,051	BURIED GATE JFET	ISSUED	10/29/1987	7/4/1989	Siliconix incorporated

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87.	UTL	07/107,725	5,164,325	METHOD OF MAKING A VERTICAL CURRENT FLOW FIELD EFFECT TRANSISTOR	ISSUED	10/8/1987	11/17/1992	Siliconix incorporated
88.	UTL	07/406,844	4,952,992	METHOD AND APPARATUS FOR IMPROVING THE ON-VOLTAGE CHARACTERISTICS OF A SEMICONDUCTOR DEVICE	ISSUED	9/13/1989	8/28/1990	Siliconix incorporated
89.	UTL	07/268,839	5,156,989	COMPLEMENTARY, ISOLATED DMOS IC TECHNOLOGY	ISSUED	11/8/1988	10/20/1992	Siliconix incorporated
90.	UTL	07/133,710	4,890,146	HIGH VOLTAGE LEVEL SHIFT SEMICONDUCTOR DEVICE	ISSUED	12/16/1987	12/26/1989	Siliconix incorporated
91.	UTL	11/151,749	7,595,547	SEMICONDUCTOR DIE PACKAGE INCLUDING CUP-SHAPED LEADFRAME	ISSUED	6/13/2005	9/29/2009	Siliconix incorporated
92.	UTL	12/487,666	9,040,356B2	SEMICONDUCTOR PACKAGING TECHNIQUES	ISSUED	6/19/2009	5/26/2015	Vishay-Siliconix, Inc.

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93.	UTL	07/290,546	5,072,266	TRENCH DMOS POWER TRANSISTOR WITH FIELD-SHAPING BODY PROFILE AND THREE- DIMENSIONAL GEOMETRY	ISSUED	12/27/1988	12/10/1991	Siliconix incorporated
94.	UTL	07/285,842	5,055,896	SELF-ALIGNED LDD LATERAL DMOS TRANSISTOR WITH HIGH-VOLTAGE INTERCONNECT CAPABILITY	ISSUED	12/15/1988	10/8/1991	Siliconix incorporated
95.	UTL	10/832,776	7,005,347	STRUCTURES OF AND METHOD OF FABRICATING TRENCH-GATED MIS DEVICES	ISSUED	4/27/2004	2/28/2006	Siliconix incorporated
96.	UTL	10/898,431	7,335,946	STRUCTURES OF AND METHOD OF FABRICATING TRENCH-GATED MIS DEVICES	ISSUED	7/22/2004	2/26/2008	Siliconix incorporated
97.	UTL	11/982,906	7,868,381B1	STRUCTURES OF AND METHOD OF FABRICATING TRENCH-GATED MIS DEVICES	ISSUED	11/5/2007	1/11/2011	Siliconix incorporated

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98.	UTL	09/591,179		TRENCH-GATED MIS DEVICE HAVING THICK POLYSILICON INSULATION LAYER AT TRENCH BOTTOM AND METHOD OF FABRICATING THE SAME	PENDING	6/8/2000		Siliconix incorporated
99.	UTL	11/112,403	7,494,876	TRENCH-GATED MIS DEVICE HAVING THICK POLYSILICON INSULATION LAYER AT TRENCH BOTTOM AND METHOD OF FABRICATING THE SAME	ISSUED	4/21/2005	2/24/2009	Siliconix incorporated
100.	UTL	09/908,178	6,552,889	CURRENT LIMITING TECHNIQUE FOR HYBRID POWER MOSFET CIRCUITS	ISSUED	7/17/2001	4/22/2003	Siliconix incorporated
101.	UTL	10/254,385	8,629,019B2	METHOD OF FORMING SELF ALIGNED CONTACTS FOR A POWER MOSFET	ISSUED	9/24/2002	1/14/2014	Siliconix incorporated

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102.	UTL	10/378,766		METHOD OF FORMING SELF ALIGNED CONTACTS FOR A POWER MOSFET	PENDING	3/3/2003		Siliconix incorporated
103.	UTL	10/951,831	7,642,164B1	METHOD OF FORMING SELF ALIGNED CONTACTS FOR A POWER MOSFET	ISSUED	9/27/2004	1/5/2010	Siliconix incorporated
104.	UTL	10/247,906	6,858,471	SEMICONDUCTOR SUBSTRATE WITH TRENCHES FOR REDUCING SUBSTRATE RESISTANCE	ISSUED	9/20/2002	2/22/2005	Siliconix incorporated
105.	UTL	10/869,382	8,080,459B2	SELF-ALIGNED CONTACT IN A SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	ISSUED	6/15/2004	12/20/2011	Siliconix incorporated

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106.	UTL	11/724,961		SELF-ALIGNED CONTACT IN A SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	PENDING	3/16/2007		Siliconix incorporated
107.	UTL	10/726,922	7,279,743	CLOSED CELL TRENCH METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR	ISSUED	12/2/2003	10/9/2007	Siliconix incorporated
108.	UTL	11/040,129	7,361,558	METHOD OF MANUFACTURING A CLOSED CELL TRENCH MOSFET	ISSUED	1/20/2005	4/22/2008	Siliconix incorporated
109.	UTL	12/107,738	7,833,863	METHOD OF MANUFACTURING A CLOSED CELL TRENCH MOSFET	ISSUED	4/22/2008	11/16/2010	Siliconix incorporated
110.	UTL	10/846,339	6,906,380	DRAIN SIDE GATE TRENCH METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR	ISSUED	5/13/2004	6/14/2005	Siliconix incorporated

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111.	UTL	12/050,929	8,183,629	STACKED TRENCH- OXIDE- SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICE	ISSUED	3/18/2008	5/22/2012	Siliconix incorporated
112.	UTL	11/023,327	7,344,945	METHOD OF MANUFACTURING A DRAIN SIDE GATE TRENCH METAL- OXIDE- SEMICONDUCTOR FIELD EFFECT TRANSISTOR	ISSUED	12/22/2004	3/18/2008	Siliconix incorporated
113.	UTL	11/352,031	7,880,446B2	ADAPTIVE FREQUENCY COMPENSATION FOR DC-TO-DC CONVERTER	ISSUED	2/10/2006	2/1/2011	Siliconix incorporated
114.	UTL	12/571,194	7,960,647B2	ADAPTIVE FREQUENCY COMPENSATION FOR DC-TO-DC CONVERTER	ISSUED	9/30/2009	6/14/2011	Siliconix incorporated
115.	UTL	11/386,927	8,409,954B2	ULTRA-LOW DRAIN-SOURCE RESISTANCE POWER MOSFET	ISSUED	3/21/2006	4/2/2013	Siliconix incorporated

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116.	UTL	12/069,712	9,887,266	ULTR-LOW DRAIN-SOURCE RESISTANCE POWER MOSFET	ISSUED	2/11/2008	2/6/2018	Siliconix incorporated
117.	UTL	11/799,889	8,471,390B2	POWER MOSFET CONTACT METALLIZATION	ISSUED	5/2/2007	6/25/2013	Siliconix incorporated
118.	UTL	11/373,630	9,685,524b2	NARROW SEMICONDUCTOR TRENCH STRUCTURE	ISSUED	3/9/2006	6/20/2017	Siliconix incorporated
119.	UTL	12/030,809	9,412,833B2	NARROW SEMICONDUCTOR TRENCH STRUCTURE	ISSUED	2/13/2008	8/9/2016	Siliconix incorporated
120.	UTL	11/190,682	7,583,485B1	ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT FOR INTEGRATED CIRCUITS	ISSUED	7/26/2005	9/1/2009	Siliconix incorporated
121.	UTL	12/552,205	8,582,258B1	ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT FOR INTEGRATED CIRCUITS	ISSUED	9/1/2009	11/12/2013	Siliconix incorporated

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122.	UTL	11/710,041	8,883,595B2	PROCESS FOR FORMING A SHORT CHANNEL TRENCH MOSFET AND DEVICE FORMED THEREBY	ISSUED	2/23/2007	11/11/2014	Siliconix incorporated
123.	UTL	11/322,040	7,544,545B2	TRENCH POLYSILICON DIODE	ISSUED	12/28/2005	6/9/2009	Siliconix incorporated
124.	UTL	12/009,379	7,612,431B2	TRENCH POLYSILICON DIODE	ISSUED	1/17/2008	11/3/2009	Siliconix incorporated
125.	UTL	12/611,865	8,072,013B1	TRENCH POLYSILICON DIODE	ISSUED	11/3/2009	12/6/2011	Siliconix incorporated
126.	UTL	12/098,950	8,368,126	TRENCH METAL OXIDE SEMICONDUCTOR WITH RECESSED TRENCH MATERIAL AND REMOTE CONTACTS	ISSUED	4/7/2008	2/5/2013	Siliconix incorporated
127.	UTL	11/651,258	9,437,729B2	HIGH-DENSITY POWER MOSFET WITH PLANARIZED METALIZATION	ISSUED	1/8/2007	9/6/2016	Siliconix incorporated

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128.	UTL	11/479,671	8,471,381B2	POWER MANAGEMENT SYSTEM IMPEMENTED IN A SINGLE SURFACE MOUNT PACKAGE	ISSUED	6/30/2006	6/25/2013	Siliconix incorporated
129.	UTL	12/779,815	8,928,138B2	COMPLETE POWER MANAGEMENT SYSTEM IMPEMENTED IN A SINGLE SURFACE MOUNT PACKAGE	ISSUED	5/13/2010	12/30/2014	Siliconix incorporated
130.	UTL	11/479,619	9,093,359B2	POWER MANAGEMENT SYSTEM IMPEMENTED IN A SINGLE SURFACE MOUNT PACKAGE	ISSUED	6/30/2006	7/28/2015	Siliconix incorporated
131.	UTL	11/644,553	9,425,043	HIGH MOBILITY POWER METAL- OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTORS	ISSUED	3/10/2006	8/23/2016	Siliconix incorporated

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132.	UTL	12/123,664	9,437,424B2	HIGH MOBILITY POWER METAL- OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTORS	ISSUED	5/20/2008	9/6/2016	Siliconix incorporated
133.	UTL	11/655,493	9,111,754B2	FLOATING GATE STRUCTURE WITH HIGH ELECTROSTATIC DISCHARGE PERFORMANCE	ISSUED	1/18/2007	8/18/2015	Siliconix incorporated
134.	UTL	11/823,375	8,222,874B2	A CURRENT MODE BOOST CONVERTER USING SLOPE COMPENSATION	ISSUED	6/26/2007	7/17/2012	Siliconix incorporated
135.	UTL	12/015,723	9,947,770B2	SELF-ALIGNED TRENCH MOSFET AND METHOD OF MANUFACTURE	ISSUED	1/17/2008	4/17/2018	Siliconix incorporated
136.	UTL	12/030,719		SELF-REPAIRING FIELD EFFECT TRANSISTOR	PENDING	2/13/2008		Siliconix incorporated
137.	UTL	12/203,846	9,484,451B	MOSFET ACTIVE AREA AND EDGE TERMINATION CHARGE BALANCE	ISSUED	9/3/2008	11/1/2016	Siliconix incorporated

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138.	UTL	12/119,367	8,269,263	HIGH CURRENT DENSITY POWER FIELD EFFECT TRANSISTOR	ISSUED	5/12/2008	9/18/2012	Siliconix incorporated
139.	UTL	12/603,028	9,419,129B2	SPLIT GATE SEMICONDUCTOR DEVICE WITH CURVED GATE OXIDE PROFILE	ISSUED	10/21/2009	8/16/2016	Siliconix incorporated
140.	UTL	12/548,841	9,425,306B2	SUPER JUNCTION TRENCH POWER MOSFET DEVICES	ISSUED	8/27/2009	8/23/2016	Siliconix incorporated
141.	UTL	12/549,190	9,443,974B2	SUPER JUNCTION TRENCH POWER MOSFET DEVICE FABRICATION	ISSUED	8/27/2009	9/13/2016	Siliconix incorporated
142.	UTL	12/873,147	9,230,810	SYSTEM AND METHOD FOR SUBSTRATE WAFER BACK SIDE AND EDGE CROSS SECTION SEALS	ISSUED	8/31/2010	1/5/2016	Siliconix incorporated
143.	UTL	12/829,247	8,735,992B2	POWER SWITCH WITH ACTIVE SNUBBER	ISSUED	7/1/2010	5/27/2014	Vishay-Siliconix, Inc.

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144.	UTL	12/610,148	9,306,056B2	SEMICONDUCTOR DEVICE WITH TRENCH-LIKE FEED-THROUGHS	ISSUED	10/30/2009	4/5/2016	Siliconix incorporated
145.				TRANSISTOR STRUCTURE WITH FEED-THROUGH SOURCE-TO - SUBSTRATE CONTACT	PENDING			Siliconix incorporated
146.				FIELD BOOSTED METAL-OXIDE- SEMICONDUCTOR FIELD EFFECT TRANSISTOR	ISSUED	6/25/2010	7/17/2018	Siliconix incorporated
147.	UTL	12/824,075	10,026,835		ISSUED	6/25/2010	7/17/2018	Siliconix incorporated
	UTL	12/869,554	9,425,305	STRUCTURES OF AND METHODS OF FABRICATING SPLIT GATE MIS DEVICES	ISSUED	8/26/2010	8/23/2016	Siliconix incorporated
148.	UTL	12/788,158	9,431,530B2	SUPER-HIGH DENSITY POWER TRENCH MOSFET	ISSUED	5/26/2010	8/30/2016	Siliconix incorporated

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149.	UTL	12/730,230	8,586,419b2	SEMICONDUCTOR PACKAGES INCLUDING DIE AND L-SHAPED LEAD AND METHOD OF MANUFACTURING	ISSUED	3/24/2010	11/19/2013	Vishay-Siliconix, Inc.
150.	UTL			STRUCTURES OF AND METHODS OF FABRICATING DUAL GATE MIS DEVICES	PENDING			Siliconix incorporated
151.	UTL	08/062,503	5,508,874	DISCONNECT SWITCH CIRCUIT TO POWER HEAD RETRACT IN HARD DISK DRIVE MEMORIES	ISSUED	5/14/1993	4/16/1996	Siliconix incorporated
152.	UTL	10/146,539	7,186,609	METHOD OF FABRICATING TRENCH JUNCTION BARRIER ERCTIFIER	ISSUED	5/14/2002	3/6/2007	Siliconix incorporated
153.	UTL	09/428,299	6,348,712	HIGH DENSITY TRENCH-GATED POWER MOSFET	ISSUED	10/27/1999	2/19/2002	Siliconix incorporated
154.	UTL			SEE VISH-11671-1D	PENDING			Siliconix incorporated

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155.	UTL	13/039,098	9,577,089	STRUCTURES OF AND METHODS OF FABRICATING DUAL GATE DEVICES	ISSUED	3/2/2011	2/21/2017	Siliconix incorporated
156.	UTL	61/487,627		SEMICONDUCTOR DEVICE HAVING REDUCED GATE CHARGES AND SUPERIOR FIGURE OF MERIT	PENDING	5/18/2011		Siliconix incorporated
157.	UTL	11/582,755		CHIP SCALE SCHOTTKY DEVICE	PENDING	5/11/2011		Siliconix incorporated
158.	UTL	13/229,667	8,822,273B2	DUAL LEAD FRAME SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURE	ISSUED	9/9/2011	9/2/2014	Vishay-Siliconix, Inc.
159.	UTL	13/308,375	9,431,550B2	TRENCH POLYSILICON DIODE	ISSUED	11/30/2011	8/30/2016	Siliconix incorporated
160.	UTL	13/370,243	9,614,043B2	MOSFET TERMINATION TRENCH	ISSUED	2/9/2012	4/4/2017	Siliconix incorporated

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161.	UTL	13/475,255		SEMICONDUCTOR DEVICE HAVING REDUCED GATE CHARGES AND SUPERIOR FIGURE OF MERIT	PENDING	5/18/2012		Siliconix incorporated
162.	UTL	13/484,114	9,716,166	ADAPTIVE CHARGE BALANCED EDGE TERMINATION	ISSUED	5/30/2012	12/12/2017	Siliconix incorporated
163.	UTL	13/460,567		HYBRID SPLIT GATE SEMICONDUCTOR	PENDING	4/30/2012		Siliconix incorporated
164.	UTL	13/460,600		METHOD OF FORMING A HYBRID SPLIT GATE SEMICONDUCTOR	PENDING	4/30/2012		Siliconix incorporated
165.	UTL	13/478,037		STACKED TRENCH METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR DEVICE	PENDING	5/22/2012		Siliconix incorporated
166.	UTL	13/565,672	8,836,404B2	PREVENTING REVERSE CONDUCTION	ISSUED	8/2/2012	9/16/2014	Vishey-Siliconix, Inc.

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167.	UTL	13/622,997	9,722,041	BREAKDOWN VOLTAGE BLOCKING DEVICE	ISSUED	9/19/2012	8/1/2017	Siliconix incorporated
168.	UTL	13/551,516	9,423,812B2	CURRENT MODE BOOST CONVERTER USING SLOPE COMPENSATION	ISSUED	7/17/2012	8/23/2016	Siliconix incorporated
169.	UTL	13/622,322		HIGH CURRENT DENSITY POWER FIELD EFFECT TRANSISTOR	PENDING	9/18/2012		Siliconix incorporated
170.	UTL	13/654,230	8,697,571B2	POWER MOSFET CONTACT METALIZATION	ISSUED	10/17/2012	4/15/2014	Vishay-Siliconix, Inc.
171.	UTL	13/728,997	8,883,580B2	TRENCH METAL OXIDE SEMICONDUCTOR WITH RECESSED TRENCH MATERIAL AND REMOTE CONTACTS	ISSUED	12/27/2012	11/11/2014	Siliconix incorporated
172.	UTL	13/829,623	9,966,330	POWER MOSFET PACKAGE WITH STACK DIE, LDMOS DIE STRUCTURE, FLIP CHIP ON LEADFRAME AND SOURCE, DRAIN AND GATE CLIPS	ISSUED	3/14/2013	5/8/2018	Siliconix incorporated

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173.	UTL	13/830,041	9,589,929	METHOD OF FABRICATING STACKED DIE PACKAGE	ISSUED	3/14/2013	3/7/2017	Siliconix incorporated
174.	UTL	13/732,284	9,853,140B2	ADAPTIVE CHARGE BALANCED MOSFET TECHNIQUES	ISSUED	12/31/2012	12/26/2017	Siliconix incorporated
175.	UTL	13/867,964	9,793,706B2	CURRENT LIMITING SYSTEMS AND METHODS	ISSUED	4/22/2013	10/17/2017	Siliconix incorporated
176.	UTL	12/917,172	8,604,525b2	TRANSISTOR STRUCTURE WITH FEED-THROUGH SOURCE-TO- SUBSTRATE CONTACT	ISSUED	11/1/2010	12/10/2013	Vishay-Siliconix, Inc.
177.	UTL	14/098,183		DUAL TRENCH STRUCTURE	PENDING	12/5/2013		Vishay-Siliconix, Inc.
178.	UTL	14/076,980		ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT FOR INTEGRATED CIRCUITS	PENDING	11/11/2013		Vishay-Siliconix, Inc.

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179.	UTL	14/102,208	9,064,896B2	TRANSISTOR STRUCTURE WITH FEED-THROUGH SOURCE-TO- SUBSTRATE CONTACT	ISSUED	12/10/2013	6/23/2015	Vishay-Siliconix, Inc.
180.	UTL	14/058,933		SEMICONDUCTOR STRUCTURE WITH HIGH ENERGY DOPANT IMPLANTATION	PENDING	10/21/2013		Vishay-Siliconix
181.	UTL	14/153,986		METHOD OF FORMING SELF ALIGNED CONTACTS FOR A POWER MOSFET	PENDING	1/13/2014		Vishay-Siliconix, Inc.
182.	UTL	14/221,012		SELF-ALIGNED TRENCH MOSFET AND METHOD OF MANUFACTURE	PENDING	3/20/2014		Vishay-Siliconix, Inc.
183.	UTL	14/311,165	9,508,596B2	PROCESSES USED IN FABRICATING A METAL- INSULATOR- SEMICONDUCTOR FIELD EFFECT TRANSISTOR	ISSUED	6/20/2014	11/29/2016	Vishay-Siliconix, Inc.

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184.	UTL	14/465,697	9,425,304B2	TRANSISTOR STRUCTURE WITH IMPROVED UNCLAMPED INDUCTIVE SWITCHING IMMUNITY	ISSUED	8/21/2014	8/23/2016	Vishay-Siliconix, Inc.
185.	UTL	14/341,772	9,184,152b2	DUAL LEAD FRAME SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURE	ISSUED	7/26/2014	11/10/2015	Vishay-Siliconix, Inc.
186.	UTL	14/474,420	9,595,503	DUAL LEAD FRAME SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURE	ISSUED	9/2/2014	3/14/2017	Vishay- Siliconix, Inc.
187.	UTL	14/486,926	9,787,309B2	PREVENTING RESERVE CONDUCTION	ISSUED	9/15/2014	10/10/2017	Vishay-Siliconix, Inc.
188.	UTL	14/537,760	9,831,336B2	PROCESS FOR FORMING A SHORT CHANNEL TRENCH MOSFET AND DEVICE FORMED THEREBY	ISSUED	11/11/2014	11/28/2017	Siliconix Incorporated

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189.	UTL	14/659,394	9,887,259B2	MODULATED SUPER JUNCTION POWER MOSFET DEVICES	ISSUED	3/16/2015	2/6/2018	Vishay-Siliconix
190.	UTL	14/659,415		SEMICONDUCTOR DEVICE WITH COMPOSITE TRENCH AND IMPLANT COLUMNS	PENDING	3/16/2015		Vishay-Siliconix, Inc.
191.	UTL	14/663,872	9,935,193B2	MOSFET TERMINATION TRENCH	ISSUED	3/20/2015	4/3/2018	Vishay-Siliconix, Inc.
192.	UTL	14/711,553	9,443,959B2	TRANSISTOR STRUCTURE WITH FEED-THROUGH SOURCE-TO- SUBSTRATE CONTACT	ISSUED	5/13/2015	9/13/2016	Vishay-Siliconix, Inc.
193.	UTL	14/830,277	9,882,044B2	EDGE TERMINATION FOR SUPER-JUNCTION MOSFETS	ISSUED	8/9/2015	1/30/2018	Vishay-Siliconix
194.	UTL	14/830,324	10,234,486	VERTICAL SENSE DEVICES IN VERTICAL TRENCH MOSFET	ISSUED	8/19/2015	3/19/2019	Vishay-Siliconix

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195.	UTL	14/811,579		COMPLETE POWER MANAGEMENT SYSTEM IMPLEMENTED IN A SINGLE SURFACE MOUNT PACKAGE	PENDING	7/28/2015		Vishay-Siliconix
196.	UTL	11/966,695	9,136,060B2	PRECISION HIGH-FREQUENCY CAPACITOR FORMED ON SEMICONDUCTOR SUBSTRATE	ISSUED	12/28/2007	9/15/2015	Vishay-Siliconix, Inc.
197.	UTL	14/988,639		SYSTEM AND METHOD FOR SUBSTRATE WAFER BACK SIDE AND EDGE CROSS SECTION SEALS	PENDING	1/5/2016		Vishay-Siliconix, Inc.
198.	UTL	12/917,378	9,324,858B2	TRENCH-GATED MIS DEVICES	ISSUED	11/1/2010	4/26/2016	Vishay-Siliconix, Inc.
199.	UTL	15/097,024		SEMICONDUCTOR DEVICE HAVING MULTIPLE GATE PADS	PENDING	4/12/2016		Vishay-Siliconix, Inc.
200.	UTL	13/309,444	9,431,249B2	EDGE TERMINATION FOR SUPER JUNCTION MOSFET DEVICES	ISSUED	12/1/2011	8/30/2016	Vishay-Siliconix, Inc.

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201.	UTL	15/091,431	10,032,901	SEMICONDUCTOR DEVICE WITH TRENCH-LIKE FEED-THROUGHS	ISSUED	4/5/2016	7/24/2018	Vishay-Siliconix, Inc.
202.	UTL	15/237,259	9,893,168B2	SPLIT GATE SEMICONDUCTOR DEVICE WITH CURVED GATE OXIDE PROFILE	ISSUED	8/15/2016	2/13/2018	Vishay-Siliconix, Inc.
203.	UTL	15/263,882		TRENCH MOSFET WITH SELF-ALIGN BODY CONTACT WITH SPACER	PENDING	9/13/2016		Vishay-Siliconix, Inc.
204.	UTL	15/339,678	10,084,037	MOSFET ACTIVE AREA AND EDGE TERMINATION AREA CHARGE BALANCE	ISSUED	10/31/2016	9/25/2018	Vishay-Siliconix, Inc.
205.	UTL	15/364,109		PROCESSES USED IN FABRICATING A METAL- INSULATOR- SEMICONDUCTOR FIELD EFFECT TRANSISTOR	PENDING	11/29/2016		Vishay-Siliconix, Inc.
206.	UTL	15/439,817		METHOD FOR FABRICATING STACK DIE PACKAGE	PENDING	2/22/2017		Vishay-Siliconix, Inc.

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207.	UTL	15/457,790	10,229,893	DUAL LEAD FRAME SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURE	ISSUED	3/13/2017	3/12/2019	Vishay-Siliconix, Inc.
208.	UTL	14/794,164	9,673,314B2	SEMICONDUCTOR DEVICE WITH NON-UNIFORM TRENCH OXIDE LAYER	ISSUED	7/8/2015	6/6/2017	Vishay-Siliconix, Inc.
209.	UTL	16/044,835		HIGH ELECTRON MOBILITY TRANSISTOR WITH ESD PROTECTION STRUCTURES	PENDING	7/25/2018		Vishay-Siliconix, Inc.
210.	UTL	15/634,739		VERTICAL SENSE DEVICES IN VERTICAL TRENCH MOSFET	PENDING	6/27/2017		Vishay-Siliconix, Inc.
211.	UTL	15/595,743		EDGE TERMINATION FOR SUPER-JUNCTION MOSFETS	PENDING	5/15/2017		Vishay-Siliconix, Inc.
212.	UTL	15/614,257	9,978,859B2	SEMICONDUCTOR DEVICE WITH NON-UNIFORM TRENCH OXIDE LAYER	ISSUED	6/5/2017	5/22/2018	Vishay-Siliconix, Inc.

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213.	UTL	15/093,557	9,761,696	SELF-ALIGNED TRENCH MOSFET AND METHOD OF MANUFACTURE	ISSUED	3/20/2014	9/12/2017	Vishay-Siliconix, Inc.
214.	UTL	15/643,306	10,224,426	HIGH-ELECTRON MOBILITY TRANSISTOR DEVICES	ISSUED	7/6/2017	3/5/2019	Vishay-Siliconix, Inc.
215.	UTL	15/643,328		HIGH-ELECTRON- MOBILITY TRANSISTOR WITH BURIED INTERCONNECT	PENDING	7/6/2017		Vishay-Siliconix, Inc.
216.	UTL	15/659,539	10,181,523	TRANSISTOR STRUCTURE WITH IMPROVED UNCLAMPED INDUCTIVE SWITCHING IMMUNITY	ISSUED	7/25/2017	1/15/2019	Vishay-Siliconix, Inc.
217.	UTL	15/786,437		CURRENT LIMITING SYSTEMS AND METHODS	PENDING	10/17/2017		Vishay-Siliconix, Inc.
218.	UTL	15/838,165	10,229,988	ADAPTIVE CHARGE BALANCED EDGE TERMINATION	ISSUED	12/11/2017	3/12/2019	Vishay-Siliconix, Inc.

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219.	UTL	15/854,648		ADAPTIVE CHARGE BALANCED MOSFET TECHNIQUES	PENDING	12/26/2017		Vishay-Siliconix, Inc.
220.	UTL	15/889,784		MODULATED SUPER JUNCTION POWER MOSFET DEVICES	PENDING	2/6/2018		Vishay-Siliconix, Inc.
221.	UTL	16/002,413		DEVICES AND METHODS FOR DRIVING A SEMICONDUCTOR SWITCHING SERVICE	PENDING	6/7/2018		Vishay-Siliconix, Inc.
222.	UTL	16/019,282		PROTECTION CIRCUITS WITH NEGATIVE GATE SWING CAPABILITY	PENDING	6/26/2018		Vishay-Siliconix, Inc.
223.	UTL	16/262,598		SPLIT GATE SEMICONDUCTOR WITH NON- UNIFORM TRENCH OXIDE	PENDING	1/30/2019		Vishay Siliconix
224.	UTL	16/291,996		HIGH-ELECTRON- MOBILITY TRANSISTOR DEVICES	PENDING	3/4/2019		Vishay Siliconix

Vishay Sprague, Inc.

	<u>Type</u>	<u>Serial No.</u>	<u>Patent No.</u>	<u>Title: (Patent Description)</u>	<u>Status</u>	<u>File Date</u>	<u>Issue Date</u>	<u>Domestic Loan Party</u>
1.	UTL	09/441,434	6,184,775	SURFACE MOUNT RESISTOR	ISSUED	11/16/1999	2/6/2001	Vishay Sprague, Inc.
2.	UTL	09/074,185	6,159,817	MULTI-TAP THIN FILM INDUCTOR	ISSUED	5/7/1998	12/12/2000	Vishay EFL, Inc.
3.	UTL	11/266,915	7,449,032	METHOD OF MANUFACTURING SURFACE MOUNT CAPACITOR	ISSUED	11/4/2005	11/11/2008	Vishay Sprague, Inc.
4.	UTL	11/293,673	7,283,350	SURFACE MOUNT CHIP CAPACITOR	ISSUED	12/2/2005	10/16/2007	Vishay Sprague, Inc.
5.	UTL	11/132,116	7,161,797	SURFACE MOUNT CAPACITOR AND METHOD OF MAKING SAME	ISSUED	5/17/2005	1/9/2007	Vishay Sprague, Inc.
6.	UTL	10/792,639	7,085,127	SURFACE MOUNT CHIP CAPACITOR	ISSUED	3/2/2004	8/1/2006	Vishay Sprague, Inc.
7.	UTL	10/792,135	6,914,770	SURFACE MOUNT FLIPCHIP CAPACITOR	ISSUED	3/2/2004	7/5/2005	Vishay Sprague, Inc.
8.	UTL	12/759,769		HERMETICALLY SEALED WET ELECTROLYTIC CAPACITOR	PENDING	4/14/2010		Vishay Sprague, Inc
9.	UTL	12/107,349		FRAME PACKAGED ARRAY ELECTRONIC COMPONENT	PENDING	4/22/2008		Vishay Sprague, Inc

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10.	UTL	12/189,492		HIGH VOLTAGE CAPACITORS	PENDING	8/11/2008		Vishay Sprague, Inc
11.	UTL	12/052,251		ELECTROPHORETIC ALLY DEPOSITED CATHODE CAPACITOR	PENDING	3/20/2008		Vishay Sprague, Inc
12.	UTL	07/677,203	5,099,397	FUZED SOLID ELECTROLYTE CAPACITOR	ISSUED	3/29/1991	3/24/1992	Sprague Electric Company
13.	UTL	07/677,204	5,053,927	MOLDED FUZED SOLID ELECTROLYTE CAPACITOR	ISSUED	3/29/1991	10/1/1991	Sprague Electric Company

Vishay GSI, Inc.

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1.	UTL	14/043,43 1	9,202,935	ZENER DIODE HAVING A POLYSILICON LAYER FOR IMPROVED REVERSE SURGE VOLTAGE CAPABILITY AND DECREASED LEAKAGE CURRENT	ISSUED	10/1/2013	12/1/2015	Vishay General Semiconductor, Inc.
2.	UTL	14/152,56 4	9,178,015	TRENCH MOS DEVICE HAVING A TERMINATION STRUCTURE WITH MULTIPLE FIELD- RELAXATION TRENCHES FOR HIGH VOLTAGE APPLICATIONS	ISSUED	1/10/2014	11/3/2015	Vishay General Semiconductor, Inc.
3.	UTL	14/627,01 3	9,281,417	GaN-BASED SCHOTTKY DIODE HAVING LARGE BOND PADS AND REDUCED CONTACT RESISTANCE	ISSUED	2/20/2015	3/8/2016	Vishay General Semiconductor, Inc.

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4.	UTL	14/154,804	9,263,820	ELECTRICAL PRESS-FIT PIN FOR A SEMICONDUCTOR MODULE	ISSUED	1/14/2014	2/16/2016	Vishay General Semiconductor, Inc.
5.	DIV	14/819,826	9,331,142	ZENER DIODE HAVING A POLYSILICON LAYER FOR IMPROVED REVERSE SURGE VOLTAGE CAPABILITY AND DECREASED LEAKAGE CURRENT	ISSUED	8/6/2015	5/3/2016	Vishay General Semiconductor, Inc.
6.	UTL	13/937,724	9,368,584	GALLIUM-NITRIDE POWER SEMICONDUCTOR DEVICE WITH VERTICAL STRUCTURE	ISSUED	7/9/2013	6/14/2016	Vishay General Semiconductor, Inc.
7.	DIV	14/608,742	9,537,017	PROCESS FOR FORMING A PLANAR DIODE USING ONE MASK	ISSUED	1/29/2015	1/3/2017	Vishay General Semiconductor, Inc.

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8.	UTL	15/906,698		POWER SEMICONDUCTOR DEVICE WITH NOVEL FIELD PLATE STRUCTURE	PENDING	2/27/2018		Vishay General Semiconductor, Inc.

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