PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT5533273

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
RAMBUS INC.	05/04/2018

RECEIVING PARTY DATA

Name:	HEFEI RELIANCE MEMORY LIMITED
Street Address:	ROOM A-08, 14TH FLOOR, PLAZA A, BUILDING J1
Internal Address:	INNOVATIVE INDUSTRIAL PARK PHASE II, HIGH-TECH ZONE
City:	HEFEI
State/Country:	CHINA

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	16462721

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ATTORNEY DOCKET NUMBER:	62KS-294816
NAME OF SUBMITTER:	WEIGUO CHEN
SIGNATURE:	/Weiguo Chen/
DATE SIGNED:	05/21/2019

Total Attachments: 4
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ASSIGNMENT OF PATENT RIGHTS

Assignor: Rambus Inc.
Address: 1050 Enterprise Way, Suite 700
Sunnyvale, CA 94089 USA

Assignee: Hefei Reliance Memory Limited
(with its Chinese name "合肥睿科微电子有限公司")
Address: Room A-08, 14th Floor, Plaza A, Building J1, Innovative Industrial Park
Phase II, High-tech Zone, Hefei, People's Republic of China

For good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, **Rambus Inc.** ("Assignor"), a Delaware corporation, and **Hefei Reliance Memory Limited (with its Chinese name "合肥睿科微电子有限公司")** ("Assignee"), agree as follows:

Patents

"Patents" means the following patents and patent applications:

Patents Notable with Respect to RRAM
RRAM有关专利清单

No.	Jurisdiction 地域	Patent/Publication/ Application # 专利号	App Title 应用名称
1	US	6972985	MEMORY ELEMENT HAVING ISLANDS
2	US	7082052	MULTI-RESISTIVE STATE ELEMENT WITH REACTIVE METAL
3	US	7394679	MULTI-RESISTIVE STATE ELEMENT WITH REACTIVE METAL
4	US	7538338	MEMORY USING VARIABLE TUNNEL BARRIER WIDTHS
5	US	7889539	MULTI-RESISTIVE STATE MEMORY DEVICE WITH CONDUCTIVE OXIDE ELECTRODES
6	US	8062942	METHOD FOR FABRICATING MULTI-RESISTIVE STATE MEMORY DEVICES
7	US	8237142	CONTINUOUS PLANE OF THIN-FILM MATERIALS FOR A TWO-TERMINAL CROSS-POINT MEMORY
8	US	8274817	NON VOLATILE MEMORY DEVICE ION BARRIER
9	US	8339867	FUSE ELEMENTS BASED ON TWO-TERMINAL RE-WRITEABLE NON-VOLATILE MEMORY
10	US	8395928	THRESHOLD DEVICE FOR A MEMORY ARRAY
11	US	8610099	PLANAR RESISTIVE MEMORY INTEGRATION
12	US	8611130	METHOD FOR FABRICATING MULTI-RESISTIVE STATE MEMORY DEVICES
13	US	8675389	MEMORY ELEMENT WITH A REACTIVE METAL LAYER
14	US	8861259	RESISTANCE CHANGE MEMORY CELL CIRCUITS AND METHODS
15	US	9029827	PLANAR RESISTIVE MEMORY INTEGRATION
16	US	9058300	INTEGRATED CIRCUITS AND METHODS TO CONTROL ACCESS TO MULTIPLE LAYERS OF MEMORY
17	US	9153321	RESISTANCE CHANGE MEMORY CELL CIRCUITS AND METHODS
18	US	9159408	MEMORY ELEMENT WITH A REACTIVE METAL LAYER
19	US	9159913	TWO-TERMINAL REVERSIBLY SWITCHABLE MEMORY DEVICE
20	US	9230641	FAST READ SPEED MEMORY DEVICE

No.	Jurisdiction 地域	Patent/Publication/ Application # 专利号	App Title 应用名称
21	US	9305644	RESISTANCE MEMORY CELL
22	US	9390798	1T-1R ARCHITECTURE FOR RESISTIVE RANDOM ACCESS MEMORY
23	US	9437291	DISTRIBUTED CASCODE CURRENT SOURCE FOR RRAM SET CURRENT LIMITATION
24	US	9484533	MULTI-LAYERED CONDUCTIVE METAL OXIDE STRUCTURES AND METHODS FOR FACILITATING ENHANCED PERFORMANCE CHARACTERISTICS OF TWO-TERMINAL MEMORY CELLS
25	US	9490009	FAST READ SPEED MEMORY DEVICE
26	US	9570164	SYSTEM AND METHOD FOR PERFORMING MEMORY OPERATIONS ON RRAM CELLS
27	US	9570165	1D-2R MEMORY ARCHITECTURE
28	US	9570171	RESISTANCE CHANGE MEMORY CELL CIRCUITS AND METHODS
29	US	9570515	MEMORY ELEMENT WITH A REACTIVE METAL LAYER
30	US	9806130	MEMORY ELEMENT WITH A REACTIVE METAL LAYER
31	US	9818480	RESISTANCE CHANGE MEMORY CELL CIRCUITS AND METHODS
32	US	9818799	MULTI-LAYERED CONDUCTIVE METAL OXIDE STRUCTURES AND METHODS FOR FACILITATING ENHANCED PERFORMANCE CHARACTERISTICS OF TWO-TERMINAL MEMORY CELLS
33	US	9824752	1T-1R ARCHITECTURE FOR RESISTIVE RANDOM ACCESS MEMORY
34	US	9831425	TWO-TERMINAL REVERSIBLY SWITCHABLE MEMORY DEVICE
35	TW	I602177	SYSTEM AND METHOD FOR PERFORMING MEMORY OPERATIONS ON RRAM CELLS
36	CN	ZL2015201657805	MEMORY DEVICE
37	CN	ZL200580038024.5	MEMORY ELEMENT AND METHOD FOR CREATING MEMORY EFFECT
38	US	2016-0240249	RESISTANCE MEMORY CELL
39	US	2016-0379710	2T-1R ARCHITECTURE FOR RESISTIVE RAM
40	US	2017-0110188	FAST READ SPEED MEMORY DEVICE
41	US	2017-0004882	DISTRIBUTED CASCODE CURRENT SOURCE FOR RRAM SET CURRENT LIMITATION
42	US	2017-0178723	SYSTEM AND METHOD FOR PERFORMING MEMORY OPERATIONS ON RRAM CELLS
43	TW	201735036	SYSTEM AND METHOD FOR PERFORMING MEMORY OPERATIONS ON RRAM CELLS
44	US	15/817,887	1T-1R ARCHITECTURE FOR RESISTIVE RANDOM ACCESS MEMORY
45	US	2018-0122857	MEMORY ELEMENT WITH A REACTIVE METAL LAYER
46	US	15/797,452	TWO-TERMINAL REVERSIBLY SWITCHABLE MEMORY DEVICE
47	US	15/811,179	MULTI-LAYERED CONDUCTIVE METAL OXIDE STRUCTURES AND METHODS FOR FACILITATING ENHANCED PERFORMANCE CHARACTERISTICS OF TWO-TERMINAL MEMORY CELLS
48	US	2018-0122471	RESISTANCE CHANGE MEMORY CELL CIRCUITS AND METHODS
49	WO	PCT/US17/067349	RRAM WRITE
50	WO	PCT/US17/061393	RRAM PROCESS INTERGRATION SCHEME AND CELL STRUCTURE WITH REDUCED MASKING OPERATIONS
51	WO	WO 2018-057191	TECHNIQUES FOR INITIALIZING RESISTIVE MEMORY DEVICES
52	WO	PCT/US17/061394	NON-VOLATILE MEMORY STRUCTURE WITH POSITIONED DOPING
53	WO	PCT/US17/052761	ADAPTIVE MEMORY CELL WRITE CONDITIONS
54	TW	106123197	TECHNIQUES FOR INITIALIZING RESISTIVE MEMORY DEVICES

Patents Notable with Respect to DRAM
DRAM有关专利清单

No.	Jurisdiction 地域	Patent/Publication # 专利号	App Title 应用名称
55	US	7355234	SEMICONDUCTOR DEVICE INCLUDING A STACKED CAPACITOR
56	US	7382014	SEMICONDUCTOR DEVICE WITH CAPACITOR SUPPRESSING LEAK CURRENT

No.	Jurisdiction 地域	Patent/Publication # 专利号	App Title 应用名称
57	US	7452813	METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE HAVING PLANARIZED INTERLAYER INSULATING FILM
58	US	7618869	MANUFACTURING METHOD FOR INCREASING PRODUCT YIELD OF MEMORY DEVICES SUFFERING FROM SOURCE/DRAIN JUNCTION LEAKAGE
59	US	7632696	SEMICONDUCTOR CHIP WITH A POROUS SINGLE LAYER AND MANUFACTURING METHOD OF THE SAME
60	US	7649256	SEMICONDUCTOR CHIP HAVING POLLISHED AND GROUND BOTTOM SURFACE PORTIONS
61	US	7684261	SEMICONDUCTOR APPARATUS
62	US	7691543	MASK DATA CREATION METHOD
63	US	7708621	POLISHING APPARATUS AND METHOD OF RECONDITIONING POLISHING PAD
64	US	7732273	SEMICONDUCTOR DEVICE MANUFACTURING METHOD AND SEMICONDUCTOR DEVICE
65	US	7737048	METHOD FOR CONTROLLING THICKNESS DISTRIBUTION OF A FILM
66	US	7737505	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE SAME
67	US	7741176	METHOD FOR FABRICATING A CYLINDRICAL CAPACITOR INCLUDING IMPLANTING IMPURITIES INTO THE UPPER SECTIONS OF THE LOWER ELECTRODE TO PREVENT THE FORMATION OF HEMISPHERICAL GRAIN SILICON ON THE UPPER SECTIONS
68	US	7741215	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME
69	US	7767569	METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE
70	US	7863191	MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE
71	US	7875518	SEMICONDUCTOR DEVICE HAVING SILICON LAYER IN A GATE ELECTRODE
72	US	8139424	SEMICONDUCTOR APPARATUS
73	US	8509009	SEMICONDUCTOR APPARATUS
74	JP	4072522	SEMICONDUCTOR DEVICE AND MANUFATURING METHOD THEREOF
75	JP	4237152	METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE
76	JP	4389222	METHOD FOR CREATING MASK DATA
77	JP	4437301	MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE
78	CN	ZL200510136967.3	SEMICONDUCTOR DEVICE HAVING A SILICON LAYER IN A GATE ELECTRODE
79	US	7592249	METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE
80	US	7592234	METHOD FOR FORMING A NITROGEN-CONTAINING GATE INSULATING FILM
81	US	7598549	SEMICONDUCTOR DEVICE HAVING A SILICON LAYER IN A GATE ELECTRODE

Assignment

Effective May 4, 2018, Assignor hereby irrevocably assigns, transfers, and conveys to Assignee all of its right, title, and interest in and to the Patents, and all of its rights, claims, and privileges pertaining to, arising out of, or associated with, the Patents, including, without limitation, the right to the underlying inventions, the right to file, prosecute and maintain the Patents, and the right to sue, seek equitable relief, and recover damages for past, present, and future infringement thereof.

Further Assignment

Assignor further assigns to and empowers Assignee, its successors, assigns, or nominees, all rights to make applications for patents or other forms of protection for said inventions and to prosecute such applications and the Patents.

Assignor's representative signing below represents that he or she is duly authorized to sign documents on behalf of Assignor.

Assignor grants Assignee or its agents the power to insert on this Assignment any further identification that may be necessary or desirable to in order to comply with the rules of the United States Patent and Trademark Office for recordation of this document.

EXECUTED this 4th day of May, 2018.

RAMBUS INC.

Signed _____

Typed Name: Gary Bronner

Title: Vice President

HEFEI RELIANCE MEMORY LIMITED

(with its Chinese name "合肥睿科微电子有限公司")

Signed _____

Typed Name: Zhiheo Lu

Title: CEO