

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT5703190

SUBMISSION TYPE:	NEW ASSIGNMENT		
NATURE OF CONVEYANCE:	ASSIGNMENT		
CONVEYING PARTY DATA			
Name			Execution Date
YANG LIU			03/15/2018
RECEIVING PARTY DATA			
Name:	ELENION TECHNOLOGIES, LLC		
Street Address:	171 MADISON AVENUE		
Internal Address:	SUITE 1100		
City:	NEW YORK		
State/Country:	NEW YORK		
Postal Code:	10016		
PROPERTY NUMBERS Total: 1			
Property Type	Number		
Application Number:	16126864		
CORRESPONDENCE DATA			
Fax Number:			
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>			
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ATTORNEY DOCKET NUMBER:	0200-106USP1		
NAME OF SUBMITTER:	AFSHIN (MEHDI) ZAMANPOUR		
SIGNATURE:	/Mehdi Zamanpour/		
DATE SIGNED:	09/05/2019		
Total Attachments: 4			
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ASSIGNMENT- MULTIPLE MATTERS

In conjunction with the "Proprietary Information and Inventions Agreement" previously executed by the undersigned ("Assignor"), for valuable consideration given to Assignor, the receipt and sufficiency of which is hereby acknowledged, Assignor re-confirms that he or she agrees to assign, and hereby does assign, transfer and set over to **Elenion Technologies, LLC**, having a place of business at 171 Madison Avenue, Suite 1100, New York NY 10016, (hereinafter "Assignee") his or her entire right, title, and interest in the invention(s) identified in Exhibit A throughout the world, and his or her entire right, title, and interest in the invention(s) as regards to all entities that have the power to grant patents, wherever situated, including without limitation all applications for patent which include some or all of the disclosure of, and/or claim priority to and/or the benefit of the subject matter disclosed in the invention(s) identified herein, including any provisional application, utility application, and/or design application, as well as any continuation application, divisional application, continuation-in-part application, reissue application, re-examination application, patent interference proceeding, foreign national application and/or any application filed or to be filed under a patent treaty such as the International Convention for Protection of Industrial Property and/or the Patent Cooperation Treaty, and any Letters Patent which may be granted therefor in any jurisdiction. For the avoidance of doubt, the assignments referenced herein are do not act to limit any other assignments made by Assignor to Assignee with respect to any inventions or other intellectual property not listed on Exhibit A.

In addition to the above assignment, the Assignor agrees to perform all acts required and execute all papers necessary in connection with therewith, regardless of status of the patent or patent application and any continuation applications, divisional applications, or continuations-in-part thereof, and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient to further memorialize the assignment herein of all right, title, and interest.

As to the invention(s) identified herein, to the extent that the Assignor has the power to do so, the Assignor hereby revokes all prior Powers of Attorney and grants a new Power of Attorney to each of the following individuals and hereby grants them the power to insert on this assignment any further identification which may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office or with the rules of any national or international Patent Office for recordation of this document or a true copy thereof:

Joshua Warmund, Esq., New York State Bar No. 3965050

Stephen Rudisill, Esq., USPTO Reg. No. 20,087

In connection with the foregoing, the Assignor hereby states that:

- I hereby irrevocably grant the Assignee the right to file in the future one or more patent applications based on the identified invention(s) in which I am a named inventor.
- Any patent application based on the identified invention(s) was made or authorized to be made by me.
- I believe that I may be an original inventor or an original joint inventor of a claimed invention in any such patent application.
- I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

In witness whereof, this instrument has been executed by the undersigned on the date opposite the name of the undersigned.

Assignment- Multiple Matters
Yang Liu

Date: 3/15/2018

Signature: 
Yang Liu

EITHER NOTARIZED OR WITNESSED:

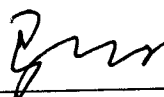
State of _____

County of _____

On this _____ day of _____, 2018, before me personally came <<Inventor>>
to me known and known to me to be the person described in and who executed the within instrument
and he/she acknowledged to me that he/she executed the same.

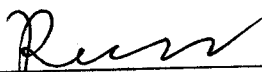
Notary Public

Witness 1:


Signature

YANGJIN MA
Printed Name

Witness 2:


Signature

Ruizhi Shi
Printed Name

EXHIBIT A

Internal Reference	Title	USPTO Serial No.
COR-002US	ULTRA-RESPONSIVE PHASE SHIFTERS FOR DEPLETION MODE SILICON MODULATORS	9,158,138
074381-000002USC1	ULTRA-RESPONSIVE PHASE SHIFTERS FOR DEPLETION MODE SILICON MODULATORS	9,638,942
074381-000002USC2	ULTRA-RESPONSIVE PHASE SHIFTERS FOR DEPLETION MODE SILICON MODULATORS	9,910,302
074381-000002USC3	ULTRA-RESPONSIVE PHASE SHIFTERS FOR DEPLETION MODE SILICON MODULATORS	15/876,856
074381-000002USP1	OPTICAL MODULATOR	15/876,623
074381-000003USPT	OPERATION AND STABILIZATION OF MOD-MUX WDM TRANSMITTERS BASED ON SILICON MICRORINGS	9,425,919
074381-000003USC1	OPERATION AND STABILIZATION OF MOD-MUX WDM TRANSMITTERS BASED ON SILICON MICRORINGS	15/217,152
074381-000003USC2	OPERATION AND STABILIZATION OF MOD-MUX WDM TRANSMITTERS BASED ON SILICON MICRORINGS	15/916,557
074381-000014USPT	INTEGRATED POLARIZATION SPLITTER AND ROTATOR INCLUDING A THIRD REGION FOR TUNING THE POLARIZATION DEPENDENT LOSS OF OUTPUT TRANSVERS ELECTRIC SIGNALS	9,874,696
074381-000014USC1	INTEGRATED POLARIZATION SPLITTER AND ROTATOR	15/840,500
074381-000016USPT	LATERAL GE/SI AVALANCHE PHOTODETECTOR	9,755,096
074381-000016USC1	LATERAL AVALANCHE PHOTODETECTOR	15/664,856
074381-000020USPT	OPTICAL HYBRID	15/659,220
074381-000034USPT	LOW LOSS HIGH EXTINCTION RATIO ON-CHIP POLARIZER	9,470,844
074381-000034USP1	INTEGRATED ON-CHIP POLARIZER	9,746,609
074381-000034USC1	INTEGRATED ON-CHIP POLARIZER	15/659,049
074381-000041USPT	OPTICAL DELAY LINES FOR ELECTRICAL SKEW COMPENSATION	14/931,796
074381- 0000101USPT	OPTICAL DUAL RESONATOR MODULATION SYSTEM AND METHOD, AND OPTICAL DUAL RESONATOR MODULATOR THEREFOR	9,787,405
074381- 0000101USC1	OPTICAL DUAL RESONATOR MODULATION SYSTEM AND METHOD, AND OPTICAL DUAL RESONATOR MODULATOR THEREFOR	15/704,895
074381-000106USPT	INTEGRATED ON-CHIP POLARIZER	9,810,840
074381-000106USC1	INTEGRATED ON-CHIP POLARIZER	15/725,450
074381-000107USPT	SHIELDED PHOTONIC INTEGRATED CIRCUIT	9,739,938
074381-000107USC1	SHIELDED PHOTONIC INTEGRATED CIRCUIT	15/659,880
074381-000121USPT	CONTROLLING BACK SCATTERING IN OPTICAL WAVEGUIDE SYSTEMS	15/481,971
074381-000124USPT	OPTICAL WAVEGUIDE MODULATOR	15/602,657
074381-000318USPT	WAVELENGTH LOCKER	15/855,242
074381-000331USPT	EXTERNAL CAVITY LASER	15/855,328
074381-000352USPT	REDUCING BACK REFLECTION IN A PHOTODIODE	15/864,714
074381-000506USC2	A COMPACT AND LOW LOSS Y-JUNCTION FOR SUBMICRON SILICON WAVEGUIDE	9,851,503
074381-000506USC3	A COMPACT AND LOW LOSS Y-JUNCTION FOR SUBMICRON SILICON WAVEGUIDE	15/825,266
074381-000115USPT	PHOTONIC-CHIP-BASED OPTICAL SPECTRUM ANALYZER	15/151,797
074381-000506USP1	METHODS FOR DESIGNING PHOTONIC DEVICES	14/858,519

Assignment- Multiple Matters

Yang Liu

074381-000506USC1	COMPACT AND LOW LOSS Y-JUNCTION FOR SUBMICRON SILICON WAVEGUIDE	14/834,597
COR-023	WAFER SCALE EDGE COUPLED SYSTEM TEST METHOD FOR SILICON PHOTONICS	UNFILED
COR-032	ON-CHIP FILTERS FOR IMPROVING OSNR	UNFILED
COR-133	METHOD FOR BIASING IQ MODULATOR USING RF POWER MONITORING	UNFILED
COR-505	LINEAR TRANSCEIVERS DESIGN	UNFILED
COR-508	ON CHIP SPECTRAL MONITORING AND CONTROL	UNFILED
COR-306	For Lasers; Ridge TM for reducing reflection; Move power splitter close to edge coupler to reduce nonlinear loss; use TM routing to reduce nonlinear loss and improve backreflection	Early Idea
COR-310	Testing actual hybrid using 2 unused ports; gc port to enable on wafer test of complex systems; In-situ phase error management of optical hybrid in coherent Tx	Early Idea
COR-314	Shorted PN junction across WG for reducing nonlinearity	Early Idea
COR-315	SiN Waveguide Bridge; SiN bridge for testing ports; adding dummy Si WG under SiN bridge to balance loss of test paths near on wafer GC test ports	Early Idea
COR-316	TWMZ bias	Early Idea
COR-317	Doped dump taper	Early Idea
COR-319	Embedded photonics kerf test set in actual chip (convene w/photonics team walk kerf structures); characterization of photonics device using integrated on chip PD (measure power imbalance of MMI)	Early Idea
COR-320	Edge coupler with angled facet; Etched facet process at SOL; using angled facet to avoid reflection; precision dicing to expose facet to fiber; facet coating for back reflection reduction w/precise dicing; on chip alignment structures to assist precision dicing saw alignment (check against 026 and 039)	Early Idea
COR-321	Asymmetrical optical power splitting between tx/rx	Early Idea
COR-322	Robust ridge to SL taper	Early Idea
COR-326	Loop back for tx testing; passive loopbacks	Early Idea
COR-341	Mode throttler + MPD for single mode detection; MPDs summing 2 tap or more inputs in one or more directions; MPD monitoring reverse direction to help fiber alignment; MPD to monitor power to help fiber alignment; may require high speed TIA to have input power to do QMPD monitoring both directions	Early Idea
COR-344	Dual input Rx PD for power handling	Early Idea
COR-346	Saturn single drive push-pull modulator; PN phase shift broken into short segments to avoid longitudinal current flow; optical delay loops; biasing network for establishing DC bias without off chip component (such as Bias-T); have isolation moat and trench; have G tie for ground plane connection (check 002 and 004 and 009)	Early Idea

PATENT

RECORDED: 09/05/2019

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