PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5819854

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
DOW SILICONES CORPORATION	09/09/2019

RECEIVING PARTY DATA

Name:	DDP SPECIALTY ELECTRONIC MATERIALS US 9, LLC
Street Address:	974 CENTRE ROAD
City:	WILMINGTON
State/Country:	DELAWARE
Postal Code:	19805

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	13745066

CORRESPONDENCE DATA

Fax Number: (302)355-4243

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 3029994278
Email: PTO-Legal.PRC@dupont.com
Correspondent Name: DUPONT DE NEMOURS INC
Address Line 1: 974 CENTRE ROAD
Address Line 2: CHESTNUT RUN PLAZA 721/2340
Address Line 4: WILMINGTON, DELAWARE 19805

ATTORNEY DOCKET NUMBER:	DIDC10449-US-CIP
NAME OF SUBMITTER:	JACKIE O'NEIL
SIGNATURE:	/Jackie O'Neil/
DATE SIGNED:	11/14/2019

Total Attachments: 12
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FORM OF
PATENT ASSIGNMENT

This PATENT ASSIGNMENT (this "Assignment"), dated as of November 1, 2018 (the "Effective Date"), is by and between Dow Silicones Corporation (f/k/a Dow Corning Corporation), a Michigan corporation ("Assignor") and DDP Specialty Electronic Materials US 9, LLC, a Delaware limited liability company ("Assignee"), (each a "Party" and collectively, the "Parties").

WHEREAS, Assignor owns the issued patents and patent applications set forth on Schedule A hereto (the foregoing, including all patents issuing from any patent applications, collectively, the "Assigned Patents"); and

WHEREAS, the Parties hereto agree that the Assignor contribute, transfer, assign and convey to the Assignee all of its right, title and interest in and to the Assigned Patents and that the Assignee accept such contribution, transfer, assignment and conveyance of such Assigned Patents;

NOW, THEREFORE, in consideration of the foregoing and the covenants and agreements contained in this Assignment, the receipt and sufficiency of which are hereby acknowledged, the Parties hereby agree as follows:

1. Conveyance. Assignor hereby assigns, transfers and conveys to Assignee all of Assignor's right, title and interest in and to the Assigned Patents, together with any and all (a) related continuations, continuations-in-part, divisionals, reissues, reexaminations, substitutions, extensions, and foreign equivalents thereof and (b) priority rights derived from any the Assigned Patents, or the items described in the foregoing subsection (a), by virtue of the International Convention for the Protection of Industrial Property and any other rights provided under applicable treaties or conventions, including rights in any and all provisional applications, together with all rights and remedies against past, present, and future infringement, misappropriation, or other violation thereof, including the right to enforce the foregoing and to sue for and recover profits and damages for any and all infringements, misappropriations or violations thereof, whether past, present or future, to the full end of the term or terms for which said patents may be granted, as fully and entirely as the same would have been held and enjoyed by Assignor without this assignment (the rights transferred under this Section 1 cumulatively, the "Assigned Rights").

2. Recordation; Further Assurances. Assignor and Assignee shall each take any and all additional actions as may be reasonably necessary to effect the transactions contemplated hereby, including Assignor's execution of individual assignment documentation prepared by Assignee at Assignee's expense for filing with the authorities of each individual country. In furtherance of the foregoing, Assignor agrees that with respect to the Assigned Patents it will enter into an assignment agreement suitable for filing with the authorities of each individual country (each an "Recordal Instrument"). The Parties agree that any Recordal Instrument shall give no greater rights or remedies in respect of the transaction completed in such Recordal

Instrument than those provided for herein and Section 4 of this Assignment shall apply to any Recordal Instrument as if fully set forth therein. As between the Parties, the responsibility to file assignments with the national patent offices of each country for the Assigned Patents shall be on the Assignee and the Assignee shall bear the cost of filing such assignments (unless, as of the Effective Date, the patent registration or application is not properly recorded in the name of the Assignor or an Affiliate of Assignor, in which case, at the request of Assignee, the Parties shall reasonably cooperate to make the necessary corrective filings and recordals of the documents that are available to them and shall split evenly any expenses in connection with the foregoing corrections and each Party shall provide any receipts and expense documentation to the other Party for the purposes of splitting such expenses).

3. Prosecution and Maintenance. For the avoidance of doubt but without limiting the obligations set forth in Section 2 hereof, as of and following the Effective Date, Assignor will have no responsibility to take any action to maintain any of the patents included in the Assigned Rights or further prosecute or seek issuance of any patent applications included in the Assigned Rights, including payment of fees, responses to any office action or other inquiries from agents of governmental entities or registrars, or otherwise.

4. No Claims. Except with respect to Section 2 of this Assignment, neither Party nor any of their respective affiliates or representatives will have, or be subject to, any liability or indemnification obligation under this Assignment to the other Party, any of its affiliates or representatives or any other entity or person resulting from, or in connection with, this Assignment or the transactions contemplated hereby. Except with respect to Section 2, each of the Parties hereby agrees (a) not to bring any claim or Action (as defined herein) under this Assignment against the other Party, its affiliates or representatives and (b) to cause its respective affiliates and representatives to comply with this Section 4. "Action" shall mean any claims, actions, suits, inquiries, proceedings or investigations by or before any governmental authority or arbitral tribunal.

5. Disclaimer of Representations and Warranties. ASSIGNEE (ON BEHALF OF ITSELF AND ITS AFFILIATES) UNDERSTANDS AND AGREES THAT NO PARTY TO THIS ASSIGNMENT IS REPRESENTING OR WARRANTING IN ANY WAY IN THIS ASSIGNMENT, AND HEREBY EXPRESSLY DISCLAIMS ALL REPRESENTATIONS AND WARRANTIES, AS TO THE ASSIGNED PATENTS AND THE OTHER ASSIGNED RIGHTS, AS TO ANY CONSENTS OR APPROVALS (INCLUDING APPROVALS FROM ANY GOVERNMENTAL ENTITIES) REQUIRED IN CONNECTION HEREWITH OR THEREWITH, AS TO THE VALUE OR FREEDOM FROM ANY SECURITY INTERESTS OF OR THE NON-INFRINGEMENT OR ABSENCE OF OTHER VIOLATION, VALIDITY OR ENFORCEABILITY OR ANY OTHER MATTER CONCERNING THE ASSIGNED PATENTS AND OTHER PATENTS AND PATENT APPLICATIONS INCLUDED IN THE ASSIGNED RIGHTS, AND ALL OF THE ASSIGNED PATENTS AND OTHER ASSIGNED RIGHTS ARE BEING TRANSFERRED ON AN "AS IS, WHERE IS" AND "WITH ALL FAULTS" BASIS.

6. Successors and Assigns. The provisions of this Assignment and the obligations and rights hereunder shall be binding upon, inure to the benefit of and be enforceable by (and against) the Parties and their respective successors and permitted transferees and assigns.

7. Counterparts. This Assignment may be executed in more than one counterpart, all of which shall be considered one and the same agreement, and shall become effective when one or more such counterparts have been signed by each of the Parties and delivered to each of the Parties.

8. Title and Headings. Titles and headings to sections herein are inserted for the convenience of reference only and are not intended to be a part of or to affect the meaning or interpretation of this Assignment.

9. Governing Law. This Assignment and any dispute arising out of, in connection with or relating to this Assignment shall be governed by and construed in accordance with the Laws of the State of Delaware, without giving effect to the conflicts of laws principles thereof.

[Signature Page Follows]

IN WITNESS WHEREOF, Assignor and Assignee have duly executed this Assignment as of the date first written above.

ASSIGNOR:

DOW SILICONES CORPORATION

By: _____
Name: Jonathan P. Wendt
Title: Secretary

THE STATE OF Michigan

County of Midland

This instrument was executed before me on this 9th day of September, 2019, by Jonathan P. Wendt, the Secretary (title) of Dow Silicones Corporation, a Michigan corporation, on behalf of said company.

Anita M. Whitney
Notary Public in and for
The State of Michigan

Anita M. Whitney
Printed or Typed Name of Notary

My commission expires October 19, 2024

Signature Page to Patent Assignment

Acknowledged and Accepted:

ASSIGNEE:

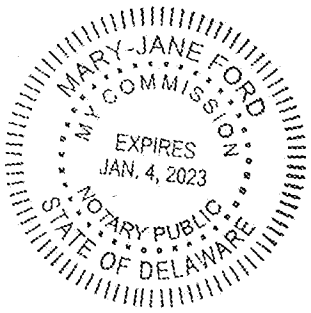
DDP SPECIALTY ELECTRONIC MATERIALS US 9, LLC

By: _____
Name: Francis X. Markey
Title: Vice President

THE STATE OF Delaware

County of New Castle

This instrument was executed before me on this 9th day of September, 2019, by Francis X. Markey, the Vice President (title) of DDP Specialty Electronic Materials US 9, LLC, a Delaware limited liability company, on behalf of said company.



_____
Notary Public in and for
The State of DELAWARE

MARY-JANE FORD
Printed or Typed Name of Notary

My commission expires JAN. 4, 2023

Signature Page to Patent Assignment

SCHEDULE A TO PATENT ASSIGNMENT

SCHEDULE A
PATENTS

Case reference	Country	Filing Date	Filing Number	Grant Date	Grant Number	Title
DIDC10449-AU-PCT	Australia	17-Jul-07	2007275780	9-Jun-11	2007275780	Method of Manufacturing Substrates Having Improved Carrier Lifetimes
DIDC10449-CN-PCT	China	17-Jul-07	200780027337.X			Method of Manufacturing Substrates Having Improved Carrier Lifetimes
DIDC10449-EP-EPT	European Procedure (Patents)	17-Jul-07	7810534.3	8-May-13	2044244	Method of Manufacturing Substrates Having Improved Carrier Lifetimes
DIDC10449-JP-DIV	Japan	17-Jul-07	2012231897			Method of Manufacturing Substrates Having Improved Carrier Lifetimes
DIDC10449-JP-DIV[2]	Japan	17-Jul-07	2014237430			Method of Manufacturing Substrates Having Improved Carrier Lifetimes
DIDC10449-US-PCT	United States Of America	17-Jul-07	12/373145			Method of Manufacturing Substrates Having Improved Carrier Lifetimes
DIDC10449-US-PSP	United States Of America	19-Jul-06	60/831839			Method of Manufacturing Substrates Having Improved Carrier Lifetimes
DIDC10449-WO-PCT	International Procedure	17-Jul-07	PCT/US07/016192			Method of Manufacturing Substrates Having Improved Carrier Lifetimes
DIDC10657-AU-PCT	Australia	8-Oct-08	2008335680			Method to Manufacture Large Uniform Ingots of Silicon Carbide by Sublimation/Condensation Processes
DIDC10657-CN-PCT	China	8-Oct-08	2.0088E+11			Method to Manufacture Large Uniform Ingots of Silicon Carbide by Sublimation/Condensation Processes
DIDC10657-EP-EPT	European Procedure (Patents)	8-Oct-08	8859709.1			Method to Manufacture Large Uniform Ingots of Silicon Carbide by Sublimation/Condensation Processes
DIDC10657-US-PSP	United States Of America	12-Dec-07	61/013083			Method to Manufacture Large Uniform Ingots of Silicon Carbide by Sublimation/Condensation Processes

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Case reference	Country	Filing Date	Filing Number	Grant Date	Grant Number	Title
DIDC10657-WO-PCT	International Procedure	8-Oct-08	PCT/US08/079126			Method to Manufacture Large Uniform Ingots of Silicon Carbide by Sublimation/Condensation Processes
DIDC10739-AU-PCT	Australia	29-May-09	2009255307			Method of Reducing Memory Effects in Semiconductor Epitaxy
DIDC10739-EP-EPT	European Procedure (Patents)	29-May-09	9759091.3			Method of Reducing Memory Effects in Semiconductor Epitaxy
DIDC10739-KR-PCT	South Korea / Republic of Korea	29-May-09	2010-7029355			Method of Reducing Memory Effects in Semiconductor Epitaxy
DIDC10739-US-PSP	United States Of America	4-Jun-08	61/058660			Method of Reducing Memory Effects in Semiconductor Epitaxy
DIDC10739-WO-PCT	International Procedure	29-May-09	PCT/US09/045551			Method of Reducing Memory Effects in Semiconductor Epitaxy
DIDC11526-EP-EPT	European Procedure (Patents)	10-Sep-13	13765897.7	26-Oct-16	2912681	Flat SiC Semiconductor Substrate
DIDC11526-JP-PCT	Japan	10-Sep-13	2015-539598			Flat SiC Semiconductor Substrate
DIDC11526-KR-PCT	South Korea / Republic of Korea	10-Sep-13	20157013789			Flat SiC Semiconductor Substrate
DIDC11526-US-PSP	United States Of America	26-Oct-12	61/719310			Flat SiC Semiconductor Substrate
DIDC11526-WO-PCT	International Procedure	10-Sep-13	PCT/US13/059064			Flat SiC Semiconductor Substrate
DIDC11578-EP-EPT	European Procedure (Patents)	10-Sep-13	13765595.7			High Voltage Power Semiconductor Devices On SiC

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Case reference	Country	Filing Date	Filing Number	Grant Date	Grant Number	Title
DIDC11578-JP-PCT	Japan	10-Sep-13	2015-510524			High Voltage Power Semiconductor Devices On SiC
DIDC11578-US-PSP	United States Of America	11-Sep-12	61/699797			High Voltage Power Semiconductor Devices On SiC
DIDC11578-WO-PCT	International Procedure	10-Sep-13	PCT/US13/058996			High Voltage Power Semiconductor Devices On SiC
DIDC11662-US-PSP	United States Of America	5-Feb-13	61/761171			SIC Crystal and Wafer Cut from Crystal with Low Dislocation Density
DIDC11662-WO-PCT	International Procedure	20-Dec-13	PCT/US13/077285			SIC Crystal and Wafer Cut from Crystal with Low Dislocation Density
DIDC11663-SE-EPT	Sweden	20-Dec-13	13818955			METHOD TO REDUCE DISLOCATIONS IN SIC CRYSTAL GROWTH
DIDC11663-US-PSP	United States Of America	5-Feb-13	61/761165			Method To Reduce Dislocations in SIC Crystal Growth
DIDC11663-WO-PCT	International Procedure	20-Dec-13	PCT/US13/077189			Method To Reduce Dislocations in SIC Crystal Growth
DIDC11664-AT-EPT	Austria	20-Dec-13	13821355.8	15-May-19	2954100	SIC Crystal With Low Dislocation Density
DIDC11664-BE-EPT	Belgium	20-Dec-13	13821355.8	15-May-19	2954100	SIC CRYSTAL WITH LOW DISLOCATION DENSITY
DIDC11664-DE-EPT	Germany	20-Dec-13	13821355.8	15-May-19	2954100	SIC Crystal With Low Dislocation Density
DIDC11664-EP-EPT	European Procedure (Patents)	20-Dec-13	13821355.8	15-May-19	2954100	SIC CRYSTAL WITH LOW DISLOCATION DENSITY

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Case reference	Country	Filing Date	Filing Number	Grant Date	Grant Number	Title
DIDC11664-FR-EPT	France	20-Dec-13	13821355.8	15-May-19	2954100	SIC Crystal With Low Dislocation Density
DIDC11664-GB-EPT	United Kingdom	20-Dec-13	13821355.8	15-May-19	2954100	SIC Crystal With Low Dislocation Density
DIDC11664-IT-EPT	Italy	20-Dec-13	13821355.8	15-May-19	2954100	SIC Crystal With Low Dislocation Density
DIDC11664-JP-PCT	Japan	20-Dec-13	2015-556014	7-Dec-18	6444890	SIC CRYSTAL WITH LOW DISLOCATION DENSITY
DIDC11664-KR-PCT	South Korea / Republic of Korea	20-Dec-13	2015-7024104			SIC Crystal With Low Dislocation Density
DIDC11664-SE-EPT	Sweden	20-Dec-13	13821355.8	15-May-19	2954100	SIC Crystal With Low Dislocation Density
DIDC11664-US-DIV	United States Of America	31-Jan-17	15/421220	23-Oct-18	10106912	SIC Crystal With Low Dislocation Density
DIDC11664-US-NP	United States Of America	9-Aug-13	13/963989	22-Aug-17	9738991	SIC Crystal With Low Dislocation Density
DIDC11664-US-PSP	United States Of America	5-Feb-13	61/761179			SIC Crystal With Low Dislocation Density
DIDC11664-WO-PCT	International Procedure	20-Dec-13	PCT/US13/077291			SIC Crystal With Low Dislocation Density
DIDC11735-EP-EPT	European Procedure (Patents)	15-Mar-14	14721146	17-May-17	2837020	SiC Substrate With SiC Epitaxial Film
DIDC11735-US-PSP	United States Of America	15-Mar-13	61/798819			SiC Substrate With SiC Epitaxial Film

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Case reference	Country	Filing Date	Filing Number	Grant Date	Grant Number	Title
DIDC11735-WO-PCT	International Procedure	15-Mar-14	PCT/US14/030022			SiC Substrate With SiC Epitaxial Film
DIDC11943-CN-PCD	China					Large Diameter Semiconductor Wafer For Integration With Power Device Manufacturing Technology
DIDC11943-US-PCT	United States Of America	29-Jul-15	PCT/US15/042590			Large Diameter Semiconductor Wafer For Integration With Power Device Manufacturing Technology
DIDC11943-US-PSP	United States Of America	29-Jul-14	62/030490			Large Diameter Semiconductor Wafer For Integration With Power Device Manufacturing Technology
DIDC11943-WO-PCT	International Procedure	29-Jul-15	PCT/US15/042590			Large Diameter Semiconductor Wafer For Integration With Power Device Manufacturing Technology
DIDC11995-AT-EPT	Austria	29-Jan-16	16707276.8	19-Dec-18	3253909	FURNACE FOR SEEDED SUBLIMATION OF WIDE BAND GAP CRYSTALS
DIDC11995-BE-EPT	Belgium	29-Jan-16	16707276.8	19-Dec-18	3253909	FURNACE FOR SEEDED SUBLIMATION OF WIDE BAND GAP CRYSTALS
DIDC11995-DE-EPT	Germany	29-Jan-16	16707276.8	19-Dec-18	3253909	FURNACE FOR SEEDED SUBLIMATION OF WIDE BAND GAP CRYSTALS
DIDC11995-FR-EPT	France	29-Jan-16	16707276.8	19-Dec-18	3253909	FURNACE FOR SEEDED SUBLIMATION OF WIDE BAND GAP CRYSTALS
DIDC11995-GB-EPT	United Kingdom	29-Jan-16	16707276.8	19-Dec-18	3253909	FURNACE FOR SEEDED SUBLIMATION OF WIDE BAND GAP CRYSTALS
DIDC11995-IT-EPT	Italy	29-Jan-16	16707276.8	19-Dec-18	3253909	FURNACE FOR SEEDED SUBLIMATION OF WIDE BAND GAP CRYSTALS
DIDC11995-SE-EPT	Sweden	29-Jan-16	16707276.8	19-Dec-18	3253909	FURNACE FOR SEEDED SUBLIMATION OF WIDE BAND GAP CRYSTALS

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Case reference	Country	Filing Date	Filing Number	Grant Date	Grant Number	Title
DIDC11995-US-PSP	United States Of America	5-Feb-15	62/112622			Furnace for Seeded Sublimation of Wide Band Gap Crystals
DIDC11995-WO-PCT	International Procedure	29-Jan-16	PCT/US16/015773			Furnace for Seeded Sublimation of Wide Band Gap Crystals