

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT5852825

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT AND ASSUMPTION OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
MORGAN STANLEY SENIOR FUNDING, INC.	12/04/2019

RECEIVING PARTY DATA

Name:	MUFG UNION BANK, N.A.
Street Address:	350 CALIFORNIA STREET
Internal Address:	17TH FLOOR
City:	SAN FRANCISCO
State/Country:	CALIFORNIA
Postal Code:	94104

PROPERTY NUMBERS Total: 141

Property Type	Number
Patent Number:	6297993
Patent Number:	6385093
Patent Number:	6567289
Patent Number:	6567303
Patent Number:	6574139
Patent Number:	6574149
Patent Number:	6768682
Patent Number:	6778437
Patent Number:	6788580
Patent Number:	6961267
Patent Number:	7174435
Patent Number:	7251161
Patent Number:	7295461
Patent Number:	7306988
Patent Number:	7319615
Patent Number:	7515478
Patent Number:	7586788
Patent Number:	7802114
Patent Number:	7847607

PATENT

Property Type	Number
Patent Number:	8117445
Patent Number:	8122204
Patent Number:	8139763
Patent Number:	8140746
Patent Number:	8190908
Patent Number:	8190919
Patent Number:	8190928
Patent Number:	8239637
Patent Number:	8239732
Patent Number:	8244964
Patent Number:	8261124
Patent Number:	8278983
Patent Number:	8291126
Patent Number:	8311054
Patent Number:	8327052
Patent Number:	8359423
Patent Number:	8443131
Patent Number:	8458393
Patent Number:	8508146
Patent Number:	8575898
Patent Number:	8635397
Patent Number:	8638140
Patent Number:	8642441
Patent Number:	8670557
Patent Number:	8725920
Patent Number:	9142301
Patent Number:	9176636
Patent Number:	9298531
Patent Number:	9305995
Patent Number:	9310953
Patent Number:	9400546
Patent Number:	9425691
Patent Number:	9455027
Patent Number:	9473144
Patent Number:	9513319
Patent Number:	9514797
Patent Number:	9514816
Patent Number:	9514833

Property Type	Number
Patent Number:	9515075
Patent Number:	9515659
Patent Number:	9520888
Patent Number:	9541990
Patent Number:	9542588
Patent Number:	9547788
Patent Number:	9548729
Patent Number:	9553588
Patent Number:	9564062
Patent Number:	9575606
Patent Number:	9577654
Patent Number:	9588626
Patent Number:	9590079
Patent Number:	9590441
Patent Number:	9590592
Patent Number:	9607695
Patent Number:	9614366
Patent Number:	9624094
Patent Number:	9625988
Patent Number:	9634667
Patent Number:	9639226
Patent Number:	9639733
Patent Number:	9640237
Patent Number:	9646661
Patent Number:	9646694
Patent Number:	9646976
Patent Number:	9652015
Patent Number:	9658632
Patent Number:	9658726
Patent Number:	9673206
Patent Number:	9679831
Patent Number:	9697312
Patent Number:	9704012
Patent Number:	9705697
Patent Number:	9721665
Patent Number:	9727123
Patent Number:	9746974
Patent Number:	9753597

Property Type	Number
Patent Number:	9766650
Patent Number:	9811135
Patent Number:	9813232
Patent Number:	9819360
Patent Number:	9831114
Patent Number:	9831864
Patent Number:	9837469
Patent Number:	9846664
Patent Number:	9858376
Patent Number:	9864607
Patent Number:	9866055
Patent Number:	9872346
Patent Number:	9880536
Patent Number:	9887178
Patent Number:	9891765
Patent Number:	9922833
Patent Number:	9923572
Patent Number:	9927915
Patent Number:	9928919
Patent Number:	9952282
Patent Number:	9972146
Patent Number:	9977551
Patent Number:	10013593
Patent Number:	10020810
Patent Number:	10033403
Patent Number:	10068121
Patent Number:	10116307
Patent Number:	10141393
Patent Number:	10165425
Patent Number:	10185867
Patent Number:	10303625
Patent Number:	10360985
Patent Number:	10380397
Patent Number:	10429998
Application Number:	13073691
Application Number:	13682826
Application Number:	13901167
Application Number:	14445364

Property Type	Number
Application Number:	14868296
Application Number:	14714118
Application Number:	15048886
Application Number:	15012644
Application Number:	15088855
Application Number:	14866168
Application Number:	15686011
Application Number:	15476758

CORRESPONDENCE DATA

Fax Number: (212)735-2000
Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 2127353000
Email: jselle@skadden.com
Correspondent Name: SKADDEN, ARPS, SLATE, MEAGHER & FLOM LLP
Address Line 1: FOUR TIMES SQUARE
Address Line 2: JUSTIN C. SELLE
Address Line 4: NEW YORK, NEW YORK 10036

ATTORNEY DOCKET NUMBER:	127110/12
NAME OF SUBMITTER:	SHAYA AFSHAR
SIGNATURE:	/shaya afshar/
DATE SIGNED:	12/05/2019

Total Attachments: 8
source=Cypress - Assignment and Assumption of Security Interest in Intellectual Property (12.4.2019) (Execution)#page1.tif
source=Cypress - Assignment and Assumption of Security Interest in Intellectual Property (12.4.2019) (Execution)#page2.tif
source=Cypress - Assignment and Assumption of Security Interest in Intellectual Property (12.4.2019) (Execution)#page3.tif
source=Cypress - Assignment and Assumption of Security Interest in Intellectual Property (12.4.2019) (Execution)#page4.tif
source=Cypress - Assignment and Assumption of Security Interest in Intellectual Property (12.4.2019) (Execution)#page5.tif
source=Cypress - Assignment and Assumption of Security Interest in Intellectual Property (12.4.2019) (Execution)#page6.tif
source=Cypress - Assignment and Assumption of Security Interest in Intellectual Property (12.4.2019) (Execution)#page7.tif
source=Cypress - Assignment and Assumption of Security Interest in Intellectual Property (12.4.2019) (Execution)#page8.tif

**ASSIGNMENT AND ASSUMPTION OF SECURITY INTEREST IN
INTELLECTUAL PROPERTY**

This ASSIGNMENT AND ASSUMPTION OF SECURITY INTEREST IN INTELLECTUAL PROPERTY dated as of December 4, 2019, and effective as of July 31, 2019 (the “**Effective Date**”) (this “**Assignment and Assumption**”) is made by and between MORGAN STANLEY SENIOR FUNDING, INC. (“**MSSF**”) and MUFG UNION BANK, N.A. (“**Union Bank**”) as collateral agent for the Secured Parties.

WHEREAS, Cypress Semiconductor Corporation (“**Borrower**”), the Guarantors, the Lenders from time to time party thereto, MSSF, as administrative agent and collateral agent for the Lenders and the other Agents from time to time party thereto, and Morgan Stanley Bank, N.A., an Issuing Bank, entered into that certain Amended and Restated Credit and Guaranty Agreement dated as of March 12, 2015 (as further amended, restated, amended and restated, supplemented or otherwise modified from time to time, the “**Credit Agreement**”);

WHEREAS, pursuant to the Credit Agreement, Borrower and MSSF, together with any Additional Grantors, entered into that certain Amended and Restated Pledge and Security Agreement, dated as of March 12, 2015 (as further amended, restated, amended and restated, supplemented or otherwise modified from time to time, the “**Security Agreement**”; capitalized terms not otherwise defined herein shall have the meaning ascribed to them in the Security Agreement);

WHEREAS, pursuant to the Security Agreement, the Grantors or Additional Grantors, as applicable, executed and delivered to MSSF: (i) that certain Patent Security Agreement dated as of March 12, 2015, (ii) that certain Patent Security Agreement dated as of August 5, 2016, (iii) that certain Patent Security Agreement dated as of April 21, 2017 and (iv) that certain Patent Security Agreement dated as of June 20, 2018, each as further amended, restated, amended and restated, supplemented or otherwise modified from time to time, by and between each Grantor party thereto (or each Additional Grantor party thereto) and MSSF (collectively, the “**Patent Security Agreements**”), which were respectively recorded with the United States Patent and Trademark Office on, on March 21, 2015 at Reel/Frame 035240/0429, on August 15, 2016 at Reel/Frame 039676/0237, on April 25, 2017 at Reel/Frame 042326/0396 and on June 21, 2018 at Reel/Frame 046402/0277;

WHEREAS, pursuant to the Security Agreement and subject to the Patent Security Agreements, the Grantors or Additional Grantors, as applicable, executed and delivered to MSSF a security interest in and Lien on all of Grantors’ or Additional Grantors’ right, title and interest in the Patents set forth in Schedule 1 (the “**Patent Collateral**”);


WHEREAS, pursuant to that certain Agency Resignation and Appointment Agreement and Amendment No. 9 to Amended and Restated Credit and Guaranty Agreement, dated as of the date hereof (the “**Amendment**”), MSSF has resigned as Administrative Agent and Collateral Agent and has appointed MUFG Bank, Ltd. as the successor Administrative Agent and Union Bank as the successor Collateral Agent pursuant to Section 10.07 of the Credit Agreement.

NOW THEREFORE, in consideration of the foregoing premises and other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, each of the parties hereto agree, subject to the terms and conditions set forth in the Amendment, as follows:

1. MSSF hereby irrevocably, absolutely and unconditionally assigns to Union Bank, and Union Bank hereby assumes from MSSF, all of MSSF's right, title and interest in and to, and MSSF's obligations under, the Patent Security Agreements, as of the Effective Date, and in connection therewith, the security interest in and Lien on all of MSSF's right, title and interest in, to and under all Patent Collateral;
2. This Assignment and Assumption and the rights and obligations of the parties hereunder shall be governed by, and construed and enforced in accordance with the law of the state of New York without regard to conflict of law principles that would result in the application of any law other than the law of the state of New York. The terms and provisions of Section 9.13 of the Security Agreement are incorporated by reference herein with respect hereto as if fully set forth herein.

[Remainder of Page Intentionally Blank]

MORGAN STANLEY SENIOR FUNDING, INC.

By 
Name: Lisa Hanson
Title: Vice President

ACCEPTED AND AGREED:
MUFG UNION BANK, N.A., as Collateral Agent

By 
Name: Keith Sevigny
Title Vice President

[Signature Page to Assignment and Assumption of Security Interest in Intellectual Property]

Schedule 1

Patents

Title	App. No.	File Date	Patent No.	Issue Date
Acceleration voltage implementation for a high density flash memory device	09/712382	11/13/2000	6297993	10/2/2001
I/o partitioning system and methodology to reduce band-to-band tunneling current during erase	09/822995	3/30/2001	6385093	5/7/2002
Physical memory layout with various sized memory sectors	09/644359	8/23/2000	6567289	5/20/2003
Charge injection	10/050483	1/16/2002	6567303	5/20/2003
Method and device for reading dual bit memory cells using multiple reference cells with two side read	10/052484	1/18/2002	6574139	6/3/2003
Semiconductor memory and its usage	10/097924	3/15/2002	6574149	6/3/2003
Nonvolatile semiconductor memory and method for controlling programming voltage of nonvolatile semiconductor memory	10/259761	9/30/2002	6768682	7/27/2004
Memory circuit for providing word line redundancy in a memory sector	10/635974	8/7/2003	6778437	8/17/2004
Nonvolatile semiconductor storage device and data erasing method	10/454630	6/5/2003	6788580	9/7/2004
Method and device for programming cells in a memory array in a narrow distribution	10/738301	12/16/2003	6961267	11/1/2005
Memory control circuit, memory device, and microcomputer	10/715366	11/19/2003	7174435	2/6/2007
Semiconductor device and method of controlling said semiconductor device	11/290001	11/30/2005	7251161	7/31/2007
Memory device with a self-assembled polymer film and method of making the same	10/958044	10/4/2004	7295461	11/13/2007
Memory cell and method of making the memory cell	11/063138	2/22/2005	7306988	12/11/2007
Ramp gate erase for dual bit flash memory	11/497597	8/2/2006	7319615	1/15/2008
Cmos logic compatible non-volatile memory cell structure, operation, and array configuration	11/841468	8/20/2007	7515478	4/7/2009
Nonvolatile semiconductor memory having voltage adjusting circuit	11/607090	12/1/2006	7586788	9/8/2009
State change sensing	11/687487	3/16/2007	7802114	9/21/2010
PLL circuit	11/987003	11/26/2007	7847607	12/7/2010
Near field communication, security and non-volatile memory integrated sub-system for embedded portable applications	11/613620	12/20/2006	8117445	2/14/2012
Shadow write and transfer schemes for memory devices	12/137443	6/11/2008	8122204	2/21/2012
Randomized rsa-based cryptographic exponentiation resistant to side channel and fault attacks	11/870102	10/10/2007	8139763	3/20/2012
Intelligent memory data management	11/957226	12/14/2007	8140746	3/20/2012
Secure data verification via biometric input	11/613627	12/20/2006	8190908	5/29/2012
Multiple stakeholder secure memory partitioning and access control	11/613691	12/20/2006	8190919	5/29/2012
Power-on detection circuit and microcontroller	12/392674	2/25/2009	8190928	5/29/2012
Byte mask command for memories	11/625158	1/19/2007	8239637	8/7/2012
Error correction coding in flash memory devices	11/928434	10/30/2007	8239732	8/7/2012
Read preamble for data capture optimization	12/646279	12/23/2009	8244964	8/14/2012
System and method for optimized error correction in flash memory arrays	11/963078	12/21/2007	8261124	9/4/2012
PLL circuit	12/917219	11/1/2010	8278983	10/2/2012
Variable read latency on a serial memory bus	12/729905	3/23/2010	8291126	10/16/2012
Transmitting/receiving system, node and communication method	12/410086	3/24/2009	8311054	11/13/2012

Title	App. No.	File Date	Patent No.	Issue Date
Variable read latency on a serial memory bus	12/646291	12/23/2009	8327052	12/4/2012
Using lppdr1 bus as transport layer to communicate to flash	12/048474	3/14/2008	8359423	1/22/2013
Non-volatile memory device	11/259874	10/26/2005	8443131	5/14/2013
Flash memory and operating system kernel	12/059816	3/31/2008	8458393	6/4/2013
Electronic device, control circuit, and method for controlling light emitting element	13/305684	11/28/2011	8508146	8/13/2013
Charging circuit, charging apparatus, electronic equipment and charging method	12/697879	2/1/2010	8575898	11/5/2013
Data writing method and system	13/070186	3/23/2011	8635397	1/21/2014
PLL circuit	13/558835	7/26/2012	8638140	1/28/2014
Self-aligned sti with single poly for manufacturing a flash memory device	11/639667	12/15/2006	8642441	2/4/2014
Cryptographic system with modular randomization of exponentiation	11/852644	9/10/2007	8670557	3/11/2014
Variable read latency on a serial memory bus	13/668935	11/5/2012	8725920	5/13/2014
Data writing method and system	14/149484	1/7/2014	9142301	9/22/2015
Low power capacitive sensor button	14/667434	3/24/2015	9176636	11/3/2015
Watchdog timer with mode dependent time out	14/635361	3/2/2015	9298531	3/29/2016
Methods of fabricating an f-ram	14/738492	6/12/2015	9305995	4/5/2016
Full-wave synchronous rectification for self-capacitance sensing	14/736811	6/11/2015	9310953	4/12/2016
Low-power implementation of type-c connector subsystem	14/866276	9/25/2015	9400546	7/26/2016
Low thermal design for dc-dc converter	14/866172	9/25/2015	9425691	8/23/2016
Power management system for high traffic integrated circuit	14/822085	8/10/2015	9455027	9/27/2016
Integrated circuit device with programmable analog subsystem	14/670295	3/26/2015	9473144	10/18/2016
Systems, methods, and devices for energy and power metering	14/866225	9/25/2015	9513319	12/6/2016
Hybrid reference generation for ferroelectric random access memory	15/179070	6/10/2016	9514797	12/6/2016
Non-volatile static ram and method of operation thereof	14/864594	9/24/2015	9514816	12/6/2016
Supply power dependent controllable write throughput for memory applications	14/930484	11/2/2015	9514833	12/6/2016
Method for fabricating ferroelectric random-access memory on pre-patterned bottom electrode and oxidation barrier	15/065410	3/9/2016	9515075	12/6/2016
Programmable input/output circuit	14/690106	4/17/2015	9515659	12/6/2016
Integrated circuit device with on-board calibration of signal generator circuits, and related methods	15/087573	3/31/2016	9520888	12/13/2016
Asynchronous transceiver for on-vehicle electronic device	14/865676	9/25/2015	9541990	1/10/2017
Capacitive fingerprint sensor with quadrature demodulator and multiphase scanning	14/672036	3/27/2015	9542588	1/10/2017
Fingerprint sensor-compatible overlay	15/088479	4/1/2016	9547788	1/17/2017
Switching circuit	14/866193	9/25/2015	9548729	1/17/2017
System level interconnect with programmable switching	14/968247	12/14/2015	9553588	1/24/2017
Body position sensing for equipment	14/970297	12/15/2015	9564062	2/7/2017
Reducing sleep current in a capacitance sensing system	14/606767	1/27/2015	9575606	2/21/2017
Analog-digital converter and control method	14/977598	12/21/2015	9577654	2/21/2017
Capacitive sensing button on chip	14/632191	2/26/2015	9588626	3/7/2017
Use disposable gate cap to form transistors, and split gate charge trapping memory cells	14/742201	6/17/2015	9590079	3/7/2017
Multi-standard compliant usb battery charging scheme with detection of host disconnection in aca-dock mode	14/750555	6/25/2015	9590441	3/7/2017
Configurable capacitor arrays and switched capacitor circuits	14/752052	6/26/2015	9590592	3/7/2017
Multi-bit non-volatile random-access memory cells	15/079462	3/24/2016	9607695	3/28/2017
Protecting circuit and integrated circuit	15/082882	3/28/2016	9614366	4/4/2017

Title	App. No.	File Date	Patent No.	Issue Date
Hydrogen barriers in a copper interconnect process	15/088557	4/1/2016	9624094	4/18/2017
Type-c connector subsystem	15/196921	6/29/2016	9625988	4/18/2017
Integrated circuit device with programmable analog subsystem	14/668984	3/26/2015	9634667	4/25/2017
Differential sigma-delta capacitance sensing devices and methods	14/965165	12/10/2015	9639226	5/2/2017
Methods and sensors for multiphase scanning in the fingerprint and touch applications	14/671129	3/27/2015	9639733	5/2/2017
Access methods and circuits for memory devices having multiple channels and multiple banks	14/866260	9/25/2015	9640237	5/2/2017
Memory device with internal combination logic	15/052709	2/24/2016	9646661	5/9/2017
10-transistor non-volatile static random-access memory using a single non-volatile memory element and method of operation thereof	14/886663	10/19/2015	9646694	5/9/2017
Ferroelectric random-access memory with pre-patterned oxygen barrier	14/970063	12/15/2015	9646976	5/9/2017
Low-power touch button sensing system	14/971728	12/16/2015	9652015	5/16/2017
Systems, methods, and devices for bootstrapped power circuits	14/668670	3/25/2015	9658632	5/23/2017
Single layer sensor pattern	14/740170	6/15/2015	9658726	5/23/2017
Buried hard mask for embedded semiconductor device patterning	15/133026	4/19/2016	9673206	6/6/2017
Tape chip on lead using paste die attach material	14/970872	12/16/2015	9679831	6/13/2017
Integrated circuit including parametric analog elements	14/606661	1/27/2015	9697312	7/4/2017
Fingerprint sensor pattern	14/977267	12/21/2015	9704012	7/11/2017
Transceiver for communication and method for controlling communication	15/198928	6/30/2016	9705697	7/11/2017
Data writing method and system	14/860035	9/21/2015	9721665	8/1/2017
Configurable and power-optimized integrated gate-driver for usb power-delivery and type-c socs	15/200538	7/1/2016	9727123	8/8/2017
Providing a baseline capacitance for a capacitance sensing channel	14/670345	3/26/2015	9746974	8/29/2017
Mutual capacitance sensing array	14/830624	8/19/2015	9753597	9/5/2017
Microcontroller programmable system on a chip with programmable interconnect	14/866439	9/25/2015	9766650	9/19/2017
Low-power type-c receiver with high idle noise and dc-level rejection	14/977589	12/21/2015	9811135	11/7/2017
Device and method for resisting non-invasive attacks	14/659924	3/17/2015	9813232	11/7/2017
Ratio-metric self-capacitance-to-code convertor	15/199559	6/30/2016	9819360	11/14/2017
Self-aligned trench isolation in integrated circuits	15/191882	6/24/2016	9831114	11/28/2017
Programmable switched capacitor block	14/865999	9/25/2015	9831864	11/28/2017
Resistive memory array using p-i-n diode select device and methods of fabrication thereof	15/197099	6/29/2016	9837469	12/5/2017
Rfid interface and interrupt	14/645798	3/12/2015	9846664	12/19/2017
Tool and method for refining a circuit including parametric analog elements	14/865163	9/25/2015	9858376	1/2/2018
Methods and physical computer-readable storage media for initiating re-enumeration of usb 3.0 compatible devices	14/675128	3/31/2015	9864607	1/9/2018
Automatic scheme to detect multi-standard charger types	14/974804	12/18/2015	9866055	1/9/2018
Phase controller apparatus and methods	14/865722	9/25/2015	9872346	1/16/2018
Autonomous control in a programmable system	14/865824	9/25/2015	9880536	1/30/2018
Semiconductor device and method of manufacturing the same	15/007052	1/26/2016	9887178	2/6/2018
Method and apparatus for data transmission via capacitance sensing device	14/609274	1/29/2015	9891765	2/13/2018

Title	App. No.	File Date	Patent No.	Issue Date
Charge trapping split gate embedded flash memory and associated methods	14/971531	12/16/2015	9922833	3/20/2018
Delta modulator receive channel for capacitance measurement circuits	15/087625	3/31/2016	9923572	3/20/2018
Optical navigation systems and methods for background light detection and avoiding false detection and auto-movement	14/858217	9/18/2015	9927915	3/27/2018
Method and apparatus for staggered start-up of a predefined, random, or dynamic number of flash memory devices	14/716719	5/19/2015	9928919	3/27/2018
Combined analog architecture and functionality in a mixed-signal array	14/860515	9/21/2015	9952282	4/24/2018
Security system with a wireless security device	14/751559	6/26/2015	9972146	5/15/2018
Capacitance to code converter with sigma-delta modulator	14/832529	8/21/2015	9977551	5/22/2018
Multiphase fingerprint sensor layout and construction	14/964562	12/9/2015	10013593	7/3/2018
Psoc architecture	14/976580	12/21/2015	10020810	7/10/2018
Integrated circuit device with reconfigurable digital filter circuits	14/736488	6/11/2015	10033403	7/24/2018
Baseline compensation for capacitive sensing	15/084363	3/29/2016	10068121	9/4/2018
Low power capacitive sensor button	14/865288	9/25/2015	10116307	10/30/2018
Three dimensional capacitor	15/060249	3/3/2016	10141393	11/27/2018
Dynamically switching communication modes in multi-standard wireless communication devices	14/855158	9/15/2015	10165425	12/25/2018
Pressure detection and measurement with a fingerprint sensor	15/199444	6/30/2016	10185867	1/22/2019
Variable read latency on a serial memory bus	14/228384	3/28/2014	10303625	5/28/2019
Method and apparatus for staggered start-up of a predefined, random, or dynamic number of flash memory devices	15/198235	6/30/2016	10360985	7/23/2019
Half-bridge fingerprint sensing method	14/978442	12/22/2015	10380397	8/13/2019
Generating a baseline compensation signal based on a capacitive circuit	14/752687	6/26/2015	10429998	10/1/2019
Reconfigurable circuit using valid signals and method of operating reconfigurable circuit	13/073691	3/28/2011		
Inter-layer insulator for electronic devices and apparatus for forming same	13/682826	11/21/2012		
Differential file system for computer memory	13/901167	5/23/2013		
Techniques for generating microcontroller configuration information	14/445364	7/29/2014		
Computer system including reconfigurable arithmetic device with network of processor elements	14/868296	9/28/2015		
Systems, methods, and devices for touch event and hover event detection	14/714118	5/15/2015		
Lateral charge storage region formation for semiconductor wordline	15/048886	2/19/2016		
Buried trench isolation in integrated circuits	15/012644	2/1/2016		
Integrated circuits with non-volatile memory and methods for manufacture	15/088855	4/1/2016		
Fingerprint sensing access for security and personalization in apps and devices	14/866168	9/25/2015		
System for re-enumeration of usb 3.0 compatible peripheral devices	15/686011	8/24/2017		
Embedded certificate method for strong authentication and ease of use for wireless iot systems	15/476758	3/31/2017		