PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5863915

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
VERIMATRIX	11/13/2019

RECEIVING PARTY DATA

Name:	Rambus Inc.
Street Address:	1050 Enterprise Way, Suite 700
City:	Sunnyvale
State/Country:	CALIFORNIA
Postal Code:	94089

PROPERTY NUMBERS Total: 99

Property Type	Number
Patent Number:	8457919
Patent Number:	8572406
Patent Number:	8301890
Patent Number:	7644322
Patent Number:	8997255
Patent Number:	7984301
Patent Number:	8028015
Patent Number:	8213612
Patent Number:	7774587
Patent Number:	6718536
Patent Number:	7392276
Patent Number:	8793300
Patent Number:	8959134
Patent Number:	9577826
Patent Number:	9977899
Patent Number:	8369517
Patent Number:	8549218
Patent Number:	8006045
Patent Number:	8233620
Patent Number:	8352752

Property Type	Number
Patent Number:	7845568
Patent Number:	8559625
Patent Number:	8233615
Patent Number:	8619977
Patent Number:	7895404
Patent Number:	8327100
Patent Number:	8301905
Patent Number:	7809133
Patent Number:	7805480
Patent Number:	7791898
Patent Number:	7848515
Patent Number:	7672990
Patent Number:	7788311
Patent Number:	7822207
Patent Number:	8280041
Patent Number:	8024391
Patent Number:	9430650
Patent Number:	9621550
Patent Number:	9268559
Patent Number:	9596080
Patent Number:	9405729
Patent Number:	9772821
Patent Number:	6678734
Patent Number:	6807553
Patent Number:	6856981
Patent Number:	7054894
Patent Number:	7200759
Patent Number:	7240040
Patent Number:	7302487
Patent Number:	7305391
Patent Number:	9043272
Patent Number:	7461370
Patent Number:	7505473
Patent Number:	7548992
Patent Number:	9594541
Patent Number:	8566920
Patent Number:	9780946
Application Number:	15463364

Property Type	Number
Application Number:	15808362
Application Number:	15784007
Application Number:	15784010
Application Number:	15594122
Patent Number:	10303903
Patent Number:	8243925
Patent Number:	9014375
Patent Number:	9712786
Patent Number:	7970138
Patent Number:	8879729
Patent Number:	8761393
Patent Number:	8281359
Patent Number:	8151235
Patent Number:	8418091
Patent Number:	9355199
Patent Number:	8111089
Patent Number:	9355426
Patent Number:	9942586
Patent Number:	10277935
Patent Number:	8510700
Patent Number:	9542520
Patent Number:	9940425
Patent Number:	9800405
Patent Number:	9277259
Patent Number:	9735781
Application Number:	15675418
Patent Number:	10348501
Application Number:	16505477
Application Number:	16333589
Patent Number:	10476883
Patent Number:	10477151
Application Number:	16670912
Application Number:	16670957
PCT Number:	US2018042542
Application Number:	16056268
Application Number:	16552919
Application Number:	16297511
Application Number:	16297516

Property Type	Number
Application Number:	16363958
Application Number:	16364056
Application Number:	16681465

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone:	408-462-8000
Email:	annw@rambus.com
Correspondent Name:	ANN WILLIAMS
Address Line 1:	1050 ENTERPRISE WAY #700
Address Line 4:	SUNNYVALE, CALIFORNIA 94089

ATTORNEY DOCKET NUMBER:	VERIMATRIX ACQUSITION
NAME OF SUBMITTER:	ANN C WILLIAMS
SIGNATURE:	/Ann C Williams/
DATE SIGNED:	12/12/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 40

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PATENT ASSIGNMENT

THIS PATENT ASSIGNMENT (this "Patent Assignment") from Verimatrix, a *société anonyme* incorporated under the laws of the Republic of France ("Assignor") to Rambus Inc., a Delaware corporation ("Assignee"), is effective as of December 6, 2019.

WHEREAS, Assignor and Assignee have entered into an Asset Purchase Agreement, dated as of September 11, 2019 (the "Purchase Agreement"), pursuant to which, among other things, Assignor has agreed to assign to Assignee all of Assignor's right, title and interest in and to the Assigned Patents (as defined below).

NOW, THEREFORE, in consideration of the premises and the mutual covenants and agreements contained in this Patent Assignment and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties hereto, intending to be legally bound, agree as follows:

1. <u>Assigned Patents</u>. The term "Assigned Patents" means the issued patents, pending patent applications and certificates of invention set forth on <u>Schedule A</u>, attached hereto.

2. <u>Assignment</u>. Assignor hereby irrevocably assigns, transfers, sells and delivers to Assignee all of Assignor's right, title and interest in and to (i) the Assigned Patents and the inventions and improvements disclosed therein; (ii) all reissues, divisionals, continuations, continuations-in-part, extensions, renewals, reexaminations and foreign counterparts thereof; (iii) all patents and applications which claim priority to or are linked by terminal disclaimer to any such patents or patent applications; and (iv) all rights corresponding to any of the foregoing throughout the world, including the right to claim priority from any of the Assigned Patents, the right to prosecute and maintain any of the Assigned Patents, and the right to sue, claim remedies and recover damages for past, present and future infringement or other violation or impairment of any of the Assigned Patents, the same to be held and enjoyed by Assignee for its own use and enjoyment, and for the use and enjoyment of its successors, assigns and other legal representatives, as fully and entirely as the same would have been held and enjoyed by Assignor, if this assignment and sale had not been made.

3. <u>No Warranties</u>. EXCEPT AS EXPRESSLY SET FORTH IN THE PURCHASE AGREEMENT, NO EXPRESS OR IMPLIED WARRANTIES ARE GIVEN BY ASSIGNOR OR ITS WITH RESPECT TO ANY ASSIGNED PATENTS OR ANY OTHER MATTER OR SUBJECT ARISING OUT OF THIS PATENT ASSIGNMENT, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ANY IMPLIED WARRANTY ARISING OUT OF COURSE OF DEALING OR USAGE OF TRADE, OR REGARDING THE VALIDITY, REGISTRABILITY, TITLE SCOPE, ENFORCEABILITY OR NON-INFRINGEMENT OF ANY PATENTS SUBJECT TO THIS PATENT ASSIGNMENT.

4. <u>Further Assurances</u>. Assignor agrees that Assignee shall have the right to file or record this Patent Assignment with the United States Patent and Trademark Office or other such entities throughout the world, and Assignor authorizes and requests the relevant authorities to record Assignee as the assignee and owner of the Assigned Patents. Assignor shall execute and

**PATENT
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deliver to Assignee such documents and take such actions as reasonably requested by Assignee and at Assignee's sole expense, to register, evidence or perfect Assignee's rights under this Patent Assignment.

     5.   <u>Governing Law</u>. This Patent Assignment shall be governed by, and construed in accordance with, the laws of the State of Delaware, regardless of the laws that might otherwise govern under applicable principles of choice or conflicts of law thereof.

[The remainder of this page is intentionally left blank; signature page follows.]

IN WITNESS WHEREOF, Assignor has caused this Patent Assignment to be executed as of the date first written above by its duly authorized officer.

ASSIGNOR:

Verimatrix

By: _~~signature~~_
Name: _Amedeo D'Angelo_
Title: _C.E.O._

ACKNOWLEDGMENT

State of New York   )
) ss:
County of _New York_   )

On this _13th_ day of _November_, _2019_ before me, the undersigned, personally appeared _Amedeo D'Angelo_, personally known to me or proved to me on the basis of satisfactory evidence to be the person who executed this instrument on behalf of the corporation named herein, and acknowledged that s/he executed it in such representative capacity.

IN WITNESS WHEREOF, I have hereunto set my hand and official seal.

~~signature~~
Notary Public

My Commission Expires on _12.06.21_

[SIGNATURE PAGE TO PATENT ASSIGNMENT]

SCHEDULE A
ASSIGNED PATENTS

Country	Title	Application Number/ Patent Number	Filing Date	File Number	Issue Date	Owner/ Assignee	Status
FR	Method and Devices for Protecting a Microcircuit From Attacks for Obtaining Secret Data	2,923,305	2-Nov-07	0707695	29-Apr-11	Verimatrix	Granted
DE	Method and Devices for Protecting a Microcircuit From Attacks for Obtaining Secret Data	2,215,768	3-Nov-08	08871332.6	21-Aug-19	Verimatrix	Granted
FR	Method and Devices for Protecting a Microcircuit From Attacks for Obtaining Secret Data	2,215,768	3-Nov-08	08871332.6	21-Aug-19	Verimatrix	Granted
GB	Method and Devices for Protecting a Microcircuit From Attacks for Obtaining Secret Data	2,215,768	3-Nov-08	08871332.6	21-Aug-19	Inside Secure	Granted
FR	Countermeasure Method and Devices for Asymmetric Encryption	2,926,651	23-Jan-08	0800344	21-May-10	Verimatrix	Granted
FR	Countermeasure Method and Devices for Asymmetric Encryption With Signature Scheme	2,926,652	23-Jan-08	0800345	18-Jun-10	Verimatrix	Granted

Country	Title	Patent Number	Filing Date	Application Number	Grant Date	Assignee	Status
CN	Countermeasure Method and Devices for Asymmetric Encryption With Signature Scheme	101911009	23-Jan-09	200980102305.0	10-Oct-12	Inside Secure	Granted
CA	Process for Testing the Resistance of an Integrated Circuit to a Side Channel Analysis	2,732,651	24-Feb-11	2732651	30-May-17	Verimatrix	Granted
CN	Process for Testing the Resistance of an Integrated Circuit to a Side Channel Analysis	ZL201110049399.9	1-Mar-11	201110049399.9	6-May-15	Inside Secure	Granted
KR	Process for Testing the Resistance of an Integrated Circuit to a Side Channel Analysis	10-1792650	2-Mar-11	10-2011-0018644	26-Oct-17	Inside Secure	Granted
US	Process for Testing the Resistance of an Integrated Circuit to a Side Channel Analysis	8,457,919	31-Mar-10	12/750 846	4-Jun-13	Verimatrix	Granted
DE	Process for Testing the Resistance of an Integrated Circuit to a Side Channel Analysis	2,365,659	21-Feb-11	11001428.9	12-Apr-17	Verimatrix	Granted
FR	Process for Testing the Resistance of an Integrated Circuit to a Side Channel Analysis	2,365,659p	21-Feb-11	11001428.9	12-Apr-17	Verimatrix	Granted

Country	Title	Number	Date	Application No.	Date	Owner	Status
GB	Process for Testing the Resistance of an Integrated Circuit to a Side Channel Analysis	2,365,659	21-Feb-11	11001428.9	12-Apr-17	Inside Secure	Granted
FR	Integrated Circuit Protected Against Horizontal Side Channel Analysis		1-Mar-10	1000834		Verimatrix	Published
CA	Integrated Circuit Protected Against Horizontal Side Channel Analysis		24-Feb-11	2732444		Verimatrix	Allowance
EP	Integrated Circuit Protected Against Horizontal Side Channel Analysis		23-Feb-11	11001491.7		Verimatrix	Allowance
US	Integrated Circuit Protected Against Horizontal Side Channel Analysis	8,572,406	31-Mar-10	12/750 953	29-Oct-13	Verimatrix	Granted
DE	Encryption Method Comprising an Exponentiation Operation	2,492,804	8-Feb-12	121544466.2	4-Sep-13	Verimatrix	Granted
FR	Encryption Method Comprising an Exponentiation Operation	2,492,804	8-Feb-12	121544466.2	4-Sep-13	Verimatrix	Granted
GB	Encryption Method Comprising an Exponentiation Operation	2,492,804	8-Feb-12	121544466.2	4-Sep-13	Inside Secure	Granted
US	SOFTWARE EXECUTION RANDOMIZATION	8,301,890	10-Aug-06	11501968	30-Oct-12	Verimatrix	Granted

Country	Title	Number	Date	Application No.	Date	Owner	Status
TW	SOFTWARE EXECUTION RANDOMIZATION	1449392	8-Aug-07	96129254	11-Aug-14	Inside Secure	Granted
US	HARDWARE FLOW CONTROL MONITOR	7,644,322	21-Nov-06	11/562 280	5-Jan-10	Verimatrix	Granted
TW	HARDWARE FLOW CONTROL MONITOR	1431526	20-Nov-07	96143994	21-Mar-14	Inside Secure	Granted
US	Verifying Data Integrity in a Data Storage Device	8,997,255	7-Sep-06	11/516 846	31-Mar-15	Inside Secure	Granted
KR	Verifying Data Integrity in a Data Storage Device	10-1484331	17-Jan-07	10-2009-7004354	13-Jan-15	Inside Secure	Granted
US	BI-PROCESSOR ARCHITECTURE FOR SECURE SYSTEMS	7,984,301	9-Nov-06	11558367	19-Jul-11	Verimatrix	Granted
TW	BI-PROCESSOR ARCHITECTURE FOR SECURE SYSTEMS	1431502	16-Aug-07	961303344	21-Mar-14	Inside Secure	Granted
DE	BI-PROCESSOR ARCHITECTURE FOR SECURE SYSTEMS	2,052,344	14-Aug-07	07868330.7	27-Sep-17	Verimatrix	Granted
FR	BI-PROCESSOR ARCHITECTURE FOR SECURE SYSTEMS	2,052,344	14-Aug-07	07868330.7	27-Sep-17	Verimatrix	Granted
GB	BI-PROCESSOR ARCHITECTURE FOR SECURE SYSTEMS	2,052,344	14-Aug-07	07868330.7	27-Sep-17	Inside Secure	Granted

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Country	Title	Number	Filing Date	Application Number	Grant Date	Owner	Status
CN	BI-PROCESSOR ARCHITECTURE FOR SECURE SYSTEMS	ZL200780030561.4	14-Aug-07	200780030561.4	9-May-12	Inside Secure	Granted
KR	BI-PROCESSOR ARCHITECTURE FOR SECURE SYSTEMS	10-1460811	14-Aug-07	10-2009-7005441	5-Nov-14	Inside Secure	Granted
US	Method and System for Large Number Multiplication	8,028,015	10-Aug-07	11837387	27-Sep-11	Inside Secure	Granted
TW	Method and System for Large Number Multiplication	I438678	8-Aug-08	97130432	21-May-14	Inside Secure	Granted
CN	Method and System for Large Number Multiplication	ZL 200880102372.8	8-Aug-08	200880102372.8	6-Nov-13	Inside Secure	Granted
DE	Method and System for Large Number Multiplication		8-Aug-08	11 2008 002 158.9		Verimatrix	Published
US	Secure Software Download	8,213,612	7-Dec-07	11/952 880	3-Jul-12	Verimatrix	Granted
TW	Secure Software Download	I468971	5-Dec-08	97147538	11-Jan-15	Inside Secure	Granted
US	Dynamic Redundancy Checker Against Fault Injection	7,774,587	12-Jul-06	11486232	10-Aug-10	Verimatrix	Granted
TW	Dynamic Redundancy Checker Against Fault Injection	I368152	12-Jul-07	96125462	11-Jul-12	Inside Secure	Granted
US	Computer-Implemented Method for Fast Generation	6,718,536	21-Jun-02	10176497	6-Apr-04	Verimatrix	Granted

	Title						
	and Testing of Probable Prime Numbers for Cryptographic Applications						
TW	Computer-Implemented Method for Fast Generation and Testing of Probable Prime Numbers for Cryptographic Applications	1282512	21-May-03	92113699	11-Jun-07	Inside Secure	Granted
DE	Computer-Implemented Method for Fast Generation and Testing of Probable Prime Numbers for Cryptographic Applications	1,518,172	25-Apr-03	03721875.7	18-Apr-12	Verimatrix	Granted
FR	Computer-Implemented Method for Fast Generation and Testing of Probable Prime Numbers for Cryptographic Applications	1,518,172	25-Apr-03	03721875.7	18-Apr-12	Verimatrix	Granted
GB	Computer-Implemented Method for Fast Generation and Testing of Probable Prime Numbers for Cryptographic Applications	1,518,172	25-Apr-03	03721875.7	18-Apr-12	Inside Secure	Granted
CN	Computer-Implemented Method for Fast Generation and Testing of Probable Prime Numbers for Cryptographic Applications	ZL03818316.1	25-Apr-03	038183316.1	30-Dec-09	Inside Secure	Granted

Country	Title	Application No.	Date	Publication No.	Date	Assignee	Status
JP	Computer-Implemented Method for Fast Generation and Testing of Probable Prime Numbers for Cryptographic Applications	4756117	25-Apr-03	2004-515648	10-Jun-11	Inside Secure	Granted
KR	Computer-Implemented Method for Fast Generation and Testing of Probable Prime Numbers for Cryptographic Applications	10-938030	25-Apr-03	10-2004-7020867	13-Jan-10	Inside Secure	Granted
FR	Séquence de multiplication efficace pour opérandes à grands nombres entiers plus larges que le matériel multiplicateur	2,853,425	7-Apr-03	0304299	13-Jan-06	Verimatrix	Granted
TW	Séquence de multiplication efficace pour opérandes à grands nombres entiers plus larges que le matériel multiplicateur	I338858	6-Apr-04	93109455	11-Mar-11	Inside Secure	Granted
US	Séquence de multiplication efficace pour opérandes à grands nombres entiers plus larges que le matériel multiplicateur	7,392,276	7-Jul-03	10615475	24-Jun-08	Verimatrix	Granted
DE	Séquence de multiplication efficace pour opérandes à grands nombres entiers plus	1,614,027	22-Mar-04	04759716.6	9-Sep-09	Verimatrix	Granted

	larges que le matériel multiplicateur						
CN	Séquence de multiplication efficace pour opérandes à grands nombres entiers plus larges que le matériel multiplicateur	ZL2004800091 60.7	22-Mar-04	2004800009160.7	20-May-09	Inside Secure	Granted
FR	Microprocessor Protected Against Memory Dump	2,979,442	29-Aug-11	1157603	16-Aug-13	Verimatrix	Granted
EP	Microprocessor Protected Against Memory Dump		14-Aug-12	12180413.2		Verimatrix	Published
US	Montgomery Multiplication Circuit	8,793,300	11-Apr-12	13/444 109	29-Jul-14	Verimatrix	Granted
DE	Montgomery Multiplication Circuit	2,515,227	29-Mar-12	12162000.9	21-Aug-13	Verimatrix	Granted
FR	Montgomery Multiplication Circuit	2,515,227	29-Mar-12	12162000.9	21-Aug-13	Verimatrix	Granted
GB	Montgomery Multiplication Circuit	2,515,227	29-Mar-12	12162000.9	21-Aug-13	Inside Secure	Granted
FR	Encryption Process Protected Against Side Channel Attacks	2,985,624	11-Jan-12	1250272	21-Nov-14	Verimatrix	Granted
CN	Encryption Process Protected Against Side Channel Attacks	ZL201280066783.2	21-Dec-12	201280066783.2	31-Aug-18	Inside Secure	Granted

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US	Montgomery Multiplication Method	8,959,134	11-Apr-12	13/444 125	17-Feb-15	Verimatrix	Granted
DE	Montgomery Multiplication Method	2,515,228	29-Mar-12	12162002.5	13-Nov-13	Verimatrix	Granted
FR	Montgomery Multiplication Method	2,515,228	29-Mar-12	12162002.5	13-Nov-13	Verimatrix	Granted
GB	Montgomery Multiplication Method	2,515,228	29-Mar-12	12162002.5	13-Nov-13	Inside Secure	Granted
FR	Method of Generating Provable Prime Numbers Suitable to Be Implemented Into a Smartcard	2,984,547	15-Dec-11	1161739	6-Apr-18	Verimatrix	Granted
FR	Method of Generating Provable Prime Numbers Suitable to Be Implemented Into a Smartcard	2,984,548	15-Dec-11	1161740	2-Oct-15	Verimatrix	Granted
FR	Method of Generating Provable Prime Numbers Suitable to Be Implemented Into a Smartcard	2,984,550	15-Dec-11	1161742	2-Oct-15	Verimatrix	Granted
DE	Method of Generating Provable Prime Numbers Suitable to Be Implemented Into a Smartcard	2,791,783	12-Dec-12	12815733.6	17-Apr-19	Verimatrix	Granted
FR	Method of Generating Provable Prime Numbers	2,791,783	12-Dec-12	12815733.6	17-Apr-19	Verimatrix	Granted

	Suitable to Be Implemented Into a Smartcard						
GB	Method of Generating Provable Prime Numbers Suitable to Be Implemented Into a Smartcard	2,791,783	12-Dec-12	12815733.6	17-Apr-19	Inside Secure	Granted
US	Method of Generating Provable Prime Numbers Suitable to Be Implemented Into a Smartcard	9,577,826	12-Dec-12	14/365 671	21-Feb-17	Verimatrix	Granted
DE	Cyclic Redundancy Check Method With Protection From Side-Channel Attacks	2,842,232	26-Mar-13	13719930.3	21-Sep-16	Verimatrix	Granted
FR	Cyclic Redundancy Check Method With Protection From Side-Channel Attacks	2,842,232	26-Mar-13	13719930.3	21-Sep-16	Verimatrix	Granted
GB	Cyclic Redundancy Check Method With Protection From Side-Channel Attacks	2,842,232	26-Mar-13	13719930.3	21-Sep-16	Inside Secure	Granted
CN	Cyclic Redundancy Check Method With Protection From Side-Channel Attacks	ZL201380022194.9	26-Mar-13	201380022194.9	22-Sep-17	Inside Secure	Granted
IN	Cyclic Redundancy Check Method With Protection From Side-Channel Attacks		26-Mar-13	2283/KOLNP/2014		Inside Secure	Filed

US	Cyclic Redundancy Check Method With Protection From Side-Channel Attacks	9,977,899	26-Mar-13	14/397 330	22-May-18	Verimatrix	Granted
US	Fast Scalar Multiplication for Elliptic Curve Cryptosystems over Prime Fields	8,369,517	12-Aug-08	12/190 539	5-Feb-13	Verimatrix	Granted
US	Low Cost Implementation for Small Content-Addressable Memories	8,549,218	10-Nov-08	12/268 367	1-Oct-13	Verimatrix	Granted
FR	Portable Device Protected Against an Attack	2,996,028	21-Sep-12	1258862	7-Aug-15	Verimatrix	Granted
US	Dummy Write Operations	8,006,045	27-Feb-09	12/395 572	23-Aug-11	Verimatrix	Granted
US	Mécanisme de récupération de clé pour systèmes cryptographiques	8,233,620	27-Feb-09	12/395 504	31-Jul-12	Verimatrix	Granted
TW	Mécanisme de récupération de clé pour systèmes cryptographiques	I469609	25-Feb-10	99105492	11-Jan-15	Inside Secure	Granted
CN	Mécanisme de récupération de clé pour systèmes cryptographiques	201080009480.8	25-Feb-10	201080009480.8	1-Apr-15	Inside Secure	Granted
US	Detecting Radiation-Based Attacks	8,352,752	1-Sep-06	11/515 103	8-Jan-13	Verimatrix	Granted
TW	Detecting Radiation-Based Attacks	I420397	29-Aug-07	96132124	21-Dec-13	Inside Secure	Granted

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CN	Detecting Radiation-Based Attacks	200780032310.X	29-Aug-07	200780032310.X	5-Dec-12	Inside Secure	Granted
DE	Detecting Radiation-Based Attacks		29-Aug-07	11 2007 002 037.7		Verimatrix	Published
US	Managing Power and Timing in a Smart Card Device	7,845,568	9-May-07	11/746 311	7-Dec-10	Inside Secure	Granted
TW	Managing Power and Timing in a Smart Card Device	1444896	9-May-08	97117313	11-Jul-14	Inside Secure	Granted
CN	Managing Power and Timing in a Smart Card Device		9-May-08	201510855231.5		Inside Secure	Published
DE	Managing Power and Timing in a Smart Card Device		9-May-08	11 2008 001 187.7	15-Oct-13	Verimatrix	Published
US	Elliptic Curves Point Transformations	8,559,625	7-Aug-07	11/835 292	15-Oct-13	Verimatrix	Granted
US	Modular Reduction With Modulus of Special Form of the Modulus	8,233,615	19-Feb-08	12/033 512	31-Jul-12	Verimatrix	Granted
DE	Modular Reduction With Modulus of Special Form of the Modulus		13-Jan-09	112009000152.1		Verimatrix	Published
TW	Modular Reduction With Modulus of Special Form of the Modulus	1512610	14-Jan-09	98101307	11-Dec-15	Inside Secure	Granted
US	Modular Reduction With Modulus of Special Form of the Modulus			12/028 427		Verimatrix	Published
DE	Modular Reduction With Modulus of Special Form of the Modulus					Verimatrix	Published
US	REPRESENTATION CHANGE OF A POINT ON AN ELLIPTIC CURVE	8,619,977	8-Feb-08	12/028 427	31-Dec-13	Verimatrix	Granted

Country	Title	Number	Date	Application No.	Date	Owner	Status
TW	REPRESENTATION CHANGE OF A POINT ON AN ELLIPTIC CURVE	I462010	14-Jan-09	98101308	21-Nov-14	Inside Secure	Granted
DE	REPRESENTATION CHANGE OF A POINT ON AN ELLIPTIC CURVE		13-Jan-09	11 2009 000 154.8		Verimatrix	Published
US	Access Rights on a Memory Map	7,895,404	14-Feb-08	12/031 586	22-Feb-11	Verimatrix	Granted
TW	Access Rights on a Memory Map	I461914	13-Feb-09	98104759	21-Nov-14	Inside Secure	Granted
US	Access Rights on a Memory Map	8,327,100	16-Feb-11	13/028 756	4-Dec-12	Verimatrix	Granted
DE	Access Rights on a Memory Map		9-Feb-09	112009000344.3		Verimatrix	Published
US	System and Method for Encrypting Data	8,301,905	8-Sep-06	11/517 641	30-Oct-12	Verimatrix (Joint ownership)	Granted
TW	System and Method for Encrypting Data	I368919	7-Sep-07	96133588	21-Jul-12	Inside Secure (Joint ownership)	Granted
US	Randomized Modular Reduction Method and Hardware Therefor	7,809,133	18-Feb-04	10/781 311	5-Oct-10	Verimatrix	Granted
TW	Randomized Modular Reduction Method and Hardware Therefor	I403144	10-Nov-04	93134209	21-Jul-13	Inside Secure	Granted

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DE	Randomized Modular Reduction Method and Hardware Therefor	1,687,930	5-Nov-04	04 800 660.5	4-Jan-12	Verimatrix	Granted
FR	Randomized Modular Reduction Method and Hardware Therefor	1,687,930	5-Nov-04	04800660.5	4-Jan-12	Verimatrix	Granted
GB	Randomized Modular Reduction Method and Hardware Therefor	1,687,930	5-Nov-04	04800660.5	4-Jan-12	Inside Secure	Granted
CN	Randomized Modular Reduction Method and Hardware Therefor	ZL200480033 595.5	5-Nov-04	200480033595.5	22-Oct-10	Inside Secure	Granted
FR	Randomized Modular Polynomial Reduction Method and Hardware Therefor	2,885,711	12-May-05	0504779	6-Jul-07	Verimatrix	Granted
TW	Randomized Modular Polynomial Reduction Method and Hardware Therefor	1386818	8-May-06	95116180	21-Feb-13	Inside Secure	Granted
US	Randomized Modular Polynomial Reduction Method and Hardware Therefor	7,805,480	15-Aug-05	11/203 939	28-Sep-10	Verimatrix	Granted
DE	Randomized Modular Polynomial Reduction Method and Hardware Therefor	1,889,398	12-Apr-06	06749987.1	13-Jan-16	Verimatrix	Granted

Country	Title	Number	Date	Number	Date	Owner	Status
GB	Randomized Modular Polynomial Reduction Method and Hardware Therefor	1,889,398	12-Apr-06	06749987.1	13-Jan-16	Inside Secure	Granted
CN	Randomized Modular Polynomial Reduction Method and Hardware Therefor	101194457	12-Apr-06	200680020941.5	1-Jun-11	Inside Secure	Granted
JP	Randomized Modular Polynomial Reduction Method and Hardware Therefor	4875700	12-Apr-06	2008511127	2-Dec-11	Inside Secure	Granted
KR	Randomized Modular Polynomial Reduction Method and Hardware Therefor	10-1252318	12-Apr-06	10-2007-7029023	2-Apr-13	Inside Secure	Granted
FR	Procédé de securisation pour la protection de donnees	2,888,975	21-Jul-05	0507766	7-Sep-07	Verimatrix	Granted
TW	Procédé de securisation pour la protection de donnees	1388048	20-Jul-06	95126522	1-Mar-13	Inside Secure	Granted
US	Procédé de securisation pour la protection de donnees	7,791,898	21-Oct-05	11/256 124	7-Sep-10	Verimatrix	Granted
CN	Procédé de securisation pour la protection de donnees	ZL200680032529.5	20-Jun-06	200680032529.5	30-May-12	Inside Secure	Granted
FR	Procédé de protection par chiffrement	2,893,796	21-Nov-05	0511768	4-Jan-08	Verimatrix	Granted

TW	Procédé de protection par chiffrement	I418197	14-Nov-06	95142013	1-Dec-13	Inside Secure	Granted
US	Procédé de protection par chiffrement	7,848,515	22-Feb-06	11/358 979	7-Dec-10	Inside Secure	Granted
DE	Procédé de protection par chiffrement	1,955,465	21-Nov-06	06850185.7	11-Sep-19	Verimatrix	Granted
FR	Procédé de protection par chiffrement	1,955,465	21-Nov-06	06850185.7	11-Sep-19	Verimatrix	Granted
GB	Procédé de protection par chiffrement	1,955,465	21-Nov-06	06850185.7	11-Sep-19	Inside Secure	Granted
CN	Procédé de protection par chiffrement	ZL200680051506.9	21-Nov-06	200680051506.9	21-Aug-13	Inside Secure	Granted
JP	Procédé de protection par chiffrement	4990908	21-Nov-06	2008-541510	11-May-12	Inside Secure	Granted
KR	Procédé de protection par chiffrement	10-1345083	21-Nov-06	10-2008-7015072	18-Dec-13	Inside Secure	Granted
FR	Procédé de calcul numérique incluant la division euclidienne	2,897,964	28-Feb-06	0601782	13-Jan-17	Verimatrix	Granted
US	Procédé de calcul numérique incluant la division euclidienne	7,672,990	30-May-06	11/442 776	2-Mar-10	Verimatrix	Granted
FR	Procédé pour les conjectures de quotient rapide et une manipulation de congruences		28-Feb-06	0601781		Verimatrix	Published

Country	Title	Patent No.	Date	Application No.	Date	Owner	Status
US	Procédé pour les conjectures de quotient rapide et une manipulation de congruences	7,788,311	30-May-06	11/442 922	31-Aug-10	Verimatrix	Granted
US	Key Protection Mechanism	7,822,207	22-Dec-06	11/615 225	26-Oct-10	Verimatrix	Granted
TW	Key Protection Mechanism	I434565	15-Nov-07	96143280	11-Apr-14	Inside Secure	Granted
CN	Key Protection Mechanism	ZL200780047663.7	2-Nov-07	200780047663.7	12-Dec-12	Inside Secure	Granted
DE	Key Protection Mechanism		2-Nov-07	11 2007 003 061.5		Verimatrix	Published
US	Chinese Remainder Theorem-Based Computation Method for Cryptosystems	8,280,041	12-Mar-07	11/684 842	2-Oct-12	Inside Secure	Granted
TW	Chinese Remainder Theorem-Based Computation Method for Cryptosystems	I448963	12-Mar-08	97108763	11-Aug-14	Inside Secure	Granted
CN	Chinese Remainder Theorem-Based Computation Method for Cryptosystems	ZL200880008030.X	12-Mar-08	200880008030.X	5-Mar-14	Inside Secure	Granted
DE	Chinese Remainder Theorem-Based Computation Method for Cryptosystems		12-Mar-08	11 2008 000 668.7		Verimatrix	Published

Country	Title	Number	Date	Application No.	Date	Owner	Status
US	Modular Multiplication Method With Precomputation Using One Known Operand	8,024,391	6-Nov-06	11/556 894	20-Sep-11	Verimatrix	Granted
FR	Secure Processor With No Non-Volatile Memory	2,991,797	12-Jun-12	1201678	30-Aug-19	Verimatrix	Granted
US	Method for Managing Memory Space in a Secure Non-Volatile Memory of a Secure Element	9,430,650	2-Apr-12	13/437 124	30-Aug-16	Verimatrix	Granted
DE	Method for Managing Memory Space in a Secure Non-Volatile Memory of a Secure Element	2,626,804	9-Feb-12	121547244	13-Sep-17	Verimatrix	Granted
FR	Method for Managing Memory Space in a Secure Non-Volatile Memory of a Secure Element	2,626,804	9-Feb-12	121547244	13-Sep-17	Verimatrix	Granted
GB	Method for Managing Memory Space in a Secure Non-Volatile Memory of a Secure Element	2,626,804	9-Feb-12	121547244	13-Sep-17	Inside Secure	Granted
FR	A Method for Backing Up Data Outside a Secure Microcircuit		12-Jun-12	1201677		Verimatrix	Published
EP	A Method for Backing Up Data Outside a Secure Microcircuit		6-May-13	137272613		Verimatrix	Published

Country	Title	Patent Number	Date	Application Number	Date	Owner	Status
FR	Method for Providing a Secure Service	2,997,525	26-Oct-12	1260227	4-Dec-15	Verimatrix	Granted
DE	Method for Providing a Secure Service	2,912,594	25-Sep-13	13779300.6	10-Apr-19	Verimatrix	Granted
FR	Method for Providing a Secure Service	2,912,594	25-Sep-13	13779300.6	10-Apr-19	Verimatrix	Granted
GB	Method for Providing a Secure Service	2,912,594	25-Sep-13	13779300.6	10-Apr-19	Inside Secure	Granted
CN	Method for Providing a Secure Service	ZL201380054027.2	25-Sep-13	201380054027.2	8-Aug-17	Inside Secure	Granted
US	Method for Providing a Secure Service	9,621,550	25-Sep-13	14/431 153	11-Apr-17	Verimatrix	Granted
FR	System for Detecting Call Stack Tampering	2,994,290	6-Aug-12	1257635	6-Apr-18	Verimatrix	Granted
CN	System for Detecting Call Stack Tampering	ZL201380041553.5	31-Jul-13	201380041553.5	8-Aug-17	Inside Secure	Granted
EP	System for Detecting Call Stack Tampering		31-Jul-13	13756638.6		Verimatrix	Published
IN	System for Detecting Call Stack Tampering		31-Jul-13	341/CHENP/2015		Inside Secure	Published
US	System for Detecting Call Stack Tampering	9,268,559	31-Jul-13	14/417 639	23-Feb-16	Verimatrix	Granted
FR	Method for Generating Prime Numbers Proven Suitable for Chip Cards	2,984,551	30-May-12	1201550	17-Jul-15	Verimatrix	Granted

Country	Title	Number	Filing Date	Application No.	Issue Date	Company	Status
IN	Method for Generating Prime Numbers Proven Suitable for Chip Cards		12-Dec-12	4637/CHENP/2014		Inside Secure	Published
US	Method for Generating Prime Numbers Proven Suitable for Chip Cards	9,596,080	12-Dec-12	14/365 899	14-Mar-17	Verimatrix	Granted
US	Cryptographic Method Comprising a Modular Exponentiation Operation	9,405,729	5-Nov-13	14/072 155	2-Aug-16	Verimatrix	Granted
DE	Cryptographic Method Comprising a Modular Exponentiation Operation	2,731,006	5-Nov-13	13191662.9	15-Apr-15	Verimatrix	Granted
FR	Cryptographic Method Comprising a Modular Exponentiation Operation	2,731,006	5-Nov-13	13191662.9	15-Apr-15	Verimatrix	Granted
GB	Cryptographic Method Comprising a Modular Exponentiation Operation	2,731,006	5-Nov-13	13191662.9	15-Apr-15	Inside Secure	Granted
DE	Cryptography Method Comprising an Operation of Multiplication by a Scalar or an Exponentiation	2,946,284	13-Jan-14	14703138.9	26-Apr-17	Verimatrix	Granted
FR	Cryptography Method Comprising an Operation of Multiplication by a Scalar or an Exponentiation	2,946,284	13-Jan-14	14703138.9	26-Apr-17	Verimatrix	Granted

GB	Cryptography Method Comprising an Operation of Multiplication by a Scalar or an Exponentiation	2,946,284	13-Jan-14	147031138.9	26-Apr-17	Inside Secure	Granted
CN	Cryptography Method Comprising an Operation of Multiplication by a Scalar or an Exponentiation	ZL201480005200.4	13-Jan-14	201480005200.4	24-Oct-17	Inside Secure	Granted
IN	Cryptography Method Comprising an Operation of Multiplication by a Scalar or an Exponentiation		13-Jan-14	21186/KOLNP/2015		Inside Secure	Published
KR	Cryptography Method Comprising an Operation of Multiplication by a Scalar or an Exponentiation		13-Jan-14	10-2015-7021332		Inside Secure	
US	Cryptography Method Comprising an Operation of Multiplication by a Scalar or an Exponentiation	9,772,821	13-Jan-14	14/762 010	26-Sep-17	Verimatrix	Granted
DE	Method of Updating the Operating System of a Secure Microcircuit	2,772,868	11-Feb-14	14154663.0	6-Dec-17	Verimatrix	Granted
FR	Method of Updating the Operating System of a Secure Microcircuit	2,772,868	11-Feb-14	14154663.0	6-Dec-17	Verimatrix	Granted

GB	Method of Updating the Operating System of a Secure Microcircuit	2,772,868	11-Feb-14	14154663.0	6-Dec-17	Inside Secure	Granted
US	Method for Intercepting Network Packets in a Computing Device	6,678,734	13-Nov-99	09/439 419	13-Jan-04	Verimatrix	Granted
CA	Method for Intercepting Network Packets in a Computing Device	2,325,652	10-Nov-00	2325652	17-Aug-10	Verimatrix	Granted
DE	Method for Intercepting Network Packets in a Computing Device	10054923	6-Nov-00	DE 100 54 923.3	14-Nov-13	Verimatrix	Granted
IL	Method for Intercepting Network Packets in a Computing Device	IL139415	1-Nov-00	20000139415	19-Jun-05	Inside Secure	Granted
US	Digital True Random Number Generator Circuit	6,807,553	23-Apr-01	09/839 121	19-Oct-04	Verimatrix	Granted
US	High Speed Data Stream Pattern Recognition	6,856,981	3-Dec-01	10/005 462	15-Feb-05	Verimatrix	Granted
US	Generator Circuit for Generating Large Numbers	7,054,894	16-Aug-02	10/219 741	30-May-06	Verimatrix	Granted
US	Method and Device for Making Information Contents of a Volatile Semiconductor Memory Irretrievable	7,200,759	8-Jun-01	09/875 977	3-Apr-07	Verimatrix	Granted

US	Method of Generating of Dfa State Machine That Groups Transitions Into Classes in Order to Conserve Memory	7,240,040	8-Aug-02	10/217 592	3-Jul-07	Verimatrix	Granted
US	Security System for a Data Communications Network	7,302,487	22-Mar-02	10/104 790	27-Nov-07	Verimatrix	Granted
US	System and Method for Determining the Start of a Match of a Regular Expression	7,305,391	6-Feb-04	10/773 595	4-Dec-07	Verimatrix	Granted
US	System and Method for Determining the Start of a Match of a Regular Expression	9,043,272	18-Sep-07	11/901 515	26-May-15	Verimatrix	Granted
US	Fast Hardware Processing of Regular Expressions Containing Sub-Expressions	7,461,370	7-Feb-03	10/359 839	2-Dec-08	Verimatrix	Granted
US	Transmission of Broadcast Packets in Secure Communication Connections Between Computers	7,505,473	30-Jun-03	10/611 358	17-Mar-09	Verimatrix	Granted
US	Method for Preparing a Decision Tree for Packet Processing	7,548,992	28-Mar-03	10/402 734	16-Jun-09	Verimatrix	Granted
US	Système et procédé de détection de verrouillage	9,594,541	6-Jan-09	12/319 308	14-Mar-17	Verimatrix	Granted

Country	Title					Owner	Status
DE	Système et procédé de détection de verrouillage	2,207,088	23-Dec-09	09180596.0	23-Jan-13	Verimatrix	Granted
FR	Système et procédé de détection de verrouillage	2,207,088	23-Dec-09	09180596.0	23-Jan-13	Verimatrix	Granted
US	Application Gateway System and Method for Maintaining Security in a Packet-Switched Information Network	8,566,920	30-Sep-09	12/586 965	22-Oct-13	Verimatrix	Granted
FR	Memory Circuit Comprising Means for Detecting an Error Injection	3,010,822	17-Sep-13	1358926	2-Oct-15	Verimatrix	Granted
EP	Memory Circuit Comprising Means for Detecting an Error Injection		8-Sep-14	14796156.9		Verimatrix	Published
FR	Procédé de protection de l'intégrite de données a l'aide d'un nombre idempotent	3,010,561	12-Sep-13	1358798	18-Nov-16	Verimatrix	Granted
EP	A Digital Method and Device for Generating True Random Numbers		18-Apr-14	14165296.6		Verimatrix	Published
CN	Elliptic Curve Encryption Method Comprising an Error Detection		4-Aug-15	201510472582.8		Inside Secure	Published
IN	Elliptic Curve Encryption Method Comprising an Error Detection		30-Jul-15	829/KOL/2015		Inside Secure	Filed

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US	Elliptic Curve Encryption Method Comprising an Error Detection	9,780,946	5-Aug-15	14/818 684	3-Oct-17	Verimatrix	Granted
DE	Elliptic Curve Encryption Method Comprising an Error Detection	2,983,083	22-Jul-15	15177904.8	12-Apr-17	Verimatrix	Granted
FR	Elliptic Curve Encryption Method Comprising an Error Detection	2,983,083	22-Jul-15	15177904.8	12-Apr-17	Verimatrix	Granted
GB	Elliptic Curve Encryption Method Comprising an Error Detection	2,983,083	22-Jul-15	15177904.8	12-Apr-17	Inside Secure	Granted
FR	A Method of Countermeasure Against an Attack by Analysis of Electrical Consumption for Cryptographic Device	3,026,206	23-Sep-14	1458951	1-Dec-17	Verimatrix	Granted
EP	A Method of Countermeasure Against an Attack by Analysis of Electrical Consumption for Cryptographic Device	3,198,515	23-Sep-15	15787251.6	20-Nov-19	Verimatrix	Granted
US	A Method of Countermeasure Against an Attack by Analysis of Electrical Consumption for Cryptographic Device		23-Sep-15	15/463 364		Verimatrix	Published

Country	Title	Number	Filing Date	Application No.	Date	Owner	Status
DE	Fault Detection for Systems Implementing a Block Cipher	3,086,503	23-Apr-15	15164808.6	6-Jun-18	Verimatrix	Granted
FR	Fault Detection for Systems Implementing a Block Cipher	3,086,503	23-Apr-15	15164808.6	6-Jun-18	Inside Secure	Granted
GB	Fault Detection for Systems Implementing a Block Cipher	3,086,503	23-Apr-15	15164808.6	6-Jun-18	Verimatrix	Granted
FR	Method of Securing a Comparison of Data During the Execution of a Program	3,036,203	13-May-15	1554348	19-May-17	Verimatrix	Granted
CN	Method of Securing a Comparison of Data During the Execution of a Program		10-May-16	201680027175.9		Inside Secure	Published
EP	Method of Securing a Comparison of Data During the Execution of a Program		10-May-16	16731207.3		Verimatrix	Published
IN	Method of Securing a Comparison of Data During the Execution of a Program		10-May-16	201737037429		Inside Secure	Published
US	Method of Securing a Comparison of Data During the Execution of a Program		10-May-16	15/808 362		Verimatrix	Published
FR	Method for Sharing a Memory Between at Least Two Functional Entities	3,035,241	16-Apr-15	1553369	22-Dec-17	Verimatrix	Granted

Country	Title	Number	Date	Application Number	Date	Owner	Status
DE	Method for Sharing a Memory Between at Least Two Functional Entities	3,283,968	7-Apr-16	16730870.9	20-Mar-19	Verimatrix	Granted
FR	Method for Sharing a Memory Between at Least Two Functional Entities	3,283,968	7-Apr-16	16730870.9	20-Mar-19	Verimatrix	Granted
GB	Method for Sharing a Memory Between at Least Two Functional Entities	3,283,968	7-Apr-16	16730870.9	20-Mar-19	Inside Secure	Granted
CN	Method for Sharing a Memory Between at Least Two Functional Entities		7-Apr-16	201680021722.2		Inside Secure	Published
IN	Method for Sharing a Memory Between at Least Two Functional Entities		7-Apr-16	201737033222		Inside Secure	Published
US	Method for Sharing a Memory Between at Least Two Functional Entities		13-Oct-17	15/784 007		Verimatrix	Allowance
FR	Method for Securing the Execution of a Program	3,035,240	15-Apr-15	1500794	6-Apr-18	Verimatrix	Granted
CN	Method for Securing the Execution of a Program		6-Apr-16	201680021925.1		Inside Secure	Published
EP	Method for Securing the Execution of a Program		6-Apr-16	16731193.5		Verimatrix	Published
IN	Method for Securing the Execution of a Program		6-Apr-16	201737035051		Inside Secure	Published

Country	Title	Patent No.	Filing Date	Application No.	Grant/Pub Date	Owner	Status
US	Method for Securing the Execution of a Program		13-Oct-17	15/784 010		Verimatrix	Published
US	Secure Asset Management System		12-May-17	15/594 122		Verimatrix	Published
DE	Secure Asset Management System	3,246,845	17-May-16	16170012.5	5-Dec-18	Verimatrix	Granted
FR	Secure Asset Management System	3,246,845	17-May-16	16170012.5	5-Dec-18	Verimatrix	Granted
GB	Secure Asset Management System	3,246,845	17-May-16	16170012.5	5-Dec-18	Inside Secure	Granted
FR	Countermeasures for Fault-Injection Attacks by Optical and Electromagnetic Pulses	3,042,055	6-Oct-15	1559497	24-Nov-17	Verimatrix	Granted
DE	Countermeasures for Fault-Injection Attacks by Optical and Electromagnetic Pulses	3,360,073	3-Oct-16	16790646.0	21-Aug-19	Verimatrix	Granted
FR	Countermeasures for Fault-Injection Attacks by Optical and Electromagnetic Pulses	3,360,073	3-Oct-16	16790646.0	21-Aug-19	Verimatrix	Granted
GB	Countermeasures for Fault-Injection Attacks by Optical and Electromagnetic Pulses	3,360,073	3-Oct-16	16790646.0	21-Aug-19	Inside Secure	Granted
US	Countermeasures for Fault-Injection Attacks by Optical and Electromagnetic Pulses	10,303,903	3-Oct-16	15/947 379	28-May-19	Verimatrix	Granted

FR	Procédé de transaction comprenant des opérations d'écriture de données dans une mémoire non volatile		5-Jul-16	1656413		Verimatrix	Published
GB	Preventing cloning of high value software using embedded hardware and software functionality	1,747,504	8-Apr-05	057370249	6-Feb-08	Inside Secure	Granted
CH	Method and Apparatus for Supporting Multiple Broadcasters Independently Using a Single Conditional Access System	1,813,107	18-Oct-05	05811812.6	18-Mar-15	Verimatrix	Granted
DE	Method and Apparatus for Supporting Multiple Broadcasters Independently Using a Single Conditional Access System	1,813,107	18-Oct-05	05811812.6	18-Mar-15	Verimatrix	Granted
FR	Method and Apparatus for Supporting Multiple Broadcasters Independently Using a Single Conditional Access System	1,813,107	18-Oct-05	05811812.6	18-Mar-15	Verimatrix	Granted
GB	Method and Apparatus for Supporting Multiple Broadcasters Independently Using a Single Conditional Access System	1,813,107	18-Oct-05	05811812.6	18-Mar-15	Inside Secure	Granted

Country	Title	Number	Date	Application Number	Date	Owner	Status
IE	Method and Apparatus for Supporting Multiple Broadcasters Independently Using a Single Conditional Access System	1,813,107	18-Oct-05	05811812.6	18-Mar-15	Inside Secure	Granted
US	Method and Apparatus for Supporting Multiple Broadcasters Independently Using a Single Conditional Access System	8,243,925	18-Oct-05	11/795 272	14-Aug-12	Verimatrix	Granted
US	Method and Apparatus for Supporting Multiple Broadcasters Independently Using a Single Conditional Access System	9,014,375	3-Jul-12	13/541 492	21-Apr-15	Verimatrix	Granted
US	Method and Apparatus for Supporting Multiple Broadcasters Independently Using a Single Conditional Access System	9,712,786	21-Apr-15	14/692 500	18-Jul-17	Verimatrix	Granted
US	Method and apparatus for supporting broadcast efficiency and security enhancements	7,970,138	26-May-06	11/441 888	28-Jun-11	Verimatrix	Granted
US	Method and apparatus for supporting broadcast efficiency and security enhancements	8,879,729	4-May-11	13/100 565	4-Nov-14	Verimatrix	Granted

US	Method and Apparatus for Providing Secure Internet Protocol Media Services	8,761,393	12-Oct-07	11/974 329	24-Jun-14	Verimatrix	Granted
US	System and method for media transcoding and presentation	8,281,359	11-Aug-09	12/539 400	2-Oct-12	Verimatrix	Granted
US	Method and Apparatus for Camouflaging a Printed Circuit Board	8,151,235	24-Feb-09	12/380 094	3-Apr-12	Verimatrix	Granted
US	Method and Apparatus for Camouflaging a Printed Circuit Board	8,418,091	13-Oct-09	12/578 441	9-Apr-13	Verimatrix	Granted
US	Method and Apparatus for Camouflaging a Printed Circuit Board	9,355,199	7-Mar-13	13/789 267	31-May-16	Verimatrix	Granted
US	Building block for a secure cmos logic cell library	8,111,089	24-May-10	12/786 205	7-Feb-12	Verimatrix	Granted
US	Hardware-Enforced, Always-on Insertion of a Watermark in a Video Processing Path	9,355,426	26-Jan-12	13/981 289	31-May-16	Verimatrix	Granted
US	Hardware-Enforced, Always-on Insertion of a Watermark in a Video Processing Path	9,942,586	27-May-16	15/167 319	10-Apr-18	Verimatrix	Granted
US	Hardware-Enforced, Always-on Insertion of a Watermark in a Video Processing Path	10,277,935	27-Mar-18	15/937 772	30-Apr-19	Verimatrix	Granted

Country	Title	Number	Date	Application No.	Filing Date	Owner	Status
US	Method and apparatus for camouflaging a standard cell based integrated circuit with micro circuits and post processing	8,510,700	9-Feb-12	13/370 118	13-Aug-13	Verimatrix	Granted
US	Method and apparatus for camouflaging a standard cell based integrated circuit with micro circuits and post processing	9,542,520	12-Jul-13	13/940 585	10-Jan-17	Verimatrix	Granted
US	Method and apparatus for camouflaging a standard cell based integrated circuit with micro circuits and post processing	9,940,425	8-Dec-16	15/373 334	10-Apr-18	Verimatrix	Granted
DE	Blackbox Security Provider Programming System Permitting Multiple Customer Use and in Field Conditional Access Switching	2,820,546	1-Mar-13	13755054.7	31-Jul-19	Verimatrix	Granted
FR	Blackbox Security Provider Programming System Permitting Multiple Customer Use and in Field Conditional Access Switching	2,820,546	1-Mar-13	13755054.7	31-Jul-19	Verimatrix	Granted
GB	Blackbox Security Provider Programming System	2,820,546	1-Mar-13	13755054.7	31-Jul-19	Inside Secure	Granted

Country	Title	Number	Date	Application No.	Date	Owner	Status
US	Permitting Multiple Customer Use and in Field Conditional Access Switching						
US	Blackbox Security Provider Programming System Permitting Multiple Customer Use and in Field Conditional Access Switching	9,800,405	1-Mar-13	14/382 539	24-Oct-17	Verimatrix	Granted
US	Method and apparatus for providing secure internet protocol media services	9,277,259	23-Jun-14	14/312 560	1-Mar-16	Verimatrix	Granted
CA	Method and apparatus for providing secure internet protocol media services		23-Jun-15	2953485		Verimatrix	Published
EP	Method and apparatus for providing secure internet protocol media services		23-Jun-15	15811834.9		Verimatrix	Published
US	Physically Unclonable Camouflage Structure and Methods for Fabricating Same	9,735,781	30-Dec-15	14/985 270	15-Aug-17	Verimatrix	Granted
US	Physically Unclonable Camouflage Structure and Methods for Fabricating Same		11-Aug-17	15/675 418		Verimatrix	Allowance

Country	Title					Owner	Status
US	Method and apparatus for a blackbox programming system permitting downloadable applications and multiple security profiles providing hardware separation of services in hardware constrained devices	10,348,501	11-Jul-16	15/207 332	9-Jul-19	Verimatrix	Granted
US	Method and apparatus for a blackbox programming system permitting downloadable applications and multiple security profiles providing hardware separation of services in hardware constrained devices		8-Jul-19	16/505 477		Verimatrix	Filed
CN	Method and Apparatus for Obfuscating an Integrated Circuit With Camouflaged Gates and Logic Encryption		19-Sep-17	201780057579.7		Inside Secure	Published
EP	Method and Apparatus for Obfuscating an Integrated Circuit With Camouflaged Gates and Logic Encryption		19-Sep-17	17853755.1		Verimatrix	Published
US	Method and Apparatus for Obfuscating an Integrated Circuit With Camouflaged Gates and Logic Encryption		19-Sep-17	16/333 589		Verimatrix	Published

US	Signaling Conditional Access System Switching and Key Derivation	10,476,883	23-Oct-17	15/791 260	12-Nov-19	Verimatrix	Granted
EP	Signaling Conditional Access System Switching and Key Derivation		9-Jan-18	18701577.1		Verimatrix	Published
IN	Signaling Conditional Access System Switching and Key Derivation		9-Jan-18	201917024836		Inside Secure	Filed
US	Method and apparatus for supporting multiple broadcasters independently using a single conditional access system	10,477,151	17-Jul-17	15/652 082	12-Nov-19	Verimatrix	Granted
US	Method and apparatus for supporting multiple broadcasters independently using a single conditional access system		31-Oct-19	16/670 912		Verimatrix	Filed
US	Method and apparatus for supporting multiple broadcasters independently using a single conditional access system		31-Oct-19	16/670 957		Verimatrix	Filed
WO	Method and apparatus for supporting multiple broadcasters independently		17-Jul-18	US2018/042542		Verimatrix	Published

	using a single conditional access system				
US	Secure logic locking and configuration with camouflaged programmable micro netlists	6-Aug-18	16/056 268	Verimatrix	Filed
WO	Secure logic locking and configuration with camouflaged programmable micro netlists	2-Aug-18	PCT/IB2018/05 5813	Verimatrix	Published
EP	Network interface with timestamping and data protection	28-Aug-18	18191268.4	Verimatrix	Filed
CN	Network interface with timestamping and data protection	27-Aug-19	201910799377.0	Inside Secure	Filed
US	Network interface with timestamping and data protection	27-Aug-19	16/552 919	Verimatrix	Filed
US	Network interface with timestamping and data protection	8-Mar-19	16/297 511	Verimatrix	Filed
US	OBFUSCATED SHIFT REGISTERS FOR INTEGRATED CIRCUITS	8-Mar-19	16/297 516	Verimatrix	Filed
US	CAMOUFLAGED FINFET AND METHOD FOR PRODUCING SAME	8-Mar-19		Verimatrix	Filed
US	System and method for managing in-field	25-Mar-19	16/363 958	Verimatrix	Published

Type	Title	Date	Application No.	Owner	Status
	deployment of multiple conditional access and watermarking systems			Verimatrix	Filed
US	Method and apparatus for camouflaging an integrated circuit using virtual camouflage cells	25-Mar-19	16/364 056	Verimatrix	Filed
EP	Side-Channel Attack Protected Gates Having Low-Latency and Reduced Complexity	26-Sep-19	19199955.6	Verimatrix	Filed
EP	Side-Channel Attack Protected Gates Having Low-Latency and Reduced Complexity	26-Sep-19	19199955.6	Verimatrix	Filed