PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
WELLS FARGO BANK, NATIONAL ASSOCIATION, AS NOTES COLLATERAL AGENT	12/20/2019

RECEIVING PARTY DATA

Name:	MICROCHIP TECHNOLOGY INCORPORATED
Street Address:	2355 W CHANDLER BOULEVARD
City:	CHANDLER
State/Country:	ARIZONA
Postal Code:	85224
Name:	ATMEL CORPORATION
Street Address:	2355 W CHANDLER BOULEVARD
City:	CHANDLER
State/Country:	ARIZONA
Postal Code:	85224

PROPERTY NUMBERS Total: 77

Property Type	Number
Application Number:	10071605
Application Number:	10666142
Application Number:	10232636
Application Number:	10407622
Application Number:	10352733
Application Number:	10364583
Application Number:	10453157
Application Number:	10760434
Application Number:	10980536
Application Number:	10687980
Application Number:	10762767
Application Number:	11530977
Application Number:	11058056
Application Number:	11062888
Application Number:	10802894

Property Type	Number
Application Number:	11061799
Application Number:	11539567
Application Number:	11137463
Application Number:	11203938
Application Number:	11168833
Application Number:	11457377
Application Number:	11933805
Application Number:	11624139
Application Number:	12014261
Application Number:	11610107
Application Number:	11539564
Application Number:	11554797
Application Number:	11668844
Application Number:	12207147
Application Number:	11846959
Application Number:	12174802
Application Number:	12174903
Application Number:	12031289
Application Number:	13335725
Application Number:	11451610
Application Number:	12395518
Application Number:	12436620
Application Number:	60823839
Application Number:	60989514
PCT Number:	US0415616
PCT Number:	US0328835
PCT Number:	US0331058
PCT Number:	US2005009865
PCT Number:	US0613794
PCT Number:	US0621815
PCT Number:	US2007071941
PCT Number:	US2007087304
PCT Number:	US2007083062
PCT Number:	US0852405
PCT Number:	US0884365
Application Number:	60690701
Application Number:	12606691
Application Number:	09870460

Property Type	Number
Application Number:	11135527
Application Number:	10946432
Application Number:	11049334
Application Number:	10348782
Application Number:	10910038
Application Number:	12481330
Application Number:	13485426
Application Number:	12017521
Application Number:	12977034
Application Number:	13894221
PCT Number:	US0884362
PCT Number:	US0851209
PCT Number:	US0526205
PCT Number:	US2006002914
PCT Number:	US0216705
PCT Number:	US0526259
Application Number:	61060626
Application Number:	60593035
Application Number:	60908328
Application Number:	61289846
Application Number:	13652166
PCT Number:	US0340000
PCT Number:	US0858196
PCT Number:	US2013041202

CORRESPONDENCE DATA

Fax Number: (415)947-2099

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4159472000
Email: qluflood@wsgr.com
Correspondent Name: WSGR, C/O QUI LU FLOOD, SENIOR PARALEGAL
Address Line 1: ONE MARKET, SPEAR TOWER, SUITE 3300
Address Line 4: SAN FRANCISCO, CALIFORNIA 94105

ATTORNEY DOCKET NUMBER:	15286.082
NAME OF SUBMITTER:	QUI LU FLOOD
SIGNATURE:	/Qui Lu Flood/
DATE SIGNED:	12/21/2019

Total Attachments: 15

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RELEASE OF SECURITY INTEREST IN CERTAIN PATENT RIGHTS

This RELEASE OF SECURITY INTEREST IN CERTAIN PATENT RIGHTS (this "Partial Release"), dated as of December 20, 2019, is executed by Wells Fargo Bank, National Association, a national banking association, as Notes Collateral Agent (in such capacity, the "Notes Collateral Agent"), in favor of Microchip Technology Incorporated, a Delaware corporation ("Microchip"), and Atmel Corporation, a Delaware corporation ("Atmel") (each a "Debtor", and collectively the "Debtors"). All capitalized terms used in this Partial Release and not otherwise defined herein, shall have the respective meanings given to such terms in the Patent Security Agreement (defined below).

RECITALS

A. Pursuant to that certain (i) Pledge and Security Agreement, dated as of May 29, 2018, by and among the Issuer and certain other Grantors, and Notes Collateral Agent, and (ii) Grant of Security Interest in Patent Rights, dated as of May 29, 2018 (the "Patent Security Agreement"), executed by Debtors in favor of Notes Collateral Agent, Debtors granted to Notes Collateral Agent a security interest in the Patent Collateral (defined below).

B. Pursuant to the requirements of Section 11.08 of the Indenture, dated as of May 29, 2018, among Microchip, the Guarantors party thereto and Wells Fargo Bank, National Association as trustee (in such capacity, the "Trustee") and as notes collateral agent (in such capacity, the "Notes Collateral Agent"), as supplemented by the First Supplemental Indenture, dated as of May 29, 2018 (as so supplemented, the "Indenture"), Microchip delivered an Officer's Certificate (as defined in the Indenture) and an Opinion of Counsel (as defined in the Indenture), each dated the date hereof, to the Notes Collateral Agent to authorize the execution by the Notes Collateral Agent of this Partial Release.

C. Notes Collateral Agent agrees to execute this Partial Release in order to evidence the automatic release of its security interest pursuant to the Indenture solely in the Patent Collateral owned by Debtors specified below.

AGREEMENT

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Notes Collateral Agent hereby agrees as follows:

(a) Notes Collateral Agent acknowledges the automatic release of its security interest pursuant to the Indenture and expressly releases all of Notes Collateral Agent's right, title and interest in, to and under the Patents referred to on Schedule A and Schedule B hereto (collectively, the "Patent Collateral").

(b) This Partial Release is made by the Notes Collateral Agent and accepted by the Debtors without representation, covenant or warranty, express or implied, at law or in equity, and without recourse to the Notes Collateral Agent or the Trustee, in any event or in any contingency.

(c) Notes Collateral Agent authorizes the Debtors to deliver this Partial Release to the Patent Division of the United States Patent and Trademark Office and to request the Patent Division of the United States Patent and Trademark Office to record this Partial Release.

(d) This Partial Release applies solely to the Patent Collateral as described above owned by Debtors. The Patent Security Agreement shall continue in full force and effect as between Notes Collateral Agent and Debtors and against all remaining Patents referenced therein.

[Signature Page Follows]

IN WITNESS WHEREOF, Notes Collateral Agent has executed and delivered this Partial Release as of the day and year first above written.

Wells Fargo Bank, National Association,
as Notes Collateral Agent

By: _____
Name: Michael Q. Tu
Title: Vice President

SCHEDULE A

United States
Patents & Patent Applications

Patent / Publication Number	Application Number	Title	Filed Date
6,650,175	10/071,605	Device generating a precise reference voltage	2/8/2002
7,436,232	10/666,142	Regenerative clock repeater	9/17/2003
6,744,291	10/232,636	Power-on reset circuit	8/30/2002
6,809,575	10/407,622	Temperature-compensated current reference circuit	4/3/2003
6,724,241	10/352,733	Variable charge pump circuit with dynamic load	1/27/2003
6,920,527	10/364,583	Portable ram drive	2/11/2003
6,917,105	10/453,157	Integrating chip scale packaging metallization into integrated circuit die structures	6/3/2003
6,900,538	10/760,434	Integrating chip scale packaging metallization into integrated circuit die structures	1/20/2004
7,211,893	10/980,536	Integrating chip scale packaging metallization into integrated circuit die structures	11/3/2004
6,876,244	10/687,980	Differential charge pump	10/16/2003
7,159,766	10/762,767	Peripheral device feature allowing processors to enter a low power state	1/20/2004
7,325,733	11/530,977	Electrically disconnecting a peripheral device	9/12/2006
7,746,216	11/058,056	Method and circuit arrangement for holding a control state during inadequate power supply in an rf transponder or remote sensor	2/14/2005
7,218,167	11/062,888	Electric reference voltage generating device of improved accuracy and corresponding electronic integrated circuit	2/22/2005
6,937,071	10/802,894	High frequency differential power amplifier	3/16/2004
7,120,061	11/061,799	Method and apparatus for a dual power supply to embedded non-volatile memory	2/18/2005
7,450,429	11/539,567	Method and apparatus for a dual power supply to embedded non-volatile memory	10/6/2006
7,075,464	11/137,463	Circuit for current measurement and current monitoring	5/26/2005
7,330,375	11/203,938	Sense amplifier circuit for parallel sensing of four current levels	8/15/2005
7,259,612	11/168,833	Efficient charge pump for a wide range of supply voltages	6/28/2005
7,369,446	11/457,377	Method and apparatus to prevent high voltage supply degradation for high-voltage latches of a non-volatile memory	7/13/2006
7,751,256	11/933,805	Method and apparatus to prevent high voltage supply degradation for high-voltage latches of a non-volatile memory	11/1/2007
7,336,110	11/624,139	Differential amplitude controlled sawtooth generator	1/17/2007
7,800,419	12/014,261	Differential amplitude controlled sawtooth generator	1/15/2008

Patent / Publication Number	Application Number	Title	Filed Date
7,671,642	11/610,107	Amplitude controlled sawtooth generator	12/13/2006
7,453,725	11/539,564	Apparatus for eliminating leakage current of a low vt device in a column latch	10/6/2006
7,417,904	11/554,797	Adaptive gate voltage regulation	10/31/2006
7,423,928	11/668,844	Clock circuitry for ddr-sdram memory controller	1/30/2007
7,679,987	12/207,147	Clock circuitry for ddr-sdram memory controller	9/9/2008
7,508,266	11/846,959	Method for enhancing linearity of a transistor amplifier using switched capacitive loads	8/29/2007
7,876,540	12/174,802	Adaptive electrostatic discharge (esd) protection of device interface for local interconnect network (lin) bus and the like	7/17/2008
7,885,047	12/174,903	Adaptive electrostatic discharge (esd) protection of device interface for local interconnect network (lin) bus and the like	7/17/2008
8,112,699	12/031,289	Error detecting/correcting scheme for memories	2/14/2008
8,214,729	13/335,725	Error detecting/correcting scheme for memories	12/22/2011
7,646,063	11/451,610	Compact cmos esd layout techniques with either fully segmented salicide ballasting (fssb) in the source and/or drain regions	6/12/2006
7,843,232	12/395,518	Dual mode, single ended to fully differential converter structure	2/27/2009
8,223,056	12/436,620	Cyclic digital to analog converter	5/6/2009
WO 2005/001891	PCT/US04/15616	Regenerative clock repeater	
	PCT/US03/28835	Temperature-compensated current reference circuit	
	PCT/US03/31058	Variable charge pump circuit with dynamic load	
	PCT/US2005/009865	Method and apparatus for a dual power supply to embedded non-volatile memory	
	PCT/US06/013794	Sense amplifier circuit for parallel sensing of four current levels	
	PCT/US06/021815	Efficient charge pump for a wide range of supply voltages	
	PCT/US2007/071941	Method and apparatus to prevent high voltage supply degradation for high-voltage latches of a non-volatile memory	
	PCT/US2007/087304	Amplitude controlled sawtooth generator	
WO2008/055183	PCT/US2007/083062	Adaptive gate voltage regulation	10/30/2007
	PCT/US08/52405	Clock circuitry for ddr-sdram memory controller	
	60/823,839	Method for enhancing linearity of a transistor amplifier using switched capacitive loads	8/29/2006
	60/989,514	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like	
WO 09/067673	PCT/US08/84365	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like	

Patent / Publication Number	Application Number	Title	Filed Date
WO 09/067672	PCT/US08/084362	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like	
	60/690,701	Compact cmos esd layout techniques with either fully segmented salicide ballasting (fssb) in the source and/or drain regions	6/15/2005
7,985,644	12/606,691	METHODS FOR FORMING FULLY SEGMENTED SALICIDE BALLASTING (FSSB) IN THE SOURCE AND/OR DRAIN REGION	
	PCT/US08/51209	Differential amplitude controlled sawtooth generator	
7,007,172	09/870,460	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	6/1/2001
7,243,372	11/135,527	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	5/23/2005
7,199,603	10/946,432	Increment/Decrement, Chip Select and Selectable Write to Non-Volatile Memory Using a Two Signal Control Protocol for an Integrated Circuit Device	9/21/2004
7,336,542	11/049,334	Nonvolatile Latch	2/1/2005
6,792,065	10/348,782	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	1/21/2003
7,102,950	10/910,038	Fuse Data Storage System Using Core Memory	8/2/2004
8,193,792	12/481,330	Circuit and Method for Operating a Circuit	6/9/2009
8,415,939	13/485,426	Circuit and Method for Operating a Circuit	5/31/2012
7,908,516	12/017,521	Low Power Mode Fault Recovery Method, System and Apparatus	1/22/2008
8,289,082	12/977,034	Circuit and Method for Adjusting an Offset Output Current for an Input Current Amplifier	12/22/2010
8,947,164	13/89221	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/14/2013
WO2006/020357	PCT/US05/026205	Fuse Data Storage System Using Core Memory	7/25/2005
	PCT/US2006/002914	Nonvolatile Latch	1/27/2006
WO02/099647	PCT/US02/16705	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	5/29/2002
WO06/014860	PCT/US05/026259	Increment/Decrement, Chip Select and Selectable Write to Non-Volatile Memory Using a Two Signal Control Protocol for an Integrated Circuit Device	7/25/2005

Patent / Publication Number	Application Number	Title	Filed Date
WO2004/068273	PCT/US03/40000	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003
	61/060,626	Schaltung und Verfahren zum Betrieb einer Schaltung	6/11/2008
	60/593,035	Selectable Write To Non-Volatile Memory Using An Increment/Decrement Serial Protocol	7/30/2004
	PCT/US08/58196	Low Power Mode Fault Recovery Method, System and Apparatus	3/26/2008
	PCT/US2013/041202	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/15/2013
	60/908,328	Low Power Mode Fault Recovery Method, System and Apparatus	3/27/2007
	61/289,846	Eingangsstromverstärker mit Offset Kalibrierung für Touchscreen Applikation	12/23/2009
8,760,227	13/652,166	Circuit and Method for Adjusting an Offset Output Current for an Input Current Amplifier	10/15/2012
	61/64721	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/18/2012

SCHEDULE B

Foreign
Patents & Patent Applications

Patent / Publication Number	Application Number	Title	Filed Date	Country Code
ITMI20031217	IT2003MI01217	Ripetitore rigenerativo di temporizzazione	6/17/2003	IT
TW200502734	TW20040116615	Regenerative clock repeater, synchronous semiconductor memory device comprising the same and method thereof	6/10/2004	TW
ITTO20020803	IT2002TO00803	Circuito di riferimento di corrente compensato in temperatura.	9/16/2002	IT
TW200417133	TW20030125338	Temperature-compensated current reference circuit	9/15/2003	TW
JP2005539335	JP20040572005	Current reference circuit is a temperature compensated	9/12/2003	JP
NO20051558	NO20050001558	Temperature-compensated current reference circuit	3/23/2005	NO
EP1559186	EP20030773076	Variable charge pump circuit with dynamic load	9/30/2003	EP
ITMI20022268	IT2002MI02268	Circuito pompa di cariche variabile con carico dinamico	10/25/2002	IT
NO20052473	NO20050002473	Variabel ladningspumpekrets med dynamisk last.	5/23/2005	NO
TWI301245	TW20050101565	System and method of processor regulation	1/19/2005	TW
DE102004007106	DE20041007106	Circuit arrangement, in particular for use in rf - transponders or remote sensors	2/13/2004	DE
ES2293476	ES20050101272T	Device for generating a reference voltage of improved precision and corresponding integrated electronic circuit.	2/18/2005	ES
DE102004036352	DE20041036352	Circuit for current measurement and current monitoring and their use for a functional unit	7/27/2004	DE
TW200703332	TW20060115862	Sense amplifier circuit for parallel sensing of four current levels	5/4/2006	TW
EP1899785	EP20060772215	Efficient charge pump for a wide range of supply voltages	6/5/2006	EP
DE602006015962	DE20066015962T	Efficient charge pump for a variety of supply voltages	6/5/2006	DE
CN101490764	CN2007826653	Method and apparatus to prevent high voltage supply degradation for high-voltage latches of a non-volatile memory	6/22/2007	CN
EP2041751	EP20070784521	Method and apparatus to prevent high voltage supply degradation for high-voltage latches of a non-volatile memory	6/22/2007	DE
TWI450272	TW20070123964	High-voltage cmos latch for non-volatile memory and method therefor	7/2/2007	TW
JP2009544109	JP20090519574	Method and the device in order to prevent the high tension source deterioration of high tension latch of non-volatile memory	6/22/2007	JP

Patent / Publication Number	Application Number	Title	Filed Date	Country Code
CN101584117	CN2008802525	Differential amplitude controlled sawtooth generator	1/16/2008	CN
TW200841596	TW20070147415	Amplitude controlled sawtooth generator	12/12/2007	TW
TW200832431	TW20070141032	Adaptive gate voltage regulation	10/31/2007	TW
TW200847184	TW20080103582	Clock circuitry for ddr-sdram memory controller	1/30/2008	TW
TWI455433	TW20080144927	Integrated circuit device having adaptive electrostatic discharge (esd) protection and noise signal rejection	11/20/2008	TW
TWI435436	TW20080144926	Adaptive electrostatic discharge (esd) protection of device interface for local interconnect network (lin) bus and the like	11/20/2008	TW
CN101842954	CN20088113858	Adaptive electrostatic discharge (esd) protection of device interface for local interconnect network (lin) bus and the like	11/21/2008	CN
KR101576261	KR20107009462	Adaptive electrostatic discharge(esd) protection of device interface for local interconnect network(lin) bus and the like	11/21/2008	KR
KR101467441	KR20107008914	Adaptive electrostatic discharge(esd) protection of device interface for local interconnect network(lin) bus and the like	11/21/2008	KR
CN101842955	CN20088113868	Adaptive electrostatic discharge (esd) protection of device interface for local interconnect network (lin) bus and the like	11/21/2008	CN
EP2212981	EP20080851188	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like	11/21/2008	EP
FR2212981	FR20080851188	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like		FR
NL2212981	NL20080851188	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like		NL
EP2212982	EP20080852419	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like	11/21/2008	EP
FR2212982	FR20080852419	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like		FR
NL2212982	NL20080852419	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like		NL
AT540460	AT20080851188T	Adaptiver schutz vor elektrostatischer entladung einer gerÃ„teschnittstelle fÃœr einen local interconnect network (lin)-bus und Ã„hnliches	11/21/2008	AT

Patent / Publication Number	Application Number	Title	Filed Date	Country Code
AT540461	AT20080852419T	Adaptiver schutz vor elektrostatischer entladung einer gerÃ„teschnittstelle fÃœr einen local interconnect network (lin)-bus und dergleichen	11/21/2008	AT
TW200947449	TW20090104737	Error detecting/correcting scheme for memories	2/13/2009	TW
GB1231529	GB2290301.7	Device generating a precise reference voltage		GB
IT1231529	IT2290301.7	Device generating a precise reference voltage		IT
EP1231529	EP2290301.7	Device generating a precise reference voltage		EP
FR0101821	FR01/01821	Device generating a precise reference voltage		FR
NL1231529	NL2290301.7	Device generating a precise reference voltage		NL
DE60212217.1	DE2290301.7	Device generating a precise reference voltage		DE
CNZL200480016980.9	CN200480016980.9	Regenerative clock repeater		CN
GB1636903	GB04752608.2	Regenerative clock repeater		GB
FR1636903	FR04752608.2	Regenerative clock repeater		FR
EP1636903	EP04752608.2	Regenerative clock repeater		EP
DE1636903	DE04752608.2	Regenerative clock repeater		DE
	CA2498780	Temperature-compensated current reference circuit		CA
	CN3821947.6	Temperature-compensated current reference circuit		CN
	EP3749655.1	Temperature-compensated current reference circuit		EP
	KR05-7004509	Temperature-compensated current reference circuit		DR
	HK6105446.3	Temperature-compensated current reference circuit		HK
GB1559186	GB03773 076.9	Variable charge pump circuit with dynamic load		GB
FR1559186	FR03773 076.10	Variable charge pump circuit with dynamic load		FR
DE1559186	DE03773 076.11	Variable charge pump circuit with dynamic load		DE
TWI239437	TW 92128687	Variable charge pump circuit with dynamic load		TW
	JP548342/2004	Variable charge pump circuit with dynamic load		JP
	CA2501564	Variable charge pump circuit with dynamic load		CA
	KR1020057006834	Variable charge pump circuit with dynamic load		KR
	CN03824590.6	Variable charge pump circuit with dynamic load		CN
	JP200513353	Peripheral device feature allowing processors to enter a low power state		JP
CNZL200510008328.9	CN200510008328.9	RF Responder or Circuit Arrangement Used in Remote Sensor and Control Method Thereof		CN
GB1566717	GB5101272.2	Electric reference voltage generating device of improved accuracy and corresponding electronic integrated circuit		GB
IT1566717	IT5101272.2	Electric reference voltage generating device of improved accuracy and corresponding electronic integrated circuit		IT

Patent / Publication Number	Application Number	Title	Filed Date	Country Code
FR2866724	FR401753	Electric reference voltage generating device of improved accuracy and corresponding electronic integrated circuit		FR
FR1566717	FR5101272.2	Electric reference voltage generating device of improved accuracy and corresponding electronic integrated circuit		FR
NL1566717	NL5101272.2	Electric reference voltage generating device of improved accuracy and corresponding electronic integrated circuit		NL
DE602005002160.4	DE5101272.2	Electric reference voltage generating device of improved accuracy and corresponding electronic integrated circuit		DE
TWI373767	TW94110507	Method and apparatus for a dual power supply to embedded non-volatile memory		TW
	CN200580010125.1	Method and apparatus for a dual power supply to embedded non-volatile memory		CN
EP1747559	EP05729910.9	Method and apparatus for a dual power supply to embedded non-volatile memory		EP
	GB05729910.10	Method and apparatus for a dual power supply to embedded non-volatile memory		GB
	IT05729910.11	Method and apparatus for a dual power supply to embedded non-volatile memory		IT
	DE05729910.12	Method and apparatus for a dual power supply to embedded non-volatile memory		DE
FR2871281	FR0403434	Method and apparatus for a dual power supply to embedded non-volatile memory		FR
	DE102004026537.2	Circuit for current measurement and current monitoring		DE
FR2885726	FR0504737	Sense amplifier circuit for parallel sensing of four current levels		FR
	HK8112890.8	Efficient charge pump for a wide range of supply voltages		HK
TWI391805	TW95122704	Efficient charge pump for a wide range of supply voltages		TW
CNZL200680023594.1	CN200680023594.1	Efficient charge pump for a wide range of supply voltages		CN
	KR1020087001004	Efficient charge pump for a wide range of supply voltages		KR
	JP2008519317	Efficient charge pump for a wide range of supply voltages		JP
DE2041751	DE602007039627.1	Method and apparatus to prevent high voltage supply degradation for high-voltage latches of a non-volatile memory	6/22/2007	DE
	KR1020097002888	Method and apparatus to prevent high voltage supply degradation for high-voltage latches of a non-volatile memory		KR

Patent / Publication Number	Application Number	Title	Filed Date	Country Code
	HK91080324	Method and apparatus to prevent high voltage supply degradation for high-voltage latches of a non-volatile memory		HK
DE2212981	DE20080851188	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like	11/21/2008	DE
DE2212982	DE20080852419	Adaptive electrostatic discharge (esd) protection of device interface for a local interconnect network (lin) bus and the like	11/21/2008	DE
CN200910006300.X	CN20091006300X	Error detecting/correcting scheme for memories		CN
DE112008000205	DE112008000205.3	Differential amplitude controlled sawtooth generator	1/16/2009	DE
TWI470932	TW97101741	Differential amplitude controlled sawtooth generator	1/16/2008	TW
DE1393183	DE02734553.7	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	5/29/2002	DE
FR1393183	FR02734553.7	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	5/29/2002	FR
GB1393183	GB02734553.7	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	5/29/2002	GB
IT1393183	IT02734553.7	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	5/29/2002	IT
NL1393183	NL02734553.7	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	5/29/2002	NL
TWNI187545	TW91111712	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	5/31/2002	TW

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CNZL200580025624.8	CN80025624.8	Increment/Decrement, Chip Select and Selectable Write to Non-Volatile Memory Using a Two Signal Control Protocol for an Integrated Circuit Device	7/25/2005	CN
DE1779389	DE05775227.1	Increment/Decrement, Chip Select and Selectable Write to Non-Volatile Memory Using a Two Signal Control Protocol for an Integrated Circuit Device	7/25/2005	DE
FR1779389	FR05775227.1	Increment/Decrement, Chip Select and Selectable Write to Non-Volatile Memory Using a Two Signal Control Protocol for an Integrated Circuit Device	7/25/2005	FR
KR911013	KR2007-7004472	Increment/Decrement, Chip Select and Selectable Write to Non-Volatile Memory Using a Two Signal Control Protocol for an Integrated Circuit Device	7/25/2005	KR
NL1779389	NL05775227.1	Increment/Decrement, Chip Select and Selectable Write to Non-Volatile Memory Using a Two Signal Control Protocol for an Integrated Circuit Device	7/25/2005	NL
TWI340977	TW094125800	Increment/Decrement, Chip Select and Selectable Write to Non-Volatile Memory Using a Two Signal Control Protocol for an Integrated Circuit Device	7/29/2005	TW
DE1844474	DE06719670.9	Nonvolatile Latch	1/27/2006	DE
DE60313807.1	DE03815650.1	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	DE
DE602005016563.0	DE602005016563.0	Fuse Data Storage System Using Core Memory	7/25/2005	DE
DE102008027392	DE102008027392.9	A circuit and method for the operation of a circuit	6/9/2008	DE
CNZL200910139122.8	CN2009101391228	Schaltung und Verfahren zum Betrieb einer Schaltung	5/7/2009	CN
TWI465895	TW97110245	Low Power Mode Fault Recovery Method, System and Apparatus	3/21/2008	TW
CNZL200880009922.1	CN80009922.1	Low Power Mode Fault Recovery Method, System and Apparatus	3/26/2008	CN
DE2130123	DE8744355.2	Low Power Mode Fault Recovery Method, System and Apparatus	3/26/2008	DE
FR2130123	FR8744355.2	Low Power Mode Fault Recovery Method, System and Apparatus	3/26/2008	FR
NL2130123	NL8744355.2	Low Power Mode Fault Recovery Method, System and Apparatus	3/26/2008	NL
DE102009060504	DE102009060504.5-35	Schaltung und Verfahren zur Einstellung eines Offset-Ausgangsstroms für einen Eingangsstromverstärker	12/23/2009	DE
CNZL201010606149.6	CN201010606149.6	Circuit and Method for Adjusting an Offset Output Current for an Input Current Amplifier	12/23/2010	CN

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CNZL201380025819.7	CN201380025819.7	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/15/2013	CN
DE2850728	DE13728021	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/15/2013	DE
FR2850728	FR13728021	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/15/2013	FR
GB2850728	GB13728021	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/15/2013	GB
KR10-1911585	KR10-2014-7035569	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/15/2013	KR
TWI-603578	TW102117502	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/17/2013	TW
	CA2513734	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	CA
CNZL200580033533.9	CN200580033533.9	Fuse Data Storage System Using Core Memory	7/25/2005	CN
CNZL200680003699.0	CN200680003699.0	Non-Volatile Latch	1/27/2006	CN
CNZL200380109892.9	CN200380109892.9	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	CN
DE602005016563	DE05776656.0	Fuse Data Storage System Using Core Memory	7/25/2005	DE
EP1774529	EP05776656.0	Fuse Data Storage System Using Core Memory	7/25/2005	EP
	EP09007531.8-1233	Schaltung und Verfahren zum Betrieb einer Schaltung	6/8/2009	EP
EP1844474	EP06719670.9	Nonvolatile Latch	1/27/2006	EP
EP1393183	EP02734553.7	MODIFIED HARVARD ARCHITECTURE PROCESSOR HAVING DATA MEMORY SPACE MAPPED TO PROGRAM MEMORY SPACE WITH ERRONEOUS EXECUTION PROTECTION	5/29/2002	EP
EP1779389	EP05775227.1	Increment/Decrement, Chip Select and Selectable Write to Non-Volatile Memory Using a Two Signal Control Protocol for an Integrated Circuit Device	7/25/2005	EP
EP1588320	EP3815650.1	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	EP
	FR05776656.0	Fuse Data Storage System Using Core Memory	7/25/2005	FR
	FR06719670.9	Nonvolatile Latch	1/27/2006	FR
FR1588320	FR3815650.1	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	FR
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GB1588320	GB3815650.1	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	GB
	IT05776656.0	Fuse Data Storage System Using Core Memory	7/25/2005	IT
IT1588320	IT3815650.1	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	IT

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	KR10-2005-7013506	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	KR
NL1588320	NL3815650.1	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	NL
	NO20053908	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	12/16/2003	NO
TWI371032	TW94126047	Fuse Data Storage System Using Core Memory	8/1/2005	TW
TWI319883	TW95103411	Nonvolatile Latch	1/27/2006	TW
	TW93100123	Method for Counting Beyond Endurance Limitations of Non-Volatile Memories	1/5/2004	TW
EP2130123	EP8744355.2	Low Power Mode Fault Recovery Method, System and Apparatus	3/26/2008	EP
EP2850728	EP13728021	Integrated Technique for Enhanced Power Amplifier Forward Power Detection	5/15/2013	EP