PATENT ASSIGNMENT COVER SHEET

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NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
STATS CHIPPAC PTE. LTD.	11/28/2019

RECEIVING PARTY DATA

Name:	JCET SEMICONDUCTOR (SHAOXING) CO., LTD.
Street Address:	NO. 500 LINJIANG ROAD
Internal Address:	YUECHENG DISTRICT
City:	SHAOXING
State/Country:	CHINA

PROPERTY NUMBERS Total: 2

Property Type	Number
Application Number:	16558135
Application Number:	16570049

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DATE SIGNED:	01/08/2020

Total Attachments: 11
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PATENT ASSIGNMENT AND AGREEMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, STATS CHIPPAC PTE. LTD. (STATS CHIPPAC), a Private Limited company, organized under the laws of Singapore, located at 5 Yishun Street 23, Singapore 768442, has sold, assigned, and transferred, and does hereby sell, assign, and transfer unto JCET SEMICONDUCTOR (SHAOXING) CO., LTD., a Company, organized under the laws of the People's Republic of China, located at No. 500 Linjiang Road, Yuecheng District, Shaoxing, China, and its successors, assigns, and legal representatives, the entire right, title, and interest for the United States of America in and to certain inventions which are described, illustrated, and claimed in Appendix A and Appendix B to the foregoing Patent Assignment and Agreement, together with the entire right, title and interest in and to the applications, and any continuation, division, reissue, reexamination, extension, renewal, or substitute thereof, and in and to any patent which may grant upon such applications. JCET SEMICONDUCTOR hereby agrees and accepts the foregoing Patent Assignment and Agreement.

STATS CHIPPAC agrees that, when requested, STATS CHIPPAC will without charge to JCET SEMICONDUCTOR, but at its expense, sign all papers, take all rightful oaths, and do all acts which may be necessary, desirable, and convenient for applying , securing, and maintaining patents for the inventions in the United States for vesting title thereto in JCET SEMICONDUCTOR, its successors, assigns, and legal representatives or nominees.

STATS CHIPPAC covenants with JCET SEMICONDUCTOR, its successors, assigns, and legal representatives that the interest and property hereby conveyed is free from all prior assignment, grant, mortgage, license, or other encumbrance.

ASSIGNOR:
STATS CHIPPAC PTE. LTD.

By: [signature]
Name: SHAN ZHENGANG
Title: General Legal Counsel
Date: NOV. 28 2019

ASSIGNEE:
JCET SEMICONDUCTOR (SHAOXING) CO., LTD.

By: [signature]
Name: Zhang Li
Title: General Manager
Date: 2019. 11. 29

APPENDIX A
PATENT ASSIGNMENT AND AGREEMENT

No.	Reference No.	Patent No.	Application No.	Title
1	ST03-010	7,306,133	10/825,810	SYSTEM FOR FABRICATING AN INTEGRATED CIRCUIT PACKAGE ON A PRINTED CIRCUIT BOARD
2	ST02-015	7,006,375	10/846,176	METHOD OF MANUFACTURING DIFFERENT BOND PADS ON THE SAME SUBSTRATE OF AN INTEGRATED CIRCUIT PACKAGE
3	SC-P04-002	7,381,634	10/907,732	INTEGRATED CIRCUIT SYSTEM FOR BONDING
4	ST04-034	7,410,824	11/009,436	METHOD FOR SOLDER BUMPING, AND SOLDER-BUMPING STRUCTURES PRODUCED THEREBY
5	SC-P04-003	7,566,650	11/162,822	INTEGRATED CIRCUIT SOLDER BUMPING SYSTEM
6	ST03-026	7,304,859	11/277,973	CHIP CARRIER AND FABRICATION METHOD
7	ST02-018.D1	7,443,039	11/306,352	SYSTEM FOR DIFFERENT BOND PADS IN AN INTEGRATED CIRCUIT PACKAGE
8	SC-P05-023	7,414,310	11/307,363	WAFERSCALE PACKAGE SYSTEM
9	SC-P05-085	7,851,257	11/538,806	INTEGRATED CIRCUIT STACKING SYSTEM WITH INTEGRATED PASSIVE COMPONENTS
10	SC-P05-084	8,669,637	11/553,949	INTEGRATED PASSIVE DEVICE SYSTEM
11	SC-P05-068	8,006,770	11/556,035	INTEGRATED CIRCUIT PACKAGE SYSTEM WITH BUMP PAD
12	SC-P06-118	8,178,962	11/618,806	DUAL MOLDED MULTI-CHIP PACKAGE SYSTEM
13	SC-P06-006	7,723,225	11/671,900	SOLDER BUMP CONFINEMENT SYSTEM FOR AN INTEGRATED CIRCUIT PACKAGE
14	SC-P06-148	7,682,959	11/689,282	METHOD OF FORMING SOLDER BUMP ON HIGH TOPOGRAPHY PLATED CU
15	SC-P06-151	7,727,879	11/689,319	METHOD OF FORMING TOP ELECTRODE FOR CAPACITOR AND INTERCONNECTION IN INTEGRATED PASSIVE DEVICE (IPD)
16	SC-P06-129	8,026,593	11/694,907	INTEGRATED CIRCUIT PACKAGE SYSTEM WITH PROTECTED CONDUCTIVE LAYERS FOR PADS AND METHOD OF MANUFACTURING THEREOF
17	SC-P06-187	7,955,160	11/734,410	COMPACT COILS FOR HIGH PERFORMANCE FILTERS
18	SC-P06-168	8,106,499	11/757,889	SEMICONDUCTOR PACKAGING SYSTEM WITH STACKING AND METHOD OF MANUFACTURE THEREOF
19	SC-P07-021	7,629,860	11/760,207	MINIATURIZED WIDE-BAND BALUNS FOR RF APPLICATIONS
20	SC-P07-047	7,553,752	11/765,939	METHOD OF MAKING A WAFER LEVEL INTEGRATION PACKAGE
21	SC-P07-042	8,445,325	11/768,825	PACKAGE-IN-PACKAGE USING THROUGH-HOLE VIA DIE ON SAW STREETS
22	SC-P07-043	7,725,159	11/768,844	PACKAGE-ON-PACKAGE USING THROUGH-HOLE VIA DIE ON SAW STREETS
23	SC-P07-044	7,750,452	11/768,869	SAME SIZE DIE STACKED PACKAGE HAVING THROUGH-HOLE VIAS FORMED IN ORGANIC MATERIAL
24	SC-P06-111	7,863,706	11/770,690	CIRCUIT SYSTEM WITH CIRCUIT ELEMENT
25	SC-P06-079	8,188,590	11/843,849	INTEGRATED CIRCUIT PACKAGE SYSTEM WITH POST-PASSIVATION INTERCONNECTION AND INTEGRATION
26	SC-P07-048	7,667,335	11/856,749	SEMICONDUCTOR PACKAGE WITH PASSIVATION ISLAND FOR REDUCING STRESS ON SOLDER BUMPS
27	SC-P07-098	8,039,960	11/859,416	SOLDER BUMP WITH INNER CORE PILLAR IN SEMICONDUCTOR PACKAGE
28	SC-P07-100	7,701,040	11/860,377	SEMICONDUCTOR PACKAGE AND METHOD OF REDUCING ELECTROMAGNETIC INTERFERENCE BETWEEN DEVICES
29	SC-P07-113	7,585,750	11/861,233	SEMICONDUCTOR PACKAGE HAVING THROUGH-HOLE VIA ON SAW STREETS FORMED WITH PARTIAL SAW
30	SC-P07-115	7,829,998	11/861,244	SEMICONDUCTOR WAFER HAVING THROUGH-HOLE VIAS ON SAW STREETS WITH BACKSIDE REDISTRIBUTION LAYER
31	SC-P07-114	7,902,638	11/861,251	SEMICONDUCTOR DIE WITH THROUGH-HOLE VIA ON SAW STREETS AND THROUGH-HOLE VIA IN ACTIVE AREA OF DIE
32	ST03-026	7,525,812	11/877,613	CHIP CARRIER AND FABRICATION METHOD
33	SC-P06-147	7,727,876	11/934,009	SEMICONDUCTOR DEVICE AND METHOD OF PROTECTING PASSIVATION LAYER IN A SOLDER BUMP PROCESS
34	SC-P07-089	7,772,106	11/936,461	METHOD OF FORMING AN INDUCTOR ON A SEMICONDUCTOR WAFER
35	SC-P07-161	7,790,576	11/947,377	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THROUGH HOLE VIAS IN DIE EXTENSION REGION AROUND PERIPHERY OF DIE
36	SC-P07-220	8,409,970	11/949,255	SEMICONDUCTOR DEVICE AND METHOD OF MAKING INTEGRATED PASSIVE DEVICES
37	SC-P07-236	7,838,395	11/951,729	SEMICONDUCTOR WAFER LEVEL INTERCONNECT PACKAGE UTILIZING CONDUCTIVE RING AND PAD FOR SEPARATE VOLTAGE SUPPLIES AND METHOD OF MAKING THE SAME
38	SC-P07-147	8,039,302	11/952,502	SEMICONDUCTOR PACKAGE AND METHOD OF FORMING SIMILAR STRUCTURE FOR TOP AND BOTTOM BONDING PADS

39	SC-P07-160	7,851,246	11/965,160	SEMICONDUCTOR DEVICE WITH OPTICAL SENSOR AND METHOD OF FORMING INTERCONNECT STRUCTURE ON FRONT AND BACKSIDE OF THE DEVICE
40	SC-P07-386	8,722,457	11/965,383	SYSTEM AND APPARATFOR WAFER LEVEL INTEGRATION OF COMPONENTS
41	SC-P07-088	9,466,577	12/035,843	SEMICONDUCTOR INTERCONNECT STRUCTURE WITH STACKED VIAS SEPARATED BY SIGNAL LINE AND METHOD THEREFOR
42	SC-P07-292	8,084,302	12/044,803	SEMICONDUCTOR PACKAGE HAVING SEMICONDUCTOR DIE WITH INTERNAL VERTICAL INTERCONNECT STRUCTURE AND METHOD THEREFOR
43	SC-P07-117	7,749,814	12/047,840	SEMICONDUCTOR DEVICE WITH INTEGRATED PASSIVE CIRCUIT AND METHOD OF MAKING THE SAME USING SACRIFICIAL SUBSTRATE
44	SC-P07-258	8,269,308	12/051,253	SEMICONDUCTOR DEVICE WITH CROSS-TALK ISOLATION USING M-CAP AND METHOD THEREOF
45	SC-P07-257	7,880,293	12/055,171	WAFER INTEGRATED WITH PERMANENT CARRIER AND METHOD THEREFOR
46	SC-P07-344	8,072,079	12/057,199	THROUGH HOLE VIAS AT SAW STREETS INCLUDING PROTRUSIONS OR RECESSES FOR INTERCONNECTION
47	SC-P07-348	7,964,450	12/126,548	WIREBONDLESS WAFER LEVEL PACKAGE WITH PLATED BUMPS AND INTERCONNECTS
48	SC-P07-163	7,863,721	12/137,242	METHOD AND APPARATFOR WAFER LEVEL INTEGRATION USING TAPERED VIAS
49	SC-P08-051	7,906,839	12/167,039	SEMICONDUCTOR DEVICE AND METHOD OF SHUNT TEST MEASUREMENT FOR PASSIVE CIRCUITS
50	SC-P08-107	7,772,080	12/167,146	SEMICONDUCTOR DEVICE AND METHOD OF PROVIDING ELECTROSTATIC DISCHARGE PROTECTION FOR INTEGRATED PASSIVE DEVICES
51	SC-P08-087 & SC-P08-088	7,858,145	12/172,817	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STEPPED-DOWN RDL AND RECESSED THV IN PERIPHERAL REGION OF THE DEVICE
52	SC-P07-309 & SC-P07-199	8,309,451	12/182,283	SEMICONDUCTOR DEVICE AND METHOD OF PROVIDING COMMON VOLTAGE BAND WIRE BONDABLE REDISTRIBUTION
53	SC-P08-073	9,324,700	12/256,727	SEMICONDUCTOR DEVICE AND METHOD OF FORMING SHIELDING LAYER OVER INTEGRATED PASSIVE DEVICE USING CONDUCTIVE MATERIAL
54	SC-P07-120	8,129,845	12/207,324	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT STRUCTURE IN NON-ACTIVE AREA OF WAFER
55	SC-P08-171	7,838,337	12/325,587	SEMICONDUCTOR DEVICE AND METHOD OF FORMING AN INTERPOSER PACKAGE WITH THROUGH SILICON VIAS
56	SC-P08-199	8,354,304	12/329,430	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE POSTS EMBEDDED IN PHOTOSENSITIVE ENCAPSULANT
57	SC-P07-378 & SC-P08-043	8,576,026	12/331,492	SEMICONDUCTOR DEVICE HAVING BALANCED BAND-PASS FILTER IMPLEMENTED WITH LC RESONATOR
58	SC-P08-175	7,935,570	12/331,898	SEMICONDUCTOR DEVICE AND METHOD OF EMBEDDING INTEGRATED PASSIVE DEVICES INTO THE PACKAGE ELECTRICALLY INTERCONNECTED USING CONDUCTIVE PILLARS
59	SC-P08-172	7,741,148	12/332,118	SEMICONDUCTOR DEVICE AND METHOD OF FORMING AN INTERCONNECT STRUCTURE FOR 3-D DEVICES USING ENCAPSULANT FOR STRUCTURAL SUPPORT
60	SC-P08-069	7,799,602	12/332,277	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SHIELDING LAYER OVER A SEMICONDUCTOR DIE AFTER FORMING A BUILD-UP INTERCONNECT STRUCTURE
61	SC-P08-295	8,017,515	12/332,325	SEMICONDUCTOR DEVICE AND METHOD OF FORMING COMPLIANT POLYMER LAYER BETWEEN UBM AND CONFORMAL DIELECTRIC LAYER/RDL FOR STRESS RELIEF
62	SC-P08-287	7,642,128	12/333,977	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A VERTICAL INTERCONNECT STRUCTURE FOR 3-D FO-WLCSP
63	SC-P08-256	7,786,008	12/334,347	INTEGRATED CIRCUIT PACKAGING SYSTEM HAVING THROUGH SILICON VIAS WITH PARTIAL DEPTH METAL FILL REGIONS AND METHOD OF MANUFACTURE THEREOF
64	ST03-026	7,733,661	12/393,034	CHIP CARRIER AND FABRICATION METHOD
65	SC-P08-290	8,035,458	12/403,234	SEMICONDUCTOR DEVICE AND METHOD OF INTEGRATING BALUN AND RF COUPLER ON A COMMON SUBSTRATE
66	SC-P08-320 & SC-P08-321	8,258,010	12/406,038	MAKING A SEMICONDUCTOR DEVICE HAVING CONDUCTIVE THROUGH ORGANIC VIAS
67	SC-P08-362	7,989,356	12/410,280	SEMICONDUCTOR DEVICE AND METHOD OF FORMING ENHANCED UBM STRUCTURE FOR IMPROVING SOLDER JOINT RELIABILITY
68	SC-P08-423	8,163,597	12/410,312	SEMICONDUCTOR DEVICE AND METHOD OF FORMING NO-FLOW UNDERFILL MATERIAL AROUND VERTICAL INTERCONNECT STRUCTURE
69	SC-P08-432	8,405,228	12/411,154	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH PACKAGE UNDERFILL AND METHOD OF MANUFACTURE THEREOF
70	SC-P08-400	8,378,383	12/411,310	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SHIELDING LAYER BETWEEN STACKED SEMICONDUCTOR DIE
71	SC-P08-259	8,531,015	12/412,279	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A THIN WAFER WITHOUT A CARRIER
72	SC-P08-427	8,003,445	12/412,312	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH Z-INTERCONNECTS HAVING TRACES AND METHOD OF MANUFACTURE THEREOF
73	SC-P08-454	7,955,942	12/467,908	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A 3D INDUCTOR FROM PREFABRICATED PILLAR FRAME
74	SC-P08-353	7,951,663	12/472,170	SEMICONDUCTOR DEVICE AND METHOD OF FORMING IPD STRUCTURE USING SMOOTH CONDUCTIVE LAYER AND BOTTOM-SIDE CONDUCTIVE LAYER
75	SC-P08-185	7,888,184	12/473,233	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH EMBEDDED CIRCUITRY AND POST, AND METHOD OF MANUFACTURE THEREOF
76	SC-P04-003	8,487,438	12/484,099	INTEGRATED CIRCUIT SYSTEM HAVING DIFFERENT-SIZE SOLDER BUMPS AND DIFFERENT-SIZE BONDING PADS
77	SC-P07-047	7,843,042	12/493,108	WAFER LEVEL INTEGRATION PACKAGE
78	SC-P08-426	8,237,252	12/507,130	SEMICONDUCTOR DEVICE AND METHOD OF EMBEDDING THERMALLY CONDUCTIVE LAYER IN INTERCONNECT STRUCTURE FOR HEAT DISSIPATION
79	SC-P07-113	8,017,501	12/533,160	SEMICONDUCTOR PACKAGE HAVING THROUGH-HOLE VIAS ON SAW STREETS FORMED WITH PARTIAL SAW

80	SC-P07-113	8,021,923	12/533,270	SEMICONDUCTOR PACKAGE HAVING THROUGH-HOLE VIAS ON SAW STREETS FORMED WITH PARTIAL SAW
81	SC-P07-113	8,017,521	12/533,344	SEMICONDUCTOR PACKAGE HAVING THROUGH-HOLE VIAS ON SAW STREETS FORMED WITH PARTIAL SAW
82	SC-P08-324	8,587,139	12/534,029	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH THROUGH SILICON VIA BASE AND METHOD OF MANUFACTURE THEREOF
83	SC-P08-052	8,003,496	12/541,334	SEMICONDUCTOR DEVICE AND METHOD OF MOUNTING SEMICONDUCTOR DIE TO HEAT SPREADER ON TEMPORARY CARRIER AND FORMING POLYMER LAYER AND CONDUCTIVE LAYER OVER THE DIE
84	SC-P09-011	9,324,672	12/545,390	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DUAL-ACTIVE SIDED SEMICONDUCTOR DIE IN FAN-OUT WAFER LEVEL CHIP SCALE PACKAGE
85	SC-P09-036	9,397,050	12/551,270	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PRE-MOLDED SEMICONDUCTOR DIE HAVING BUMPS EMBEDDED IN ENCAPSULANT
86	SC-P08-022	8,356,179	12/557,352	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DIRECTIONAL RF COUPLER WITH IPD FOR ADDITIONAL RF SIGNAL PROCESSING
87	SC-P09-093	8,143,097	12/565,380	SEMICONDUCTOR DEVICE AND METHOD OF FORMING OPEN CAVITY IN TSV INTERPOSER TO CONTAIN SEMICONDUCTOR DIE IN WLCSMP
88	SC-P09-113	8,883,559	12/567,033	SEMICONDUCTOR DEVICE AND METHOD OF FORMING ADHESIVE MATERIAL TO SECURE SEMICONDUCTOR DIE TO CARRIER IN WLCSP
89	SC-P08-287	8,736,846	12/572,590	SEMICONDUCTOR DEVICE WITH A VERTICAL INTERCONNECT STRUCTURE FOR 3-D FO-WLCSP
90	SC-P07-021	8,564,382	12/579,286	MINIATURIZED WIDE-BAND BALUNS FOR RF APPLICATIONS
91	SC-P07-021	8,803,630	12/579,299	MINIATURIZED WIDE-BAND BALUNS FOR RF APPLICATIONS
92	SC-P07-021	8,328,154	12/579,307	MINIATURIZED WIDE-BAND BALUNS FOR RF APPLICATIONS
93	SC-P08-266	8,592,973	12/580,933	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH PACKAGE-ON-PACKAGE STACKING AND METHOD OF MANUFACTURE THEREOF
94	SC-P07-021	8,823,496	12/606,351	MINIATURIZED WIDE-BAND BALUNS FOR RF APPLICATIONS
95	SC-P08-456	8,916,452	12/612,936	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WLCSP USING WAFER SECTIONS CONTAINING MULTIPLE DIE
96	SC-P07-258	7,923,295	12/615,428	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THE DEVICE USING SACRIFICIAL CARRIER
97	SC-P09-091	8,158,510	12/621,738	SEMICONDUCTOR DEVICE AND METHOD OF FORMING IPD ON MOLDED SUBSTRATE
98	SC-P09-121	8,034,661	12/625,975	SEMICONDUCTOR DEVICE AND METHOD OF FORMING COMPLIANT STRESS RELIEF BUFFER AROUND LARGE ARRAY WLCSP
99	SC-P08-075	8,575,018	12/628,631	SEMICONDUCTOR DEVICE AND METHOD OF FORMING BUMP STRUCTURE WITH MULTI-LAYER UBM AROUND BUMP FORMATION AREA
100	SC-P08-087 & SC-P08-088	8,080,882	12/641,958	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STEPPED-DOWN RDL AND RECESSED THV IN PERIPHERAL REGION OF THE DEVICE
101	SC-P07-048	7,968,445	12/651,756	SEMICONDUCTOR PACKAGE WITH PASSIVATION ISLAND FOR REDUCING STRESS ON SOLDER BUMPS
102	SC-P09-124	8,138,014	12/698,923	METHOD OF FORMING THIN PROFILE WLCSP WITH VERTICAL INTERCONNECT OVER PACKAGE FOOTPRINT
103	SC-P09-085	8,574,960	12/699,482	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CAVITY ADJACENT TO SENSITIVE REGION OF SEMICONDUCTOR DIE USING WAFER-LEVEL UNDERFILL MATERIAL
104	SC-P08-148	8,304,904	12/700,114	SEMICONDUCTOR DEVICE WITH SOLDER BUMP FORMED ON HIGH TOPOGRAPHY PLATED CU PADS
105	SC-P08-187	8,111,112	12/705,790	SEMICONDUCTOR DEVICE AND METHOD OF FORMING COMPACT COILS FOR HIGH PERFORMANCE FILTER
106	SC-P08-187	8,111,113	12/705,810	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THIN FILM CAPACITOR
107	SC-P09-227	8,822,281	12/710,995	SEMICONDUCTOR DEVICE AND METHOD OF FORMING TMV AND TSV IN WLCSP USING SAME CARRIER
108	SC-P08-432	9,922,955	12/717,335	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PACKAGE-ON-PACKAGE STRUCTURE ELECTRICALLY INTERCONNECTED THROUGH TSV IN WLCSP
109	SC-P09-149 & SC-P09-180	8,241,956	12/719,476	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WAFER LEVEL MULTI-ROW ETCHED LEAD PACKAGE
110	SC-P09-120	8,951,839	12/724,354	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE VIAS THROUGH INTERCONNECT STRUCTURES AND ENCAPSULANT OF WLCSP
111	SC-P08-383	8,343,809	12/724,367	SEMICONDUCTOR DEVICE AND METHOD OF FORMING REPASSIVATION LAYER WITH REDUCED OPENING TO CONTACT PAD OF SEMICONDUCTOR DIE
112	SC-P09-091	8,791,006	12/728,860	SEMICONDUCTOR DEVICE AND METHOD OF FORMING AN INDUCTOR ON POLYMER MATRIX COMPOSITE SUBSTRATE
113	SC-P10-002	8,791,775	12/750,517	SEMICONDUCTOR DEVICE AND METHOD OF FORMING HIGH-ATTENUATION BALANCED BAND-PASS FILTER
114	SC-P10-005	8,259,575	12/750,555	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RF BALUN HAVING REDUCED CAPACITIVE COUPLING AND HIGH CMRR
115	SC-P08-006	8,486,557	12/756,067	SOLDER BUMP CONFINEMENT SYSTEM FOR AN INTEGRATED CIRCUIT PACKAGE
116	SC-P07-043	9,847,253	12/757,750	PACKAGE-ON-PACKAGE USING THROUGH-HOLE VIA DIE ON SAW STREETS
117	SC-P06-151	8,120,183	12/763,386	METHOD OF FORMING TOP ELECTRODE FOR CAPACITOR AND INTERCONNECTION IN INTEGRATED PASSIVE DEVICE (IPD)
118	SC-P09-085	9,508,626	12/766,807	SEMICONDUCTOR DEVICE AND METHOD OF FORMING OPENINGS IN THERMALLY-CONDUCTIVE FRAME OF FO-WLCSP TO DISSIPATE HEAT AND REDUCE PACKAGE HEIGHT
119	SC-P08-172	9,029,193	12/775,170	SEMICONDUCTOR DEVICE AND METHOD OF FORMING AN INTERCONNECT STRUCTURE FOR 3-D DEVICES USING ENCAPSULANT FOR STRUCTURAL SUPPORT
120	SC-P08-172	8,049,328	12/775,188	SEMICONDUCTOR DEVICE AND METHOD OF FORMING AN INTERCONNECT STRUCTURE FOR 3-D DEVICES USING ENCAPSULANT FOR STRUCTURAL SUPPORT

121	SC-P09-114 & SC-P09-179	8,241,964	12/778,761	SEMICONDUCTOR DEVICE AND METHOD OF EMBEDDING BUMPS FORMED ON SEMICONDUCTOR DIE INTO PENETRABLE ADHESIVE LAYER TO REDUCE DIE SHIFTING DURING ENCAPSULATION
122	SC-P09-108	8,558,392	12/780,268	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT STRUCTURE AND MOUNTING SEMICONDUCTOR DIE IN RECESSED ENCAPSULANT
123	SC-P09-087	8,258,012	12/780,295	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DISCONTINUGESD PROTECTION LAYERS BETWEEN SEMICONDUCTOR DIE
124	SC-P09-083	8,357,564	12/781,751	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PREFABRICATED MULTI-DIE LEADFRAME FOR ELECTRICAL INTERCONNECT OF STACKED SEMICONDUCTOR DIE
125	SC-P08-438	8,455,300	12/787,216	INTEGRATED CIRCUIT PACKAGE SYSTEM WITH EMBEDDED DIE SUPERSTRUCTURE AND METHOD OF MANUFACTURE THEREOF
126	SC-P09-195	8,349,658	12/787,973	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE POSTS AND HEAT SINK OVER SEMICONDUCTOR DIE USING LEADFRAME
127	SC-P07-044	8,062,929	12/788,785	SEMICONDUCTOR DEVICE AND METHOD OF STACKING SAME SIZE SEMICONDUCTOR DIE ELECTRICALLY CONNECTED THROUGH CONDUCTIVE VIA FORMED AROUND PERIPHERY OF THE DIE
128	SC-P09-231	9,484,279	12/792,031	SEMICONDUCTOR DEVICE AND METHOD OF FORMING EMI SHIELDING LAYER WITH CONDUCTIVE MATERIAL AROUND SEMICONDUCTOR DIE
129	SC-P09-137	8,105,872	12/792,066	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PREFABRICATED EMI SHIELDING FRAME WITH CAVITIES CONTAINING PENETRABLE MATERIAL OVER SEMICONDUCTOR DIE
130	SC-P09-214	9,318,441	12/794,596	SEMICONDUCTOR DEVICE AND METHOD OF FORMING SACRIFICIAL ADHESIVE OVER CONTACT PADS OF SEMICONDUCTOR DIE
131	SC-P08-378	8,183,130	12/816,190	SEMICONDUCTOR DEVICE AND METHOD OF FORMING SHIELDING LAYER AROUND BACK SURFACE AND SIDES OF SEMICONDUCTOR WAFER CONTAINING IPD STRUCTURE
132	SC-P09-275	8,349,648	12/816,225	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RF FEM WITH LC FILTER AND IPD FILTER OVER SUBSTRATE
133	SC-P09-175	8,202,797	12/820,491	INTEGRATED CIRCUIT SYSTEM WITH RECESSED THROUGH SILICON VIA PADS AND METHOD OF MANUFACTURE THEREOF
134	SC-P09-217	9,320,455	12/822,458	SEMICONDUCTOR DEVICE AND METHOD OF FORMING ANISOTROPIC CONDUCTIVE FILM BETWEEN SEMICONDUCTOR DIE AND BUILD-UP INTERCONNECT STRUCTURE
135	SC-P09-178	8,796,137	12/822,488	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RDL ALONG SLOPED SIDE SURFACE OF SEMICONDUCTOR DIE FOR Z-DIRECTION INTERCONNECT
136	SC-P07-089	8,309,452	12/826,356	METHOD OF FORMING AN INDUCTOR ON A SEMICONDUCTOR WAFER
137	SC-P08-107	8,558,277	12/831,047	SEMICONDUCTOR DEVICE AND METHOD OF PROVIDING ELECTROSTATIC DISCHARGE PROTECTION FOR INTEGRATED PASSIVE DEVICES
138	SC-P09-176	8,895,440	12/852,433	SEMICONDUCTOR DIE AND METHOD OF FORMING FO-WLCSP VERTICAL INTERCONNECT USING TSV AND TMV
139	SC-P09-028	8,318,541	12/853,865	SEMICONDUCTOR DEVICE AND METHOD OF FORMING VERTICAL INTERCONNECT IN FO-WLCSP USING LEADFRAME DISPOSED BETWEEN SEMICONDUCTOR DIE
140	SC-P09-233	8,193,610	12/853,885	SEMICONDUCTOR DEVICE AND METHOD OF FORMING B-STAGE CONOUCTIVE POLYMER OVER CONTACT PADS OF SEMICONDUCTOR DIE IN FO-WLCSP
141	SC-P09-051	8,343,810	12/857,362	SEMICONDUCTOR DEVICE AND METHOD OF FORMING FO-WLCSP HAVING CONDUCTIVE LAYERS AND CONDUCTIVE VIAS SEPARATED BY POLYMER LAYERS
142	SC-P07-161	8,592,252	12/858,593	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THROUGH HOLE VIAS IN DIE EXTENSION REGION AROUND PERIPHERY OF DIE
143	SC-P07-161	8,399,991	12/858,602	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THROUGH HOLE VIAS IN DIE EXTENSION REGION AROUND PERIPHERY OF DIE
144	SC-P07-161	8,252,666	12/858,615	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THROUGH HOLE VIAS IN DIE EXTENSION REGION AROUND PERIPHERY OF DIE
145	SC-P09-213	8,288,201	12/868,334	SEMICONDUCTOR DEVICE AND METHOD OF FORMING FO-WLCSP WITH DISCRETE SEMICONDUCTOR COMPONENTS MOUNTED UNDER AND OVER SEMICONDUCTOR DIE
146	SC-P09-327	8,097,490	12/870,596	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STEPPED INTERCONNECT LAYER FOR STACKED SEMICONDUCTOR DIE
147	SC-P08-069	8,496,439	12/871,401	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SHIELDING LAYER OVER A SEMICONDUCTOR DIE AFTER FORMING A BUILD-UP INTERCONNECT STRUCTURE
148	SC-P09-225	8,518,749	12/874,787	SEMICONDUCTOR DEVICE AND METHOD OF FORMING TSV SEMICONDUCTOR WAFER WITH EMBEDDED SEMICONDUCTOR DIE
149	SC-P09-228	8,383,457	12/875,981	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERPOSER FRAME OVER SEMICONDUCTOR DIE TO PROVIDE VERTICAL INTERCONNECT
150	SC-P09-229	8,354,297	12/876,013	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DIFFERENT HEIGHT CONDUCTIVE PILLARS TO ELECTRICALLY INTERCONNECT STACKED LATERALLY OFFSET SEMICONDUCTOR DIE
151	SC-P10-003	8,080,445	12/878,425	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WLP WITH SEMICONDUCTOR DIE EMBEDDED WITHIN PENETRABLE ENCAPSULANT BETWEEN TSV INTERPOSERS
152	SC-P09-281	8,435,834	12/880,255	SEMICONDUCTOR DEVICE AND METHOD OF FORMING BOND-ON-LEAD INTERCONNECTION FOR MOUNTING SEMICONDUCTOR DIE IN FO-WLCSP
153	SC-P10-014	8,409,922	12/882,110	SEMICONDUCTOR DEVICE AND METHOD OF FORMING LEADFRAME INTERPOSER OVER SEMICONDUCTOR DIE AND TSV SUBSTRATE FOR VERTICAL ELECTRICAL INTERCONNECT
154	SC-P09-208	8,421,212	12/887,681	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH ACTIVE SURFACE HEAT REMOVAL AND METHOD OF MANUFACTURE THEREOF
155	SC-P07-115	8,247,268	12/896,430	SEMICONDUCTOR WAFER HAVING THROUGH-HOLE VIAS ON SAW STREETS WITH BACKSIDE REDISTRIBUTION LAYER
156	SC-P07-236	8,097,943	12/905,787	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WAFER LEVEL GROUND PLANE AND POWER RING
157	SC-P08-171	8,263,439	12/905,823	SEMICONDUCTOR DEVICE AND METHOD OF FORMING AN INTERPOSER PACKAGE WITH THROUGH SILICON VIAS
158	SC-P09-181	9,337,116	12/914,378	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STEPPED INTERPOSER FOR STACKING AND ELECTRICALLY CONNECTING SEMICONDUCTOR DIE
159	SC-P09-315	8,283,435	12/914,895	SEMICONDUCTOR DEVICE AND METHOD OF STACKING SEMICONDUCTOR DIE IN MOLD LASER PACKAGE INTERCONNECTED BY BUMPS AND CONDUCTIVE VIAS

160	SC-P10-008	8,546,193	12/917,629	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PENETRABLE ENCAPSULANT AROUND SEMICONDUCTOR DIE AND INTERCONNECT STRUCTURE
161	SC-P07-160	8,866,248	12/941,683	SEMICONDUCTOR DEVICE WITH OPTICAL SENSOR AND METHOD OF FORMING INTERCONNECT STRUCTURE ON FRONT AND BACKSIDE OF THE DEVICE
162	SC-P10-110	9,171,769	12/981,260	SEMICONDUCTOR DEVICE AND METHOD OF FORMING OPENINGS THROUGH ENCAPSULANT TO REDUCE WARPAGE AND STRESS ON SEMICONDUCTOR PACKAGE
163	SC-P08-449	8,994,048	12/964,117	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RECESSES IN SUBSTRATE FOR SAME SIZE OR DIFFERENT SIZED DIE WITH VERTICAL INTEGRATION
164	SC-P07-257	8,125,073	13/004,111	WAFER INTEGRATED WITH PERMANENT CARRIER AND METHOD THEREFOR
165	SC-P07-114	8,815,643	13/021,858	METHOD OF FABRICATING SEMICONDUCTOR DIE WITH THROUGH-HOLE VIA ON SAW STREETS AND THROUGH-HOLE VIA IN ACTIVE AREA OF DIE
166	SC-P08-185	8,957,530	13/023,283	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH EMBEDDED CIRCUITRY AND POST
167	SC-P09-250	8,273,604	13/032,538	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WLCSP STRUCTURE USING PROTRUDED MLP
168	SC-P08-336	8,525,344	13/034,075	SEMICONDUCTOR DEVICE AND METHOD OF FORMING BOND WIRES BETWEEN SEMICONDUCTOR DIE CONTACT PADS AND CONDUCTIVE TOV IN PERIPHERAL AREA AROUND SEMICONDUCTOR DIE
169	SC-P09-261	8,623,702	13/034,133	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE THV AND RDL ON OPPOSITE SIDES OF SEMICONDUCTOR DIE FOR RDL-TO-RDL BONDING
170	SC-P10-137	8,466,544	13/035,669	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERPOSER AND OPPOSING BUILD-UP INTERCONNECT STRUCTURE WITH CONNECTING CONDUCTIVE TMV FOR ELECTRICAL INTERCONNECT OF FO-WLCSP
171	SC-P10-092	8,835,301	13/037,191	SEMICONDUCTOR DEVICE AND METHOD OF FORMING BUMP STRUCTURE WITH INSULATING BUFFER LAYER TO REDUCE STRESS ON SEMICONDUCTOR WAFER
172	SC-P10-032	8,268,677	13/043,179	SEMICONDUCTOR DEVICE AND METHOD OF FORMING SHIELDING LAYER OVER SEMICONDUCTOR DIE MOUNTED TO TSV INTERPOSER
173	SC-P08-175	9,184,103	13/048,771	SEMICONDUCTOR DEVICE HAVING EMBEDDED INTEGRATED PASSIVE DEVICES ELECTRICALLY INTERCONNECTED USING CONDUCTIVE PILLARS
174	SC-P08-353	9,030,002	13/090,590	SEMICONDUCTOR DEVICE HAVING IPD STRUCTURE WITH SMOOTH CONDUCTIVE LAYER AND BOTTOM-SIDE CONDUCTIVE LAYER
175	SC-P07-348	8,502,376	13/101,657	WIREBONDLESS WAFER LEVEL PACKAGE WITH PLATED BUMPS AND INTERCONNECTS
176	SC-P10-283	8,389,333	13/116,328	SEMICONDUCTOR DEVICE AND METHOD OF FORMING EWLB PACKAGE CONTAINING STACKED SEMICONDUCTOR DIE ELECTRICALLY CONNECTED THROUGH CONDUCTIVE VIAS FORMED IN ENCAPSULANT AROUND DIE
177	SC-P10-234	9,252,172	13/149,628	SEMICONDUCTOR DEVICE AND METHOD OF FORMING EWLB SEMICONDUCTOR PACKAGE WITH VERTICAL INTERCONNECT STRUCTURE AND CAVITY REGION
178	SC-P10-272	8,288,209	13/153,266	SEMICONDUCTOR DEVICE AND METHOD OF USING LEADFRAME BODIES TO FORM OPENINGS THROUGH ENCAPSULANT FOR VERTICAL INTERCONNECT OF SEMICONDUCTOR DIE
179	SC-P10-239	8,687,130	13/167,487	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT STRUCTURE OVER SEED LAYER ON CONTACT PAD OF SEMICONDUCTOR DIE WITHOUT UNDERCUTTING SEED LAYER BENEATH INTERCONNECT STRUCTURE
180	SC-P10-276	9,324,673	13/167,649	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH WAFER LEVEL RECONFIGURATION AND METHOD OF MANUFACTURE THEREOF
181	SC-P10-126	9,202,713	13/181,412	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RDL OVER CONTACT PAD WITH HIGH ALIGNMENT TOLERANCE OR REDUCED INTERCONNECT PITCH
182	SC-P09-052	9,048,209	13/190,339	SEMICONDUCTOR DEVICE AND METHOD OF MOUNTING SEMICONDUCTOR DIE TO HEAT SPREADER ON TEMPORARY CARRIER AND FORMING POLYMER LAYER AND CONDUCTIVE LAYER OVER THE DIE
183	SC-P08-290	8,390,391	13/219,374	SEMICONDUCTOR DEVICE AND METHOD OF INTEGRATING BALUN AND RF COUPLER ON A COMMON SUBSTRATE
184	SC-P09-121	8,912,648	13/231,789	SEMICONDUCTOR DEVICE AND METHOD OF FORMING COMPLIANT STRESS RELIEF BUFFER AROUND LARGE ARRAY WLCSP
185	SC-P08-129	8,359,396	13/233,403	METHOD FOR MANUFACTURE OF INTEGRATED CIRCUIT PACKAGE SYSTEM WITH PROTECTED CONDUCTIVE LAYERS FOR PADS
186	SC-P10-277	9,177,832	13/234,535	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A RECONFIGURED STACKABLE WAFER LEVEL PACKAGE WITH VERTICAL INTERCONNECT
187	SC-P07-147	8,921,983	13/235,413	SEMICONDUCTOR PACKAGE AND METHOD OF FORMING SIMILAR STRUCTURE FOR TOP AND BOTTOM BONDING PADS
188	SC-P07-098	8,304,339	13/237,828	SOLDER BUMP WITH INNER CORE PILLAR IN SEMICONDUCTOR PACKAGE
189	SC-P10-114	9,679,863	13/243,214	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT SUBSTRATE FOR FO-WLCSP
190	SC-P11-091	9,385,009	13/243,558	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STACKED VIAS WITHIN INTERCONNECT STRUCTURE FOR FO-WLCSP
191	SC-P07-344	8,940,636	13/273,537	THROUGH HOLE VIAS AT SAW STREETS INCLUDING PROTRUSIONS OR RECESSES FOR INTERCONNECTION
192	SC-P10-003	9,054,095	13/254,003	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WLP WITH SEMICONDUCTOR DIE EMBEDDED WITHIN PENETRABLE ENCAPSULANT BETWEEN TSV INTERPOSERS
193	SC-P11-213	8,513,098	13/285,843	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RECONSTITUTED WAFER WITH LARGER CARRIER TO ACHIEVE MORE EWLB PACKAGES PER WAFER WITH ENCAPSULANT DEPOSITED UNDER TEMPERATURE AND PRESSURE
194	SC-P11-107	9,142,522	13/307,849	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RDL UNDER BUMP FOR ELECTRICAL CONNECTION TO ENCLOSED BUMP
195	SC-P10-288	8,624,353	13/311,266	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTEGRATED PASSIVE DEVICE OVER SEMICONDUCTOR DIE WITH CONDUCTIVE BRIDGE AND FAN-OUT REDISTRIBUTION LAYER

196	SC-P11-103	8,963,326	13/312,730	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PATTERNED REPASSIVATION OPENINGS BETWEEN RDL AND UBM TO REDUCE ADVERSE EFFECTS OF ELECTRO-MIGRATION
197	SC-P10-233	8,810,286	13/315,010	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THICK ENCAPSULANT FOR STIFFNESS WITH RECESSES FOR STRESS RELIEF IN FO-WLCSP
198	SC-P11-163	8,558,389	13/315,033	SEMICONDUCTOR DEVICE AND METHOD OF FORMING GUARD RING AROUND CONDUCTIVE TSV THROUGH SEMICONDUCTOR WAFER
199	SC-P11-109	8,809,191	13/324,446	SEMICONDUCTOR DEVICE AND METHOD OF FORMING UBM STRUCTURE ON BACK SURFACE OF TSV SEMICONDUCTOR WAFER
200	SC-P11-139	8,710,670	13/328,118	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH COUPLING FEATURES AND METHOD OF MANUFACTURE THEREOF
201	SC-P11-145	8,592,992	13/326,128	SEMICONDUCTOR DEVICE AND METHOD OF FORMING VERTICAL INTERCONNECT STRUCTURE WITH CONDUCTIVE MICRO VIA ARRAY FOR 3-D FO-WLCSP
202	SC-P10-232	8,648,470	13/326,167	SEMICONDUCTOR DEVICE AND METHOD OF FORMING FO-WLCSP WITH MULTIPLE ENCAPSULANTS
203	SC-P11-111	8,742,591	13/333,395	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INSULATING LAYER IN NOTCHES AROUND CONDUCTIVE TSV FOR STRESS RELIEF
204	SC-P11-024 & SC-P11-037	8,456,002	13/333,739	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INSULATING LAYER DISPOSED OVER THE SEMICONDUCTOR DIE FOR STRESS RELIEF
205	SC-P07-292	8,546,195	13/335,631	SEMICONDUCTOR PACKAGE HAVING SEMICONDUCTOR DIE WITH INTERNAL VERTICAL INTERCONNECT STRUCTURE AND METHOD THEREFOR
206	SC-P07-292	8,723,305	13/335,887	SEMICONDUCTOR PACKAGE HAVING SEMICONDUCTOR DIE WITH INTERNAL VERTICAL INTERCONNECT STRUCTURE AND METHOD THEREFOR
207	SC-P07-236	9,390,981	13/346,415	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WAFER LEVEL GROUND PLANE AND POWER RING
208	SC-P09-327	8,946,870	13/349,510	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STEPPED INTERCONNECT LAYER FOR STACKED SEMICONDUCTOR DIE
209	SC-P09-137	8,581,370	13/349,828	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PREFABRICATED EMI SHIELDING FRAME WITH CAVITIES CONTAINING PENETRABLE MATERIAL OVER SEMICONDUCTOR DIE
210	SC-P09-137	8,492,196	13/349,919	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PREFABRICATED EMI SHIELDING FRAME WITH CAVITIES CONTAINING PENETRABLE MATERIAL OVER SEMICONDUCTOR DIE
211	SC-P09-327	8,283,205	13/350,299	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STEPPED INTERCONNECT LAYER FOR STACKED SEMICONDUCTOR DIE
212	SC-P06-161	8,399,990	13/355,354	METHOD OF FORMING TOP ELECTRODE FOR CAPACITOR AND INTERCONNECTION IN INTEGRATED PASSIVE DEVICE (IPD)
213	SC-P11-213	8,524,577	13/368,008	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RECONSTITUTED WAFER WITH LARGER CARRIER TO ACHIEVE MORE EWLB PACKAGES PER WAFER WITH ENCAPSULANT DEPOSITED UNDER TEMPERATURE AND PRESSURE
214	SC-P09-124	9,269,595	13/403,859	SEMICONDUCTOR DEVICE WITH THIN PROFILE WLCSP WITH THIN PROFILE WLCSP WITH VERTICAL INTERCONNECT OVER PACKAGE FOOTPRINT
215	SC-P09-124	9,556,965	13/403,889	SEMICONDUCTOR DEVICE WITH THIN PROFILE WLCSP WITH VERTICAL INTERCONNECT OVER PACKAGE FOOTPRINT
216	SC-P09-093	9,048,306	13/420,400	SEMICONDUCTOR DEVICE AND METHOD OF FORMING OPEN CAVITY IN TSV INTERPOSER TO CONTAIN SEMICONDUCTOR DIE IN WLCSMP
217	SC-P09-081	9,685,495	13/423,265	SEMICONDUCTOR DEVICE AND METHOD OF FORMING IPD ON MOLDED SUBSTRATE
218	SC-P08-423	9,524,955	13/423,782	SEMICONDUCTOR DEVICE AND METHOD OF FORMING NO-FLOW UNDERFILL MATERIAL AROUND VERTICAL INTERCONNECT STRUCTURE
219	SC-P11-246	8,901,755	13/425,349	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE LAYER OVER METAL SUBSTRATE FOR ELECTRICAL INTERCONNECT OF SEMICONDUCTOR DIE
220	SC-P11-115	8,900,929	13/426,561	SEMICONDUCTOR DEVICE AND METHOD FOR FORMING OPENINGS AND TRENCHES IN INSULATING LAYER BY FIRST LDA AND SECOND LDA FOR RDL FORMATION
221	SC-P11-219	9,082,780	13/428,439	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A ROBUST FAN-OUT PACKAGE INCLUDING VERTICAL INTERCONNECTS AND MECHANICAL SUPPORT LAYER
222	SC-P08-376	8,896,115	13/435,463	SEMICONDUCTOR DEVICE AND METHOD OF FORMING SHIELDING LAYER AROUND BACK SURFACE AND SIDES OF SEMICONDUCTOR WAFER CONTANING IPD STRUCTURE
223	SC-P09-233	9,415,941	13/438,713	SEMICONDUCTOR DEVICE AND METHOD OF FORMING B-STAGE CONDUCTIVE POLYMER OVER CONTACT PADS OF SEMICONDUCTOR DIE IN FO-WLCSP
224	SC-P06-116	8,558,399	13/443,067	DUAL MOLDED MULTI-CHIP PACKAGE SYSTEM
225	SC-P05-073	8,951,904	13/458,145	INTEGRATED CIRCUIT PACKAGE SYSTEM WITH POST-PASSIVATION INTERCONNECTION AND INTEGRATION
226	SC-P11-113	9,559,004	13/469,754	SEMICONDUCTOR DEVICE AND METHOD OF SINGULATING THIN SEMICONDUCTOR WAFER ON CARRIER ALONG MODIFIED REGION WITHIN NON-ACTIVE REGION FORMED BY IRRADIATING ENERGY
227	SC-P08-439	8,575,769	13/492,869	SEMICONDUCTOR DEVICE AND METHOD OF EMBEDDING THERMALLY CONDUCTIVE LAYER IN INTERCONNECT STRUCTURE FOR HEAT DISSIPATION
228	SC-P12-009	9,385,006	13/529,918	SEMICONDUCTOR DEVICE AND METHOD OF FORMING AN EMBEDDED SOP FAN-OUT PACKAGE
229	SC-P09-114 & SC-P09-179	8,856,294	13/536,177	SEMICONDUCTOR DEVICE AND METHOD OF EMBEDDING BUMPS FORMED ON SEMICONDUCTOR DIE INTO PENETRABLE ADHESIVE LAYER TO REDUCE DIE SHIFTING DURING ENCAPSULATION
230	SC-P07-115	8,177,848	13/543,618	SEMICONDUCTOR WAFER HAVING THROUGH-HOLE VIAS ON SAW STREETS WITH BACKSIDE REDISTRIBUITION LAYER
231	SC-P07-180	9,525,080	13/555,353	SEMICONDUCTOR DEVICE WITH OPTICAL SENSOR AND METHOD OF FORMING INTERCONNECT STRUCTURE ON FRONT AND BACKSIDE OF THE DEVICE
232	SC-P09-087	8,710,635	13/560,908	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DISCONTINUOESD PROTECTION LAYERS BETWEEN SEMICONDUCTOR DIE
233	SC-P09-315	9,252,032	13/566,872	SEMICONDUCTOR DEVICE AND METHOD OF STACKING SEMICONDUCTOR DIE IN MOLD LASER PACKAGE INTERCONNECTED BY BUMPS AND CONDUCTIVE VIAS

234	SC-P09-250	8,519,544	13/570,979	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WLCSP STRUCTURE USING PROTRUDED MLP
235	SC-P10-032	8,810,011	13/571,029	SEMICONDUCTOR DEVICE AND METHOD OF FORMING SHIELDING LAYER OVER SEMICONDUCTOR DIE MOUNTED TO TSV INTERPOSER
236	SC-P10-005	8,981,866	13/571,066	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RF BALUN HAVING REDUCED CAPACITIVE COUPLING AND HIGH CMRR
237	SC-P07-268	9,082,638	13/572,517	SEMICONDUCTOR DEVICE WITH CROSS-TALK ISOLATION USING M-CAP
238	SC-P08-213	9,283,301	13/607,294	SEMICONDUCTOR DEVICE AND METHOD OF FORMING FO-WLCSP WITH DISCRETE SEMICONDUCTOR COMPONENTS MOUNTED UNDER AND OVER SEMICONDUCTOR DIE
239	SC-P06-148	9,240,384	13/621,804	SEMICONDUCTOR DEVICE WITH SOLDER BUMP FORMED ON HIGH TOPOGRAPHY PLATED CU PADS
240	SC-P07-098	9,177,930	13/621,810	SOLDER BUMP WITH INNER CORE PILLAR IN SEMICONDUCTOR PACKAGE
241	SC-P07-089	9,337,141	13/622,260	METHOD OF FORMING AN INDUCTOR ON A SEMICONDUCTOR WAFER
242	SC-P09-028	8,842,808	13/645,385	SEMICONDUCTOR DEVICE AND METHOD OF FORMING VERTICAL INTERCONNECT IN FO-WLCSP USING LEADFRAME DISPOSED BETWEEN SEMICONDUCTOR DIE
243	SC-P12-080	9,331,007	13/653,242	SEMICONDUCTOR DEVICE AND METHOD FORMING CONDUCTIVE INK LAYER AS INTERCONNECT STRUCTURE BETWEEN SEMICONDUCTOR PACKAGES
244	SC-P08-383	8,785,100	13/664,628	SEMICONDUCTOR DEVICE AND METHOD OF FORMING REPASSIVATION LAYER WITH REDUCED OPENING TO CONTACT PAD OF SEMICONDUCTOR DIE
245	SC-P09-275	9,704,857	13/678,134	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RF FEM WITH LC FILTER AND IPD FILTER OVER SUBSTRATE
246	SC-P09-051	8,836,114	13/679,792	SEMICONDUCTOR DEVICE AND METHOD OF FORMING FO-WLCSP HAVING CONDUCTIVE LAYERS AND CONDUCTIVE VIAS SEPARATED BY POLYMER LAYERS
247	SC-P08-199	9,099,455	13/683,884	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE POSTS EMBEDDED IN PHOTOSENSITIVE ENCAPSULANT
248	SC-P09-195	9,064,859	13/683,948	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE POSTS AND HEAT SINK OVER SEMICONDUCTOR DIE USING LEADFRAME
249	SC-P09-229	8,896,109	13/684,055	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DIFFERENT HEIGHT CONDUCTIVE PILLARS TO ELECTRICALLY INTERCONNECT STACKED LATERALLY OFFSET SEMICONDUCTOR DIE
250	SC-P08-460	8,907,498	13/691,440	SEMICONDUCTOR DEVICE AND METHOD AND METHOD OF FORMING A SHIELDING LAYER BETWEEN STACKED SEMICONDUCTOR DIE
251	SC-P09-083	9,153,476	13/691,464	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PREFABRICATED MULTI-DIE LEADFRAME FOR ELECTRICAL INTERCONNECT OF STACKED SEMICONDUCTOR DIE
252	SC-P09-228	9,240,380	13/715,424	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERPOSER FRAME OVER SEMICONDUCTOR DIE TO PROVIDE VERTICAL INTERCONNECT
253	SC-P09-022	9,484,334	13/716,799	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DIRECTIONAL RF COUPLER WITH IPD FOR ADDITIONAL RF SIGNAL PROCESSING
254	SC-P10-263	8,921,161	13/732,159	SEMICONDUCTOR DEVICE AND METHOD OF FORMING EWLB PACKAGE CONTAINING STACKED SEMICONDUCTOR DIE ELECTRICALLY CONNECTED THROUGH CONDUCTIVE VIAS FORMED IN ENCAPSULANT AROUND DIE
255	SC-P12-091	9,076,655	13/743,054	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THROUGH-SILICON-VIA WITH SACRIFICIAL LAYER
256	SC-P12-032	9,318,404	13/759,911	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STRESS RELIEVING VIAS FOR IMPROVED FAN-OUT WLCSP PACKAGE
257	SC-P06-161	8,703,548	13/765,478	METHOD OF FORMING TOP ELECTRODE FOR CAPACITOR AND INTERCONNECTION IN INTEGRATED PASSIVE DEVICE (IPD)
258	SC-P10-014	8,866,275	13/766,646	SEMICONDUCTOR DEVICE AND METHOD OF FORMING LEADFRAME INTERPOSER OVER SEMICONDUCTOR DIE AND TSV SUBSTRATE FOR VERTICAL ELECTRICAL INTERCONNECT
259	SC-P12-029	9,293,401	13/772,683	SEMICONDUCTOR DEVICE AND METHOD FOR FORMING WAFER LEVEL BALL GRID ARRAY MOLDED LASER PACKAGE (EWLB-LMP)
260	SC-P11-024 & SC-P11-037	8,759,155	13/782,618	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INSULATING LAYER DISPOSED OVER THE SEMICONDUCTOR DIE FOR STRESS RELIEF
261	SC-P07-220	9,449,925	13/782,939	INTEGRATED PASSIVE DEVICES
262	SC-P12-064	9,305,854	13/785,879	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RDL USING UV-CURED CONDUCTIVE INK OVER WAFER LEVEL PACKAGE
263	SC-P12-101	9,559,039	13/800,807	SEMICONDUCTOR DEVICE AND METHOD OF USING SUBSTRATE HAVING BASE AND CONDUCTIVE POSTS TO FORM VERTICAL INTERCONNECT STRUCTURE IN EMBEDDED DIE PACKAGE
264	SC-P12-058	9,799,590	13/801,675	SEMICONDUCTOR DEVICE AND METHOD OF USING PARTIAL WAFER SINGULATION FOR IMPROVED WAFER LEVEL EMBEDDED SYSTEM IN PACKAGE
265	SC-P12-102	9,443,797	13/832,761	SEMICONDUCTOR DEVICE HAVING WIRE STUDS AS VERTICAL INTERCONNECT IN FO-WLP
266	SC-P12-046	9,059,157	13/842,562	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH SUBSTRATE AND METHOD OF MANUFACTURE THEREOF
267	SC-P08-422	9,123,733	13/844,160	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH PACKAGE UNDERFILL AND METHOD OF MANUFACTURE THEREOF
268	SC-P08-069	9,790,962	13/846,329	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SHIELDING LAYER OVER A SEMICONDUCTOR DIE AFTER FORMING A BUILD-UP INTERCONNECT STRUCTURE
269	SC-P07-042	9,524,938	13/846,409	PACKAGE-IN-PACKAGE USING THROUGH HOLE VIA DIE ON SAW STREETS
270	SC-P09-291	9,679,824	13/845,542	SEMICONDUCTOR DEVICE AND METHOD OF FORMING BOND-ON-LEAD INTERCONNECTION FOR MOUNTING SEMICONDUCTOR DIE IN FO-WLCSP
271	SC-P10-137	8,994,184	13/887,180	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERPOSER AND OPPOSING BUILD-UP INTERCONNECT STRUCTURE WITH CONNECTING CONDUCTIVE TMV FOR ELECTRICAL INTERCONNECT OF FO-WLCSP

272	SC-P12-133	9,269,691	13/918,103	SEMICONDUCTOR DEVICE AND METHOD OF MAKING AN EMBEDDED WAFER LEVEL BALL GRID ARRAY (EWLB) PACKAGE ON PACKAGE (POP) DEVICE WITH A SLOTTED METAL CARRIER INTERPOSER
273	SC-P08-259	9,443,762	13/933,406	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A THIN WAFER WITHOUT A CARRIER
274	SC-P09-108	8,823,182	13/935,965	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT STRUCTURE AND MOUNTING SEMICONDUCTOR DIE IN RECESSED ENCAPSULANT
275	SC-P09-228	9,754,858	13/936,099	SEMICONDUCTOR DEVICE AND METHOD OF FORMING TSV SEMICONDUCTOR WAFER WITH EMBEDDED SEMICONDUCTOR DIE
276	SC-P10-008	9,431,331	13/937,849	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PENETRABLE FILM ENCAPSULANT AROUND SEMICONDUCTOR DIE AND INTERCONNECT STRUCTURE
277	SC-P11-163	9,257,382	13/939,044	SEMICONDUCTOR DEVICE AND METHOD OF FORMING GUARD RING AROUND CONDUCTIVE TSV THROUGH SEMICONDUCTOR WAFER
278	SC-P09-176	9,153,494	13/943,735	SEMICONDUCTOR DIE & METHOD OF FORMING FO-WLCSP VERTICAL INTERCONNECT USING TSV AND TMV
279	SC-P09-093	9,263,332	13/943,737	SEMICONDUCTOR DEVICE AND METHOD OF FORMING OPEN CAVITY IN TSV INTERPOSER TO CONTAIN SEMICONDUCTOR DIE IN WLCSP
280	SC-P12-055	9,252,092	13/950,122	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THROUGH MOLD HOLE WITH ALIGNMENT AND DIMENSION CONTROL
281	SC-P09-107	9,082,887	13/966,268	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH POSTS AND METHOD OF MANUFACTURE THEREOF
282	SC-P08-426	9,048,211	14/017,963	SEMICONDUCTOR DEVICE AND METHOD OF EMBEDDING THERMALLY CONDUCTIVE LAYER IN INTERCONNECT STRUCTURE FOR HEAT DISSAPATION
283	SC-P07-378 & SC-P08-043	8,975,980	14/018,282	SEMICONDUCTOR DEVICE HAVING BALANCED BAND-PASS FILTER IMPLEMENTED WITH LC RESONATORS
284	SC-P10-239	8,890,315	14/021,058	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT STRUCTURE OVER SEED LAYER ON CONTACT PAD OF SEMICONDUCTOR DIE WITHOUT UNDERCUTTING SEED LAYER BENEATH INTERCONNECT STRUCTURE
285	SC-P09-085	9,679,881	14/021,208	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CAVITY ADJACENT TO SENSITIVE REGION OF SEMICONDUCTOR DIE USING WAFER-LEVEL UNDERFILL MATERIAL
286	SC-P12-137	9,076,724	14/038,275	INTEGRATED CIRCUIT SYSTEM WITH DEBONDING ADHESIVE AND METHOD OF MANUFACTURE THEREOF
287	SC-P12-138	9,281,274	14/040,413	INTEGRATED CIRCUIT THROUGH-SUBSTRATE VIA SYSTEM WITH A BUFFER LAYER AND METHOD OF MANUFACTURE THEREOF
288	SC-P11-146	8,994,185	14/043,751	SEMICONDUCTIVE DEVICE AND METHOD OF FORMING VERTICAL INTERCONNECT STRUCTURE WITH CONDUCTIVE MICRO VIA ARRAY FOR 3-D FO-WLCSP
289	SC-P10-233	9,281,259	14/079,273	SEMICONDUCTOR DEVICE AND METHOD OF FORMING THICK ENCAPSULANT FOR STIFFNESS WITH RECESSES FOR STRESS RELIEF IN FO-WLCSP
290	SC-P10-232	9,142,428	14/080,608	SEMICONDUCTOR DEVICE AND METHOD OF FORMING FO-WLCSP WITH MULTIPLE ENCAPSULANTS
291	SC-P10-288	9,368,563	14/092,304	SEMICONDUCTOR DEVICE INCLUDING INTEGRATED PASSIVE DEVICE FORMED OVER SEMICONDUCTOR DIE WITH CONDUCTIVE BRIDGE AND FAN-OUT REDISTRIBUTION LAYER
292	SC-P13-085	9,154,139	14/109,313	SEMICONDUCTOR DEVICE AND METHOD OF REDUCING WARPAGE USING A SILICON TO ENCAPSULANT RATIO
293	SC-P13-094	9,728,415	14/134,907	SEMICONDUCTOR DEVICE AND METHOD OF WAFER THINNING INVOLVING EDGE TRIMMING AND CMP
294	SC-P13-070	9,768,038	14/139,312	SEMICONDUCTOR DEVICE AND METHOD OF MAKING EMBEDDED WAFER LEVEL CHIP SCALE PACKAGES
295	SC-P13-075	9,202,793	14/140,528	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH UNDER BUMP METALLIZATION AND METHOD OF MANUFACTURE THEREOF
296	SC-P13-031	9,627,338	14/187,014	SEMICONDUCTOR DEVICE AND METHOD OF FORMING ULTRA HIGH DENSITY EMBEDDED SEMICONDUCTOR DIE PACKAGE
297	SC-P09-087	9,153,544	14/194,591	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DISCONTINUOESD PROTECTION LAYERS BETWEEN SEMICONDUCTOR DIE
298	SC-P13-068	9,362,161	14/220,336	SEMICONDUCTOR DEVICE AND METHOD OF FORMING 3D DUAL SIDE DIE EMBEDDED BUILD-UP SEMICONDUCTOER PACKAGE
299	SC-P13-043	9,865,524	14/222,547	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE VIAS USING BACKSIDE VIA REVEAL AND SELECTIVE PASSIVATION
300	SC-P13-112	9,330,994	14/228,531	SEMICONDUCTOR DEVICE & METHOD OF FORMING RDL AND VERTICAL INTERCONNECT BY LASER DIRECT STRUCTURING
301	SC-P11-111	9,837,338	14/257,850	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INSULATING LAYER IN NOTCHES AROUND CONDUCTIVE TSV FOR STRESS RELIEF
302	SC-P13-071	9,478,485	14/261,252	SEMICONDUCTOR DEVICE AND METHOD FOR STACKED SEMICONDUCTOR DIE ON A FAN-OUT WLCSP
303	SC-P09-114 & SC-P09-179	9,257,411	14/265,752	SEMICONDUCTOR DEVICE AND METHOD OF EMBEDDING BUMPS FORMED ON SEMICONDUCTOR DIE INTO PENETRABLE ADHESIVE LAYER TO REDUCE DIE SHIFTING DURING ENCAPSULATION
304	SC-P08-287	9,401,331	14/267,800	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A VERTICAL INTERCONNECT STRUCTURE FOR 3-D FO-WLCSP
305	SC-P11-024 & SC-P11-037	9,087,930	14/274,599	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INSULATING LAYER DISPOSED OVER THE SEMICONDUCTOR DIE FOR STRESS RELIEF
306	SC-P08-383	9,472,452	14/284,752	SEMICONDUCTOR DEVICE AND METHOD OF FORMING REPASSIVATION LAYER WITH REDUCED OPENING TO CONTACT PAD OF SEMICONDUCTOR DIE
307	SC-P11-109	9,601,462	14/288,589	SEMICONDUCTOR DEVICE AND METHOD OF FORMING UBM STRUCTURE ON BACK SURFACE OF TSV SEMICONDUCTOR WAFER
308	SC-P13-095	9,184,104	14/288,843	SEMICONDUCTOR DEVICE AND METHOD OF FORMING ADHESIVE LAYER OVER INSULATING LAYER FOR BONDING CARRIER TO MIXED SURFACES OF SEMICONDUCTOR DIE AND ENCAPSULANT
309	SC-P09-091	9,548,347	14/289,344	SEMICONDUCTOR DEVICE AND METHOD OF FORMING AN INDUCTOR ON POLYMER MATRIX COMPOSITE SUBSTRATE
310	SC-P09-178	9,437,538	14/292,925	SEMICONDUCTOR DEVICE INCLUDING RDL ALONG SLOPED SIDE SURFACE OF SEMICONDUCTOR DIE FOR Z-DIRECTION INTERCONNECT

311	SC-P14-005	9,769,066	14/316,225	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE VIAS BY DIRECT VIA REVEAL WITH ORGANIC PASSIVATION
312	SC-P14-006	10,115,701	14/316,661	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE VIAS BY BACKSIDE VIA REVEAL WITH CMP
313	SC-P09-227	9,224,693	14/326,237	SEMICONDUCTOR DEVICE AND METHOD OF FORMING TMV AND TSV IN WLCSP USING SAME CARRIER
314	SC-P10-092	9,780,063	14/326,922	SEMICONDUCTOR DEVICE AND METHOD OF FORMING BUMP STRUCTURE WITH INSULATING BUFFER LAYER TO REDUCE STRESS ON SEMICONDUCTOR WAFER
315	SC-P10-032	9,685,403	14/331,060	SEMICONDUCTOR DEVICE AND METHOD OF FORMING SHIELDING LAYER OVER SEMICONDUCTOR DIE MOUNTED TO TSV INTERPOSER
316	SC-P09-113	9,418,878	14/340,187	SEMICONDUCTOR DEVICE AND METHOD OF FORMING ADHESIVE MATERIAL TO SECURE SEMICONDUCTOR DIE TO CARRIER IN WLCSP
317	SC-P11-249	9,673,093	14/449,914	SEMICONDUCTOR DEVICE AND METHOD OF MAKING WAFER LEVEL CHIP SCALE PACKAGE
318	SC-P09-108	9,530,739	14/462,347	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT STRUCTURE AND MOUNTING SEMICONDUCTOR DIE IN RECESSED ENCAPSULANT
319	SC-P10-239	9,105,532	14/503,698	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT STRUCTURE OVER SEED LAYER ON CONTACT PAD OF SEMICONDUCTOR DIE WITHOUT UNDERCUTTING SEED LAYER BENEATH INTERCONNECT STRUCTURE
320	SC-P11-115	9,607,959	14/512,614	SEMICONDUCTOR DEVICE AND METHOD FOR FORMING OPENINGS AND TRENCHES IN INSULATING LAYER BY FIRST LDA AND SECOND LDA FOR RDL FORMATION
321	SC-P13-125	9,472,533	14/549,064	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WIRE BONDABLE FAN-OUT EWLB PACKAGE
322	SC-P08-400	9,583,446	14/563,358	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A SHIELDING LAYER BETWEEN STACKED SEMICONDUCTOR DIE
323	SC-P11-103	9,397,058	14/563,448	SEMICONDUCTOR DEVICE AND METHOD OF FORMING PATTERNED REPASSIVATION OPENINGS BETWEEN RDL AND UBM TO REDUCE ADVERSE EFFECTS OF ELECTRO-MIGRATION
324	SC-P09-121	9,505,621	14/564,427	SEMICONDUCTOR DEVICE AND METHOD OF FORMING COMPLIANT STRESS RELIEF BUFFER AROUND LARGE ARRAY WLCSP
325	SC-P09-120	10,141,222	14/566,870	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE VIAS THROUGH INTERCONNECT STRUCTURES AND ENCAPSULANT OF WLCSP
326	SC-P09-327	9,824,975	14/612,075	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STEPPED INTERCONNECT LAYER FOR STACKED SEMICONDUCTOR DIE
327	SC-P14-156	9,704,769	14/627,347	SEMICONDUCTOR DEVICE AND METHOD OF FORMING ENCAPSULATED WAFER LEVEL CHIP SCALE PACKAGE (EWLCSP)
328	SC-P08-426	9,443,828	14/694,811	SEMICONDUCTOR DEVICE AND METHOD OF EMBEDDING THERMALLY CONDUCTIVE LAYER IN INTERCONNECT STRUCTURE FOR HEAT DISSIPATION
329	SC-P11-024 & SC-P11-037	9,666,500	14/697,352	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INSULATING LAYER DISPOSED OVER THE SEMICONDUCTOR DIE FOR STRESS RELIEF
330	SC-P09-052	9,378,064	14/697,950	SEMICONDUCTOR DEVICE AND METHOD OF MOUNTING SEMICONDUCTOR DIE TO HEAT SPREADER ON TEMPORARY CARRIER AND FORMING POLYMER LAYER AND CONDUCTIVE LAYER OVER THE DIE
331	SC-P10-003	9,418,962	14/710,393	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WLP WITH SEMICONDUCTOR DIE EMBEDDED WITHIN PENETRABLE ENCAPSULANT BETWEEN TSV INTERPOSERS
332	SC-P12-137	9,355,993	14/761,287	INTEGRATED CIRCUIT SYSTEM WITH DEBONDING ADHESIVE AND METHOD OF MANUFACTURE THEREOF
333	SC-P14-187	10,453,785	14/814,906	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DOUBLE-SIDED FAN-OUT WAFER LEVEL PACKAGE
334	SC-P13-075	9,865,554	14/855,033	INTEGRATED CIRCUIT PACKAGING SYSTEM WITH UNDER BUMP METALLIZATION AND METHOD OF MANUFACTURE THEREOF
335	SC-P09-228	9,893,045	14/971,291	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERPOSER FRAME OVER SEMICONDUCTOR DIE TO PROVIDE VERTICAL INTERCONNECT
336	SC-P10-234	9,620,557	14/974,002	SEMICONDUCTOR DEVICE AND METHOD OF FORMING EWLB SEMICONDUCTOR PACKAGE WITH VERTICAL INTERCONNECT STRUCTURE AND CAVITY REGION
337	SC-P08-073	10,211,183	15/069,719	SEMICONDUCTOR DEVICE AND METHOD OF FORMING SHIELDING LAYER OVER INTEGRATED PASSIVE DEVICE USING CONDUCTIVE CHANNELS
338	SC-P14-035	10,068,862	15/082,190	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A PACKAGE IN-FAN OUT PACKAGE
339	SC-P13-068	9,691,707	15/130,452	SEMICONDUCTOR DEVICE AND METHOD OF FORMING 3D DUAL SIDE DIE EMBEDDED BUILD-UP SEMICONDUCTOER PACKAGE
340	SC-P12-009	10,217,702	15/167,830	SEMICONDUCTOR DEVICE AND METHOD OF FORMING AN EMBEDDED SOP FAN-OUT PACKAGE
341	SC-P11-091	10,170,385	15/169,251	SEMICONDUCTOR DEVICE AND METHOD OF FORMING STACKED VIAS WITHIN INTERCONNECT STRUCTURE FOR FO-WLCSP
342	SC-P08-259	9,542,775	15/218,536	SEMICONDUCTOR DEVICE AND METHOD OF FORMING A THIN WAFER WITHOUT A CARRIER
343	SC-P13-102	10,446,523	15/218,847	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WIRE STUDS AS VERTICAL INTERCONNECT IN FO-WLP
344	SC-P11-113	9,934,998	15/379,178	SEMICONDUCTOR DEVICE AND METHOD OF SINGULATING THIN SEMICONDUCTOR WAFER ON CARRIER ALONG MODIFIED REGION WITHIN NON-ACTIVE REGION FORMED BY IRRADIATING ENERGY
345	SC-P12-101	10,242,946	15/380,788	SEMICONDUCTOR DEVICE AND METHOD OF USING SUBSTRATE HAVING BASE AND CONDUCTIVE POSTS TO FORM VERTICAL INTERCONNECT STRUCTURE IN EMBEDDED DIE PACKAGE
346	SC-P14-156	10,446,459	15/618,343	SEMICONDUCTOR DEVICE AND METHOD OF FORMING ENCAPSULATED WAFER LEVEL CHIP SCALE PACKAGE
347	SC-P13-070	10,242,887	15/674,247	SEMICONDUCTOR DEVICE AND METHOD OF MAKING EMBEDDED WAFER LEVEL CHIP SCALE PACKAGES
348	SC-P13-061	10,418,298	14/035,726	SEMICONDUCTOR DEVICE AND METHOD OF FORMING DUAL FAN-OUT SEMICONDUCTOR PACKAGE

APPENDIX B

PATENT ASSIGNMENT AND AGREEMENT

No.	Reference No.	Application No.	Title
1	SC-P09-226	15/473,447	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERPOSER FRAME OVER SEMICONDUCTOR DIE TO PROVIDE VERTICAL INTERCONNECT
2	SC-P09-226	15/473,470	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERPOSER FRAME OVER SEMICONDUCTOR DIE TO PROVIDE VERTICAL INTERCONNECT
3	SC-P11-213	13/937,952	SEMICONDUCTOR DEVICE AND METHOD OF FORMING RECONSTITUTED WAFER WITH LARGER CARRIER TO ACHIEVE MORE EWLB PACKAGES PER WAFER WITH ENCAPSULANT DEPOSITED UNDER TEMPERATURE AND PRESSURE
4	SC-P10-272	14/466,923	SEMICONDUCTOR DEVICE AND METHOD OF USING LEADFRAME BODIES TO FORM OPENINGS THROUGH ENCAPSULANT FOR VERTICAL INTERCONNECT OF SEMICONDUCTOR DIE
5	SC-P12-029	15/007,518	SEMICONDUCTOR DEVICE AND METHOD FOR FORMING A LOW PROFILE EMBEDDED WAFER LEVEL BALL GRID ARRAY MOLDED LASER PACKAGE (EWLB-MLP)
6	SC-P09-214	15/068,290	SEMICONDUCTOR DEVICE AND METHOD OF FORMING SACRIFICIAL ADHESIVE OVER CONTACT PADS OF SEMICONDUCTOR DIE
7	SC-P07-236	15/177,081	SEMICONDUCTOR DEVICE AND METHOD OF FORMING WAFER LEVEL GROUND PLANE AND POWER RING
8	SC-P09-231	15/280,632	SEMICONDUCTOR DEVICE AND METHOD OF FORMING EMI SHIELDING LAYER WITH CONDUCTIVE MATERIAL AROUND SEMICONDUCTOR DIE
9	SC-P13-031	15/457,736	SEMICONDUCTOR DEVICE AND METHOD OF FORMING ULTRA HIGH DENSITY EMBEDDED SEMICONDUCTOR DIE PACKAGE
10	SC-P11-249	15/582,418	SEMICONDUCTOR DEVICE AND METHOD OF MAKING WAFER LEVEL CHIP SCALE PACKAGE
11	SC-P10-114	15/584,897	SEMICONDUCTOR DEVICE AND METHOD OF FORMING INTERCONNECT SUBSTRATE FOR FO-WLCSP
12	SC-P13-068	15/594,443	SEMICONDUCTOR DEVICE AND METHOD OF FORMING 3D DUAL SIDE DIE EMBEDDED BUILD-UP SEMICONDUCTOER PACKAGE
13	SC-P14-005	15/675,558	SEMICONDUCTOR DEVICE AND METHOD OF FORMING CONDUCTIVE VIAS BY DIRECT VIA REVEAL WITH ORGANIC PASSIVATION
14	SC-P12-058	15/705,543	SEMICONDUCTOR DEVICE AND METHOD OF USING PARTIAL WAFER SINGULATION FOR IMPROVED WAFER LEVEL EMBEDDED SYSTEM IN PACKAGE
15	SC-P17-021	15/819,401	METHOD OF PACKAGING THIN DIE AND SEMICONDUCTOR DEVICE INCLUDING THIN DIE