

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5887458

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ULTRATECH, INC.	12/19/2019

RECEIVING PARTY DATA

Name:	VEECO INSTRUMENTS INC.
Street Address:	1 TERMINAL DRIVE
City:	PLAINVIEW
State/Country:	NEW YORK
Postal Code:	11803

PROPERTY NUMBERS Total: 190

Property Type	Number
Patent Number:	9633850
Patent Number:	10316406
Patent Number:	8202575
Patent Number:	9556519
Patent Number:	9175388
Patent Number:	9328417
Patent Number:	9777371
Patent Number:	9567670
Patent Number:	9783888
Patent Number:	9768016
Patent Number:	10090153
Patent Number:	9929011
Patent Number:	9666432
Patent Number:	9960036
Patent Number:	10351950
Patent Number:	6469788
Patent Number:	6600565
Patent Number:	6924497
Patent Number:	6513389
Patent Number:	6781702

PATENT

Property Type	Number
Patent Number:	6806578
Patent Number:	7361581
Patent Number:	7750371
Patent Number:	8455322
Patent Number:	6819566
Patent Number:	6770558
Patent Number:	6708871
Patent Number:	6583517
Patent Number:	6739497
Patent Number:	6650016
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Patent Number:	6444560
Patent Number:	6737297
Patent Number:	6864165
Patent Number:	7723824
Patent Number:	7786025
Patent Number:	8343818
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Patent Number:	7473577
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Patent Number:	6495917
Patent Number:	6569262
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Patent Number:	6593644
Patent Number:	6596621
Patent Number:	6649833
Patent Number:	6661098
Patent Number:	6667559

Property Type	Number
Patent Number:	6719188
Patent Number:	6732908
Patent Number:	6784086
Patent Number:	6819000
Patent Number:	6893799
Patent Number:	6917113
Patent Number:	7615477
Patent Number:	7635643
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Patent Number:	8637937
Patent Number:	8735251
Patent Number:	7369251
Patent Number:	7433051
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Patent Number:	6898306
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Patent Number:	6863403
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Patent Number:	8299446
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Patent Number:	8830590
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Patent Number:	9436103
Patent Number:	7116496
Patent Number:	6300208

Property Type	Number
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Patent Number:	6635541
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Patent Number:	6825101
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Patent Number:	6388297
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Patent Number:	9411163

Property Type	Number
Patent Number:	9935022
Patent Number:	7615435
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Patent Number:	9450069
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Patent Number:	8138020
Patent Number:	8138036
Patent Number:	9266437
Patent Number:	8088633
Patent Number:	7731798
Patent Number:	7326877
Patent Number:	7744274
Patent Number:	7176405
Patent Number:	8314360
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Patent Number:	8742286
Patent Number:	8153930
Patent Number:	9401278
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Patent Number:	8501638

Property Type	Number
Patent Number:	8691598
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Patent Number:	8986562
Patent Number:	9343307
Patent Number:	9613828
Patent Number:	9613815
Patent Number:	9711361
Patent Number:	10016843
Patent Number:	7348270
Application Number:	15277096
Application Number:	15877809
Application Number:	15834718
Application Number:	15145833
Application Number:	15940533
Application Number:	16036993
Application Number:	16106850
Application Number:	16429850
Application Number:	16511136

CORRESPONDENCE DATA

Fax Number: (732)560-5301

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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Email: akass@veeco.com

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Address Line 4: SOMERSET, NEW JERSEY 08873

NAME OF SUBMITTER:	ALAN P KASS
SIGNATURE:	/alan p kass 32142/
DATE SIGNED:	12/30/2019

Total Attachments: 12

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PATENT ASSIGNMENT AGREEMENT
Ultratech, Inc. to Veeco Instruments Inc.

THIS AGREEMENT is made on December 19, 2019 by and between Veeco Instruments Inc. ("Veeco"), a company incorporated in the State of Delaware, and Ultratech, Inc. ("Ultratech"), a company incorporated in the State of Delaware.

WHEREAS, Ultratech is the owner of the entire right, title and interest in and to the patents and patent applications, and the inventions disclosed therein, (hereinafter referred to collectively as the Patent Rights) described in Schedule 1;

WHEREAS, Veeco is desirous of obtaining all right, title and interest in and to the Patent Rights; and

WHEREAS, Ultratech is agreeable to assigning the Patent Rights to Veeco.

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, Ultratech has sold, assigned, transferred and set over, and by these presents does hereby sell, assign, transfer and set over, unto Veeco, its successors, legal representatives and assigns as of the effective date recited above, all right, title and interest in, to and under the Patent Rights, including specifically the right to claim priority from said Patent Rights as fully and entirely as the same would have been held and enjoyed by Ultratech if this assignment and sale had not been made, together with all claims for damages by reason of past infringement of the Patent Rights with the right to sue for and collect the same for Veeco's own use and enjoyment, and for the use and enjoyment of its successors, assigns or other legal representatives.

This Agreement shall be construed in accordance with and governed by the laws of the State of Delaware, excluding any choice of law rules which direct the application of the laws of another jurisdiction.

This assignment may be executed in any number of counterparts, each of which will be deemed an original, but all of which together constitute one and the same instrument. Executed signature pages to this assignment may be delivered by facsimile, or by email in portable document format (.pdf) and delivery of the signature page by such method will have the same effect as if the original signature had been delivered by the sending party to the receiving party.

(signature page follows)

PATENT ASSIGNMENT AGREEMENT
Ultratech, Inc. to Veeco Instruments Inc.

IN WITNESS WHEREOF, this Agreement was executed by PSP and Veeco on the date first written above.

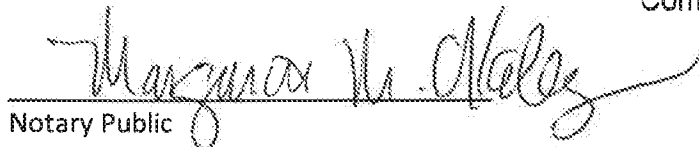
Assignor: **ULTRATECH, INC.**

Date: December 19, 2019


Signature
Gregory A. Robbins
Name Printed or typed
Secretary
Title

Subscribed to and sworn to before
me this 19 day of December, 2019.

MARGARET M. AKERLEY
Notary Public, State of New York
No. 01AK6065993
Qualified in Suffolk County
Commission Expires Nov. 5, 2021


Notary Public

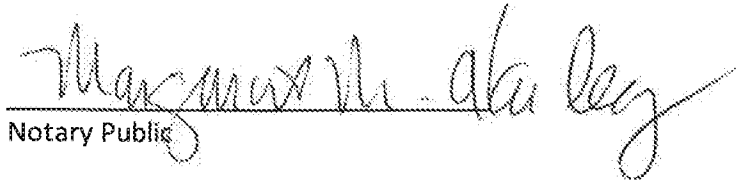
Notary Seal

Assignee: **VEECO INSTRUMENTS INC.**

Date: December 19, 2019


Signature
Gregory A. Robbins
Name Printed or typed
Secretary
Title

Subscribed to and sworn to before
me this 19 day of December, 2019.


Notary Public

Notary Seal

MARGARET M. AKERLEY
Notary Public, State of New York
No. 01AK6065993
Qualified in Suffolk County
Commission Expires Nov. 5, 2021

PATENT ASSIGNMENT AGREEMENT
Ultratech, Inc. to Veeco Instruments Inc.

SCHEDULE 1

Title	App Number	Filing Date
PLASMA ATOMIC LAYER DEPOSITION SYSTEM AND METHOD	15/277096	27-Sep-2016
CHUCK SYSTEMS AND METHODS WITH ENHANCED ELECTRICAL ISOLATION FOR SUBSTRATE-BIASED ALD	15/877809	23-Jan-2018
WAFER CHUCK WITH CONTRACTIBLE SEALING DEVICES FOR SECURING WARPED WAFERS	15/834718	07-Dec-2017
MICROCHAMBER LASER PROCESSING SYSTEMS AND METHODS USING LOCALIZED PROCESS-GAS ATMOSPHERE	15/145833	04-May-2016
LASER-ASSISTED ATOMIC LAYER DEPOSITION OF 2D METAL CHALCOGENIDE FILMS	15/940533	29-Mar-2018
LASER-BASED SYSTEMS AND METHODS FOR MELT-PROCESSING OF METAL LAYERS IN SEMICONDUCTOR MANUFACTURING	16/036993	17-Jul-2018
LASER ANNEALING SYSTEMS AND METHODS WITH ULTRA-SHORT DWELL TIMES	16/106850	21-Aug-2018
PLASMA ENHANCED ALD SYSTEM	16/429850	03-Jun-2019
HIGH-EFFICIENCY LINE-FORMING OPTICAL SYSTEMS AND METHODS USING A SERRATED SPATIAL FILTER	16/511136	15-Jul-2019

PATENT ASSIGNMENT AGREEMENT
Ultratech, Inc. to Veeco Instruments Inc.

SCHEDULE 1 (continued)

Title	Application Number	Filing Date	Patent Number	Issue Date
MASKING METHODS FOR ALD PROCESSES FOR ELECTRODE-BASED DEVICES	15/210095	14-Jul-2016	9633850	25-Apr-2017
METHODS OF FORMING AN ALD-INHIBITING LAYER USING A SELF-ASSEMBLED MONOLAYER	15/295813	17-Oct-2016	10316406	11-Jun-2019
VAPOR DEPOSITION SYSTEMS AND METHODS	11/167570	27-Jun-2005	8202575	19-Jun-2012
VAPOR DEPOSITION SYSTEMS AND METHODS	13/304676	27-Nov-2011	9556519	31-Jan-2017
REACTION CHAMBER WITH REMOVABLE LINER	12/609308	30-Oct-2009	9175388	03-Nov-2015
SYSTEM AND METHOD FOR THIN FILM DEPOSITION	12/609319	30-Oct-2009	9328417	03-May-2016
ALD SYSTEMS AND METHODS	13/203602	26-Feb-2010	9777371	03-Oct-2017
METHOD FOR HIGH-VELOCITY AND ATMOSPHERIC-PRESSURE ATOMIC LAYER DEPOSITION WITH SUBSTRATE AND COATING HEAD SEPARATION D	14/584034	29-Dec-2014	9567670	14-Feb-2017
ALD COATING SYSTEM	14/957273	02-Dec-2015	9783888	10-Oct-2017
FORMATION OF HETEROEPITAXIAL LAYERS WITH RAPID THERMAL PROCESSING TO REMOVE LATTICE DISLOCATIONS	14/899552	17-Dec-2015	9768016	19-Sep-2017
FORMATION OF HETEROEPITAXIAL LAYERS WITH RAPID THERMAL PROCESSING TO REMOVE LATTICE DISLOCATIONS	15/598763	18-May-2017	10090153	02-Oct-2018
FORMATION OF HETEROEPITAXIAL LAYERS WITH RAPID THERMAL PROCESSING TO REMOVE LATTICE DISLOCATIONS	15/597680	17-May-2017	9929011	27-Mar-2018
METHOD AND APPARATUS FOR FORMING DEVICE QUALITY GALLIUM NITRIDE LAYERS ON SILICON SUBSTRATES	14/909004	29-Jan-2016	9666432	30-May-2017
METHOD AND APPARATUS FOR FORMING DEVICE QUALITY GALLIUM NITRIDE LAYERS ON SILICON SUBSTRATES	15/457460	13-Mar-2017	9960036	01-May-2018
PLASMA ENHANCED ALD SYSTEM	15/033071	28-Apr-2016	10351950	16-Jul-2019
COHERENT GRADIENT SENSING ELLIPSOMETER	09/820094	27-Mar-2001	6469788	22-Oct-2002
Real-time evaluation of stress fields and properties in line features formed on substrates	09/560719	27-Apr-2000	6600565	29-Jul-2003
Real-time evaluation of stress fields and properties in line features formed on substrates	10/630512	29-Jul-2003	6924497	02-Aug-2005

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SCHEDULE 1 (continued)

Technique for determining curvatures of embedded line features on substrates	09/843612	25-Apr-2001	6513389	04-Feb-2003
Determining large deformations and stresses of layered and graded structures to include effects of body forces	10/157735	28-May-2002	6781702	24-Aug-2004
Copper pad structure	09/526394	16-Mar-2000	6806578	19-Oct-2004
High surface area aluminum bond pad for through-wafer connections to an electronic package	10/904677	23-Nov-2004	7361581	22-Apr-2008
Silicon germanium heterojunction bipolar transistor structure and method	11/741836	30-Apr-2007	7750371	06-Jul-2010
Silicon germanium heterojunction bipolar transistor structure and method	12/719212	08-Mar-2010	8455322	04-Jun-2013
IMPROVEMENTS IN GROUNDING AND THERMAL DISSIPATION FOR INTEGRATED CIRCUIT PACKAGES	10/605752	23-Oct-2003	6819566	16-Nov-2004
Selective filling of electrically conductive vias for three dimensional device structures	10/371466	21-Feb-2003	6770558	03-Aug-2004
Method for forming solder connections on a circuitized substrate	10/041392	08-Jan-2002	6708871	23-Mar-2004
Method and structure for joining two substrates with a low melt solder joint	10/119491	09-Apr-2002	6583517	24-Jun-2003
SMT passive device noflow underfill methodology and structure	10/145467	13-May-2002	6739497	25-May-2004
Selective C4 connection in IC packaging	10/262753	01-Oct-2002	6650016	18-Nov-2003
Multi-layered interconnect structure using liquid crystalline polymer dielectric	10/263849	03-Oct-2002	6826830	07-Dec-2004
Process for making fine pitch connections between devices and structure made by the process	09/669531	26-Sep-2000	6444560	03-Sep-2002
Process for making fine pitch connections between devices and structure made by the process	10/213872	06-Aug-2002	6737297	18-May-2004
METHOD OF FABRICATING INTEGRATED ELECTRONIC CHIP WITH AN INTERCONNECT DEVICE	10/605204	15-Sep-2003	6864165	08-Mar-2005
Methodology for recovery of hot carrier induced degradation in bipolar devices	11/744621	04-May-2007	7723824	25-May-2010
ACTIVATING DOPANTS USING MULTIPLE CONSECUTIVE MILLISECOND-RANGE ANNEALS	12/405702	17-Mar-2009	7786025	31-Aug-2010
Method for forming retrograded well for MOSFET	12/687287	14-Jan-2010	8343818	01-Jan-2013
High density interconnects	10/038483	03-Jan-2002	6764313	20-Jul-2004

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SCHEDULE 1 (continued)

Integrated chip carrier with compliant interconnect	11/502969	11-Aug-2006	7473577	06-Jan-2009
Integrated chip carrier with compliant interconnects	12/986460	07-Jan-2011	8344516	01-Jan-2013
Method of Reducing Detrimental STI-Induced Stress in MOSFET Channels	11/623935	17-Jan-2007	7618857	17-Nov-2009
Electrical interconnect structure	12/787485	26-May-2010	8476773	02-Jul-2013
In-situ ion implant activation and measurement apparatus	09/527192	17-Mar-2000	6417515	09-Jul-2002
In-situ ion implant activation and measurement apparatus	09/527698	16-Mar-2000	6488778	03-Dec-2002
Solder bump forming method and apparatus	09/521354	09-Mar-2000	6273328	14-Aug-2001
Electrical interconnect forming method	12/787527	26-May-2010	8541299	24-Sep-2013
Solder bump forming method and apparatus	09/832073	10-Apr-2001	6427898	06-Aug-2002
High density column grid array connections and method thereof	09/564110	03-May-2000	6429388	06-Aug-2002
Electronic package interconnect structure comprising lead-free solders	09/660558	12-Sep-2000	6433425	13-Aug-2002
Electrochemical etch for high tin solder bumps	09/697333	26-Oct-2000	6468413	22-Oct-2002
Method and structure of column interconnect	09/527276	17-Mar-2000	6495917	17-Dec-2002
Lead-free solder powder material, lead-free solder paste and a method for preparing same	09/511478	23-Feb-2000	6569262	27-May-2003
Electronic package interconnect structure comprising lead-free solders	10/197291	16-Jul-2002	6581821	24-Jun-2003
System of a package fabricated on a semiconductor or dielectric wafer with wiring on one face, vias extending through	09/838725	19-Apr-2001	6593644	15-Jul-2003
Method of forming a lead-free tin-silver-copper based solder alloy on an electronic substrate	10/151075	17-May-2002	6596621	22-Jul-2003
Negative volume expansion lead-free electrical connection	10/215451	09-Aug-2002	6649833	18-Nov-2003
High density area array solder microjoining interconnect structure and fabrication method	10/052620	18-Jan-2002	6661098	09-Dec-2003
Ball grid array module and method of manufacturing same	10/162830	04-Jun-2002	6667559	23-Dec-2003
Rework methods for lead BGA/CGA	09/912192	24-Jul-2001	6719188	13-Apr-2004
High density raised stud microjoining system and methods of fabricating the same	10/052591	18-Jan-2002	6732908	11-May-2004
Lead-free solder structure and method for high fatigue life	09/779812	08-Feb-2001	6784086	31-Aug-2004

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SCHEDULE 1 (continued)

High density area array solder microjoining interconnect structure and fabrication method	10/692065	23-Oct-2003	6819000	16-Nov-2004
Dual-solder flip-chip solder bump	10/248976	06-Mar-2003	6893799	17-May-2005
Lead-free alloys for column/ball grid arrays, organic interposers and passive component assembly	10/249621	24-Apr-2003	6917113	12-Jul-2005
Method and Structure for an Organic Package with Improved BGA Life	11/566956	05-Dec-2006	7615477	10-Nov-2009
METHOD FOR FORMING C4 CONNECTIONS ON INTEGRATED CIRCUIT CHIPS AND THE RESULTING DEVICES	11/380215	26-Apr-2006	7635643	22-Dec-2009
Through silicon via lithographic alignment and registration	12/690299	20-Jan-2010	8039356	18-Oct-2011
Structure to accommodate increase in volume expansion during solder reflow	09/845448	30-Apr-2001	6686664	03-Feb-2004
Through substrate via including variable sidewall profile	12/955429	29-Nov-2010	8643190	04-Feb-2014
Through silicon via for use in integrated circuit chips	13/364804	02-Feb-2012	8637937	28-Jan-2014
Through silicon via and method of fabricating same	14/046414	04-Oct-2013	8735251	27-May-2014
Full-field optical measurements of surface properties of panels, substrates and wafers	10/767406	28-Jan-2004	7369251	06-May-2008
Determination of lithography misalignment based on curvature and stress mapping data of substrates	11/716440	09-Mar-2007	7433051	07-Oct-2008
Polarization-based coherent gradient sensing systems and methods	15/152907	12-May-2016	9784570	10-Oct-2017
Machine-independent alignment system and method	09/855485	14-May-2001	6898306	24-May-2005
Lithography system and method for device manufacture	09/854226	10-May-2001	6753947	22-Jun-2004
Backside alignment system and method	09/855486	14-May-2001	6525805	25-Feb-2003
Method and apparatus for mechanically masking a workpiece	09/973790	09-Oct-2001	6680774	20-Jan-2004
Imaging stabilization apparatus and method for high-performance optical systems	09/923734	06-Aug-2001	6617555	09-Sep-2003
Dual-sided substrate measurement apparatus and methods	10/213868	05-Aug-2002	7528937	05-May-2009
Dual-sided substrate measurement apparatus and methods	12/286762	02-Oct-2008	7902040	08-Mar-2011
Large-field unit-magnification projection system	10/330567	27-Dec-2002	6879383	12-Apr-2005

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SCHEDULE 1 (continued)

Variable numerical aperture large-field unit-magnification projection system	10/336066	02-Jan-2003	6813098	02-Nov-2004
Apochromatic unit-magnification projection optical system	10/980110	01-Nov-2004	7148953	12-Dec-2006
Deep ultraviolet unit-magnification projection optical system and projection exposure apparatus	10/447128	27-May-2003	6863403	08-Mar-2005
Deep ultraviolet unit-magnification projection optical system and projection exposure apparatus	11/052239	07-Feb-2005	7177099	13-Feb-2007
Substrate-alignment using detector of substrate material	13/366199	03-Feb-2012	RE44116	02-Apr-2013
Sub-field enhanced global alignment	12/803344	24-Jun-2010	8299446	30-Oct-2012
Phase-shift mask with assist phase regions	13/066804	25-Apr-2011	8323857	04-Dec-2012
LED-based photolithographic illuminator with high collection efficiency	13/588750	17-Aug-2012	8845163	30-Sep-2014
Unit magnification large-format catadioptric lens for microlithography	13/897514	20-May-2013	8830590	09-Sep-2014
Wynn-dyson imaging system with reduced thermal distortion	13/723260	21-Dec-2012	9341951	17-May-2016
Wynne-Dyson optical system with variable magnification	14/341777	26-Jul-2014	9488811	08-Nov-2016
Wynne-Dyson projection lens with reduced susceptibility to UV damage	14/281291	19-May-2014	9436103	06-Sep-2016
High NA large-field unit-magnification projection optical system	10/976971	29-Oct-2004	7116496	03-Oct-2006
Methods for annealing an integrated device using a radiant energy absorber layer	09/505264	16-Feb-2000	6300208	09-Oct-2001
Radiation shield device and method	09/505595	16-Feb-2000	6617600	09-Sep-2003
Radiation shield device and method	09/546114	10-Apr-2000	6570656	27-May-2003
Method for annealing using partial absorber layer exposed to radiant energy and article made with partial absorber lay	09/659102	11-Sep-2000	6635541	21-Oct-2003
Method for semiconductor gate doping	09/941817	29-Aug-2001	6777317	17-Aug-2004
Acousto-optical light tunnel apparatus and method	09/595169	15-Jun-2000	6347176	12-Feb-2002
METHOD OF FORMING A SILICIDE REGION IN A SI SUBSTRATE AND A DEVICE HAVING SAME	09/547836	12-Apr-2000	6274488	14-Aug-2001
Method of forming a silicide region in a Si substrate and a device having same	09/896160	28-Jun-2001	6420264	16-Jul-2002
Apparatus having line source of radiant energy for exposing a substrate	09/536869	27-Mar-2000	6531681	11-Mar-2003
Methods for annealing a substrate and article produced by such methods	09/536927	27-Mar-2000	6825101	30-Nov-2004

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SCHEDULE 1 (continued)

Laser thermal processing apparatus and method	09/505605	16-Feb-2000	6366308	02-Apr-2002
Selective absorption process for forming an activated doped region in a semiconductor	10/122955	11-Apr-2002	6645838	11-Nov-2003
STRUCTURE AND METHOD FOR AN OPTICAL BLOCK IN SHALLOW TRENCH ISOLATION FOR IMPROVED LASER ANNEAL CONTROL	09/547834	12-Apr-2000	6388297	14-May-2002
High-speed semiconductor transistor and selective absorption process forming same	09/548326	12-Apr-2000	6380044	30-Apr-2002
Method of and apparatus for defining disk tracks in magnetic recording media	09/536867	27-Mar-2000	6671235	30-Dec-2003
Thermally induced reflectivity switch for laser thermal processing	09/592184	12-Jun-2000	6303476	16-Oct-2001
Method for laser thermal processing using thermally induced reflectivity switch	10/078842	19-Feb-2002	6635588	21-Oct-2003
Method of forming thermally induced reflectivity switch for laser thermal processing	09/933795	20-Aug-2001	6383956	07-May-2002
Thermally induced reflectivity switch for laser thermal processing	09/940102	27-Aug-2001	6495390	17-Dec-2002
Thermally induced phase switch for laser thermal processing	09/659094	11-Sep-2000	6479821	12-Nov-2002
Laser thermal process for fabricating field-effect transistors	09/698670	27-Oct-2000	6365476	02-Apr-2002
Laser thermal processing with laser diode radiation	10/653625	02-Sep-2003	7763828	27-Jul-2010
Laser scanning apparatus and methods for thermal processing	10/287864	06-Nov-2002	6747245	08-Jun-2004
Laser scanning apparatus and methods for thermal processing	10/806014	22-Mar-2004	7157660	02-Jan-2007
Method and system for laser thermal processing of semiconductor devices	10/390504	13-Mar-2003	6844250	18-Jan-2005
Laser thermal annealing of lightly doped silicon substrates	10/674106	29-Sep-2003	7148159	12-Dec-2006
Laser thermal annealing of lightly doped silicon substrates	11/478171	29-Jun-2006	7879741	01-Feb-2011
Laser thermal annealing of lightly doped silicon substrates	10/762861	22-Jan-2004	7098155	29-Aug-2006
Laser thermal annealing of lightly doped silicon substrates	11/481458	06-Jul-2006	7494942	24-Feb-2009
Substrate processing with reduced warpage and/or controlled strain	13/913045	07-Jun-2013	9401277	26-Jul-2016
Two-beam laser annealing with improved temperature performance	14/013175	29-Aug-2013	8906742	09-Dec-2014

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Two-beam laser annealing with improved temperature performance	13/359936	27-Jan-2012	8546805	01-Oct-2013
Ultrafast laser annealing with reduced pattern density effects in integrated circuit fabrication	13/134408	07-Jun-2011	8309474	13-Nov-2012
Non-melt thin-wafer laser thermal annealing methods	13/595873	27-Aug-2012	9490128	08-Nov-2016
LASER ANNEALING SYSTEMS AND METHODS WITH ULTRA-SHORT DWELL TIMES	13/909542	04-Jun-2013	8865603	21-Oct-2014
LASER ANNEALING SYSTEMS AND METHODS WITH ULTRA-SHORT DWELL TIMES	14/490446	18-Sep-2014	9558973	31-Jan-2017
Movable microchamber system with gas curtain	13/690132	30-Nov-2012	9029809	12-May-2015
Systems and methods for reducing beam instability in laser annealing	14/311747	23-Jun-2014	9559023	31-Jan-2017
High-efficiency line-forming optical systems and methods	14/744207	19-Jun-2015	9411163	09-Aug-2016
SYSTEMS AND METHODS OF CHARACTERIZING PROCESS-INDUCED WAFER SHAPE FOR PROCESS CONTROL USING CGS INTERFEROMETRY	15/362923	29-Nov-2016	9935022	03-Apr-2018
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURE	11/830867	31-Jul-2007	7615435	10-Nov-2009
METHOD OF REMOVING METALLIC, INORGANIC AND ORGANIC CONTAMINANTS FROM CHIP PASSIVATION LAYER SURFACES	11/689570	22-Mar-2007	7771541	10-Aug-2010
METHOD OF FORMING CMOS WITH Si:C SOURCE/DRAIN BY LASER MELTING AND RECRYSTALLIZATION	11/860127	24-Sep-2007	7598147	06-Oct-2009
UNDERFILL FLOW GUIDE STRUCTURES AND METHOD OF USING SAME	13/736627	08-Jan-2013	8580673	12-Nov-2013
METHOD AND APPARATUS FOR FORMING DEVICE QUALITY GALLIUM NITRIDE LAYERS ON SILICON SUBSTRATES	15/943115	02-Apr-2018	10249491	02-Apr-2019
WAFER CHUCK APPARATUS WITH MICRO-CHANNEL REGIONS	15/729877	11-Oct-2017	10468290	05-Nov-2019
SCANNING METHODS FOR FOCUS CONTROL FOR LITHOGRAPHIC PROCESSING OF RECONSTITUTED WAFERS	15/834614	07-Dec-2017	10269662	23-Apr-2019
LASER ANNEALING SYSTEMS AND METHODS WITH ULTRA-SHORT DWELL TIMES	14/941712	16-Nov-2015	10083843	25-Sep-2018
HIGH-EFFICIENCY LINE-FORMING OPTICAL SYSTEMS AND METHODS USING A SERRATED SPATIAL FILTER	15/210399	14-Jul-2016	10353208	16-Jul-2019

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SILICON GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTOR STRUCTURE AND METHOD	15/236430	13-Aug-2016	10032883	24-Jul-2018
Electronic package with optimized lamination process	11/148890	08-Jun-2005	7329816	12-Feb-2008
Electronic package with improved current carrying capability and method of forming the same	10/752176	06-Jan-2004	7332805	19-Feb-2008
Electrical interconnect forming method	12/787503	26-May-2010	8242010	14-Aug-2012
Laser annealing for 3-D chip integration	13/093798	25-Apr-2011	8138085	20-Mar-2012
Electrical interconnection package and method thereof	09/587944	06-Jun-2000	6333563	25-Dec-2001
Silicon germanium heterojunction bipolar transistor structure and method	13/852013	28-Mar-2013	9450069	20-Sep-2016
Vertical through-silicon via for a semiconductor structure	12/201580	29-Aug-2008	8097525	17-Jan-2012
Wafer level integrated interconnect decal and manufacturing method thereof	12/731793	25-Mar-2010	8138020	20-Mar-2012
Through silicon via and method of fabricating same	12/188228	08-Aug-2008	8138036	20-Mar-2012
Betavoltaic power sources for transportation applications	13/933355	02-Jul-2013	9266437	23-Feb-2016
Optical alignment methods for forming LEDs having a rough surface	12/592735	02-Dec-2009	8088633	03-Jan-2012
Heated chuck for laser thermal processing	11/001954	01-Dec-2004	7731798	08-Jun-2010
Laser thermal processing chuck with a thermal compensating heater module	11/002043	01-Dec-2004	7326877	05-Feb-2008
Methods and apparatus for temperature measurement and control on a remote substrate surface	11/820558	20-Jun-2007	7744274	29-Jun-2010
Heat shield for thermal processing	11/112647	22-Apr-2005	7176405	13-Feb-2007
Apparatuses and methods for irradiating a substrate to avoid substrate edge damage	13/164700	20-Jun-2011	8314360	20-Nov-2012
Apparatus and methods for improving the intensity profile of a beam image used to process a substrate	11/476275	28-Jun-2006	7514305	07-Apr-2009
Apparatus and method for improving the intensity profile of a beam image used to process a substrate	13/354300	19-Jan-2012	8742286	03-Jun-2014
Apparatus and methods for improving the intensity profile of a beam image used to process a substrate	12/381061	06-Mar-2009	8153930	10-Apr-2012
Apparatus and methods for improving the intensity profile of a beam image used to process a substrate	14/253570	15-Apr-2014	9401278	26-Jul-2016

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Methods of forming a denuded zone in a semiconductor wafer using rapid laser annealing	11/788192	18-Apr-2007	7732353	08-Jun-2010
Laser spike annealing for GaN LEDs	12/590360	06-Nov-2009	8592309	26-Nov-2013
Activating GaN LEDs by laser spike annealing and flash annealing	13/136019	20-Jul-2011	8658451	25-Feb-2014
Fast thermal annealing of GaN LEDs	13/199276	24-Aug-2011	8460959	11-Jun-2013
Systems and methods for forming a time-averaged line image	13/136769	10-Aug-2011	8399808	19-Mar-2013
Ultrafast laser annealing with reduced pattern density effects in integrated circuit fabrication	13/646673	06-Oct-2012	9302348	05-Apr-2016
Laser annealing scanning methods with reduced annealing non-uniformities	13/459031	27-Apr-2012	8501638	06-Aug-2013
Dual-loop control for laser annealing of semiconductor wafers	13/706397	06-Dec-2012	8691598	08-Apr-2014
Dual-loop control for laser annealing of semiconductor wafers	14/185072	20-Feb-2014	9475150	25-Oct-2016
Methods of laser processing photoresist in a gaseous environment	13/961655	07-Aug-2013	8986562	24-Mar-2015
Laser spike annealing using fiber lasers	14/497006	25-Sep-2014	9343307	17-May-2016
Method of laser annealing a semiconductor wafer with localized control of ambient oxygen	14/714544	18-May-2015	9613828	04-Apr-2017
High-efficiency line-forming optical systems and methods for defect annealing and dopant activation	14/929186	30-Oct-2015	9613815	04-Apr-2017
High-efficiency line-forming optical systems and methods for defect annealing and dopant activation	15/437055	20-Feb-2017	9711361	18-Jul-2017
SYSTEMS AND METHODS FOR REDUCING PULSED LASER BEAM PROFILE NON-UNIFORMITIES FOR LASER ANNEALING	15/064634	09-Mar-2016	10016843	10-Jul-2018
Techniques for forming interconnects	11/625449	22-Jan-2007	7348270	25-Mar-2008