PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT5919307

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ESILICON CORPORATION	01/17/2020

RECEIVING PARTY DATA

Name:	INPHI CORPORATION
Street Address:	2953 BUNKER HILL LANE
Internal Address:	SUITE 300
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State/Country:	CALIFORNIA
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PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	09912028

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NAME OF SUBMITTER:	KYLE G. ROUTEN
SIGNATURE:	/Kyle G. Routen/
DATE SIGNED:	01/20/2020

Total Attachments: 6
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ASSIGNMENT OF PATENT APPLICATION

WHEREAS, ESILICON CORPORATION hereinafter referred to as "ASSIGNOR," is an assignee by assignment recorded in the U.S. Patent and Trademark Office of the inventions described and set forth in the Applications for United States Letters Patent and United States Letters Patent identified in the Appendix attached hereto;

WHEREAS, Richard T. Ogawa, Director, and authorized representative at ESILICON CORPORATION, having authority to sell, assign, and transfer to a third party the below-identified Applications for United States Letters Patent and United States Letters Patent in the Appendix attached hereto.

WHEREAS, Richard T. Ogawa, General Counsel of INPHI CORPORATION hereinafter referred to as "ASSIGNEE," is desirous of acquiring an entirety of ASSIGNOR'S interest in the said inventions and applications and in any U.S. Letters Patent which may be granted on the same;

NOW, THEREFORE, TO ALL WHOM IT MAY CONCERN: Be it known that, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor has sold, assigned and transferred, and by these presents does sell, assign, and transfer unto the said Assignee, and Assignee's successors and assigns, 100% of their right, title, and interest in and to the said inventions, application, and U.S. Letters Patent including any corresponding foreign application, and in and to any Letters Patent which may hereafter be granted on the same in the United States and any corresponding foreign application, the said interest to be held and enjoyed by said Assignee as fully and exclusively as it would have been held and enjoyed by said Assignor had this Assignment and transfer not been made, to the full end and term of any Letters Patent which may be granted thereon, or of any division, renewal, continuation in whole or in part, substitution, conversion, reissue, prolongation or extension thereof.

Assignor further agree that they will, without charge to Assignee, but at Assignee's expense, cooperate with Assignee in the prosecution of said application and/or applications, execute, verify, acknowledge and deliver all such further papers, including applications for Letters Patent and for the reissue thereof, and instruments of assignment and transfer thereof, and will perform such other acts as Assignee lawfully may request, to obtain or maintain Letters Patent for said invention and improvement, and to vest title thereto in Assignee, or Assignee's successors and assigns.

IN TESTIMONY WHEREOF, Assignor has signed this Assignment on the date indicated.

1/17/2020
Date:

Name: Richard T. Ogawa
Title: Director

APPENDIX

Title of Invention	Application Number	Filing Date	Patent Number	Issue Date
SYSTEMS AND METHODS FOR DESIGNING INTEGRATED CIRCUITS	60/247,579	11/9/2000		
ADAPTIVE REAL-TIME WORK-IN-PROGRESS TRACKING, PREDICTION, AND OPTIMIZATION SYSTEM FOR A SEMICONDUCTOR SUPPLY CHAIN	09/912,028	7/23/2001	6748287	6/8/2004
CROSSBAR SWITCH WITH GROUPED INPUTS AND OUTPUTS	12/069,037	2/6/2008	7603509	10/13/2009
PREDICTION BASED OPTIMIZATION OF A SEMICONDUCTOR SUPPLY CHAIN USING AN ADAPTIVE REAL TIME WORK-IN-PROGRESS TRACKING SYSTEM	09/912,030	7/23/2001	7218980	5/15/2007
SYSTEM AND METHOD FOR AUTOMATING INTEGRATION OF SEMICONDUCTOR WORK IN PROCESS UPDATES	10/619,738	7/14/2003	7474933	1/6/2009
SYSTEM AND METHOD FOR AUTOMATING INTEGRATION OF SEMICONDUCTOR WORK IN PROCESS UPDATES	12/346,651	12/30/2008	7756598	7/13/2010
METHOD AND ARRANGEMENT FOR MANAGING PACKET QUEUES IN SWITCHES	09/560,105	4/28/2000	6977940	12/20/2005
DEVICE FOR DATASTREAM DECODING	09/738,720	12/15/2000	7002983	2/21/2006
DEVICE FOR DATASTREAM DECODING	11/255,759	10/21/2005	7158529	1/2/2007
APPARATUS AND METHOD FOR CONVERTING DATA IN SERIAL FORMAT TO PARALLEL FORMAT AND VICE VERSA	09/469,979	12/21/1999	7016346	3/21/2006

METHOD FOR FLOW CONTROL IN A SWITCH AND A SWITCH CONTROLLED THEREBY	09/697,708	10/25/2000	7061868	6/13/2006
METHOD AND APPARATUS FOR DISTRIBUTION OF BANDWIDTH IN A SWITCH	09/546,494	4/10/2000	7215678	5/8/2007
ARRANGEMENT AND METHOD FOR SELF-SYNCHRONIZATION DATA TO A LOCAL CLOCK	09/394,376	9/10/1999	6604203	8/5/2003
MULTICASTING METHOD AND ARRANGEMENT	09/420,909	10/20/1999	6625151	9/23/2003
QUEUE MANAGEMENT SYSTEM HAVING ONE READ AND ONE WRITE PER CYCLE BY USING FREE QUEUES	09/428,285	10/27/1999	6754742	6/22/2004
SCHEDULER METHOD AND DEVICE IN A SWITCH	09/804,591	3/12/2001	6944171	9/13/2005
MIXED-SIZED PILLARS THAT ARE PROBEABLE AND ROUTABLE	61/825,984	5/21/2013		
PARALLEL SIGNAL VIA STRUCTURE	61/825,986	5/21/2013		
TESTING OF THRU-SILICON VIAS SLAVE DLL CALIBRATION	61/825,987	5/21/2013		
SLAVE DLL CALIBRATION	61/887,583	10/7/2013		
MEMORY OPTIMIZATION IN VLSI DESIGN USING GENERIC MEMORY MODELS	14/628,105	2/20/2015	9852250	12/26/2017
INTEGRATED CIRCUIT DESIGN OPTIMIZATION	14/677,206	4/2/2015	9454636	9/27/2016
ELONGATED PAD STRUCTURE	62/089,095	12/8/2014		
WIRELESS PROBES	62/089,099	12/8/2014		
COMMUNICATION INTERFACE ARCHITECTURE USING SERIALIZER/DESERIALIZER	62/029,759	7/28/2014		

A VARIABILITY-AWARE SCHEME FOR ASYNCHRONOUS CIRCUIT INITIALIZATION	12/265,571	11/5/2008	7701255	4/20/2010
AN ASYNCHRONOUS SCHEME FOR CLOCK DOMAIN CROSSING	12/711,909	2/24/2010	8433875	4/30/2013
NETWORK OF TIGHTLY COUPLED PERFORMANCE MONITORS FOR DETERMINING THE FREQUENCY OF OPERATION OF A SEMICONDUCTOR IC	13/181,362	7/12/2011	8446224	5/21/2013
VARIABILITY-AWARE SCHEME FOR HIGH PERFORMANCE ASYNCHRONOUS CIRCUIT VOLTAGE REGULATION	12/265,585	11/5/2008	8572539	10/29/2013
GENERATING SPECIFIC MEMORY MODELS USING GENERIC MEMORY MODELS FOR DESIGNING MEMORIES IN VLSI DESIGN	14/628,668	2/23/2015	9727681	8/8/2017
DESIGNING MEMORIES IN VLSI DESIGN USING SPECIFIC MEMORY MODELS GENERATED FROM GENERIC MEMORY MODELS	14/628,676	2/23/2015	9727682	8/8/2017
SCALING LOGIC COMPONENTS OF INTEGRATED CIRCUIT DESIGN	14/678,697	4/3/2015	9460254	10/4/2016
SCALING MEMORY COMPONENTS OF INTEGRATED CIRCUIT DESIGN	14/678,702	4/3/2015	9454628	9/27/2016
SCALING OF INTEGRATED CIRCUIT DESIGN INCLUDING LOGIC AND MEMORY COMPONENTS	14/678,708	4/3/2015	9460255	10/4/2016
INTEGRATED CIRCUIT DESIGN SCALING FOR RECOMMENDING DESIGN POINT	14/678,711	4/3/2015	9460256	10/4/2016

SCALING OF INTEGRATED CIRCUIT DESIGN INCLUDING HIGH-LEVEL LOGIC COMPONENTS	14/678,715	4/3/2015	9460257	10/4/2016
COMMUNICATION INTERFACE ARCHITECTURE USING SERIALIZER/DESERIALIZER	14/810,261	7/27/2015	9984997	5/29/2018
ELONGATED PAD STRUCTURE	14/963,081	12/8/2015	10050003	8/14/2018
WIRELESS PROBES	14/963,076	12/8/2015	10018670	7/10/2018
SCALING OF INTEGRATED CIRCUIT DESIGN INCLUDING HIGH-LEVEL LOGIC COMPONENTS	15/250,885	8/29/2016		
BANDGAP CIRCUITS WITH VOLTAGE CALIBRATION	16/222,929	12/17/2018		
BAUD-RATE TIME ERROR DETECTOR	16/358,687	3/19/2019		
TRANS-IMPEDANCE AMPLIFIER (TIA) WITH A T-COIL FEEDBACK LOOP	16/298,945	3/11/2019		
SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG TO DIGITAL CONVERTER (AD) WITH PARTIAL LOOP-UNROLLING	16/239,415	1/3/2019		
SUCCESSIVE APPROXIMATION REGISTER (SAR) ANALOG TO DIGITAL CONVERTER (ADC) WITH PARTIAL LOOP-UNROLLING	16/239,421	1/3/2019		
INDUCTOR DESIGN FOR ELECTROMAGNETIC COUPLING REDUCTION	16/229,825	12/21/2018		
TUNABLE VOLTAGE CONTROLLED OSCILLATORS	16/273,047	2/11/2019		
BASELINE WANDER COMPENSATION IN SERDES TRANSCEIVERS	16/270,512	2/7/2019		
HIGH DENSITY LOW POWER	62/913,322	10/10/2019		

INTERCONNECT USING 3D DIE STACKING				